

LHCb Upgrade – Annecy  
Jan 23, 2012  
ANNECY

# Toward the readout board project

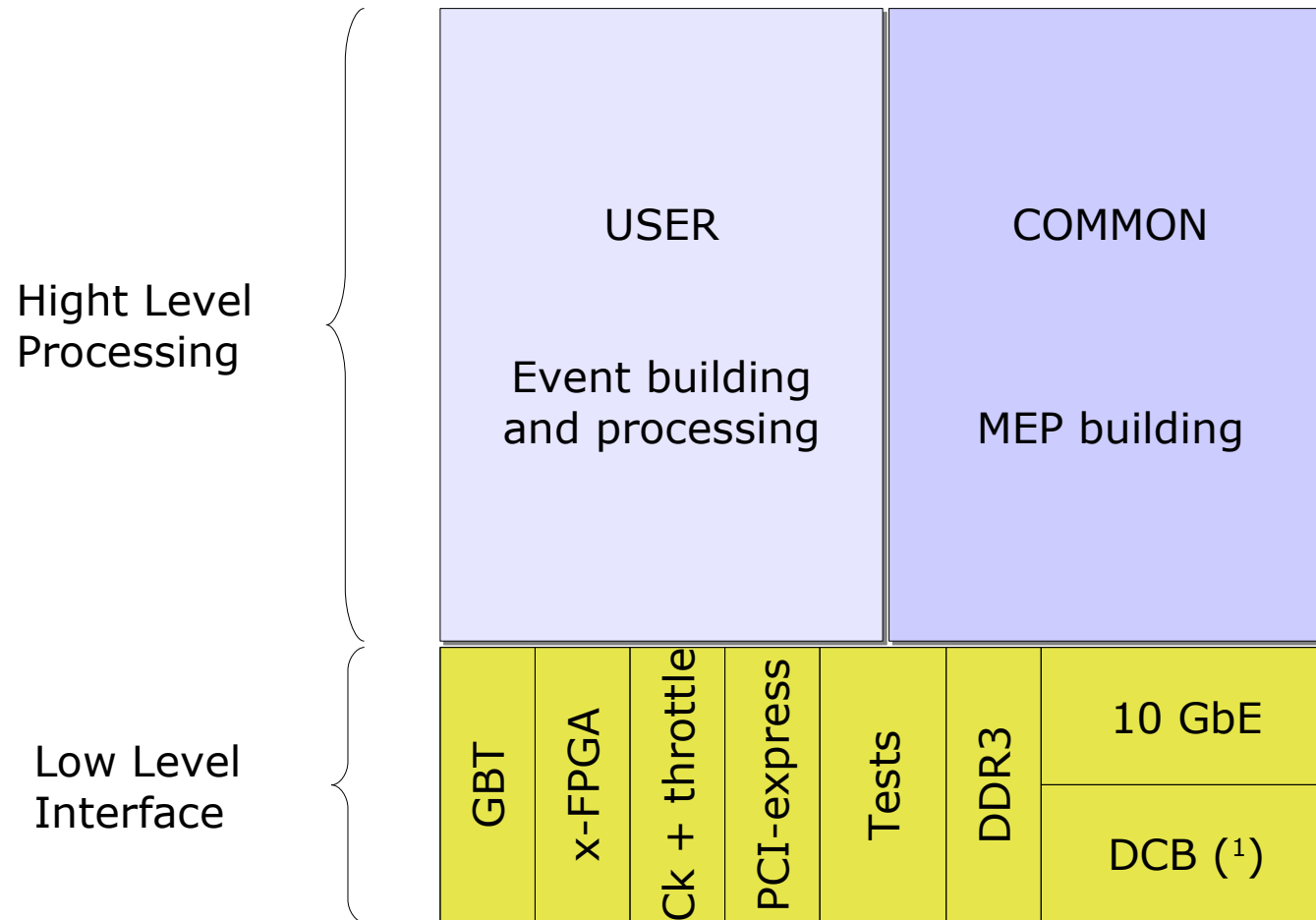
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# The Readout Board project

<i>WP</i>	<i>Work Package Title</i>	<i>Interested Lead Participant</i>
0	Coordination	Marseille
1	Hardware	Marseille
2	Firmwares	Annecy
3	PVSS Supervision	
4	Commissioning	
5	Maintenance	

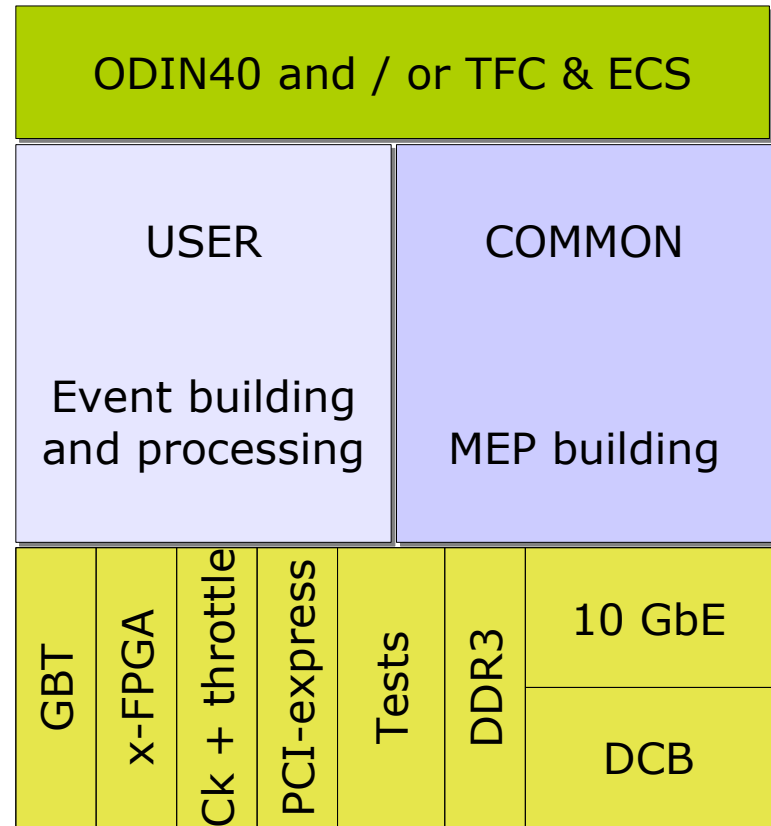
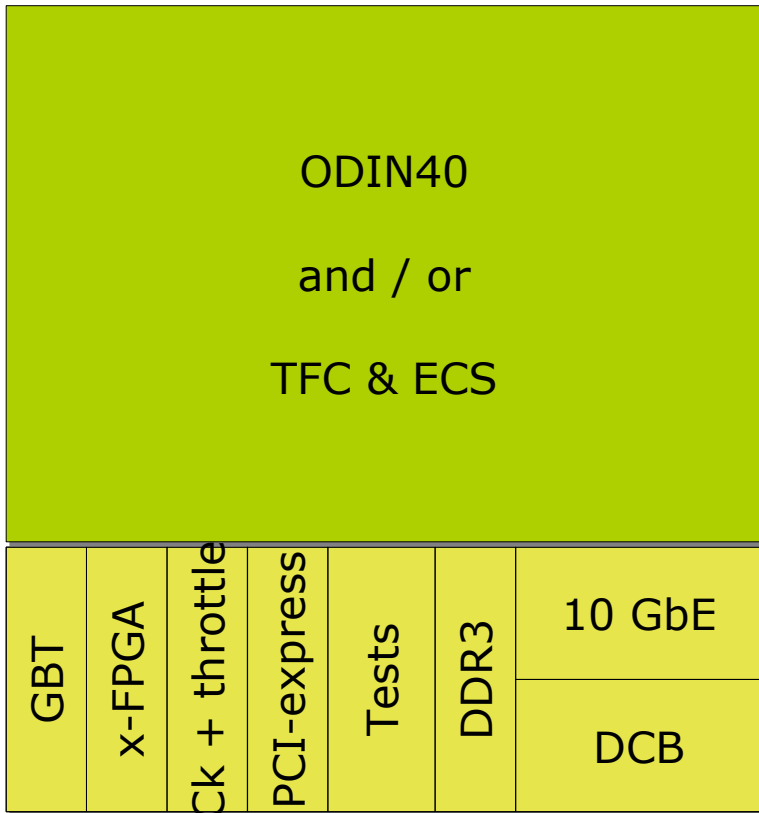
# WP 2: firmware developments

# Radiography of the TELL40 FPGA



<sup>(1)</sup> Data Center Bridging

# Variants



# Firmware Development Work Packages

<i>WP</i>	<i>Work Package Title</i>	<i>Interested Institutes</i>	<i>O(FTE)</i>
2.0	Coordination	Annecy	
2.1	Low Level Interface	Marseille	6
2.2	DCB	Cern	
2.3	TELL40 Common part		4
2.4	TELL40 Generic user part		2
2.5	ODIN, TFC & ECS	Cern	
2.6	Velopix	Manchester, AGH-Krakow	
2.7	Tracker (IT + TT)		
2.8	Tracker (OT)	Dortmund	
2.9	Tracker (Sci Fi)		
2.10	RICH		
2.11	Calo (ECAL + HCAL)		
2.12	Muon	Italie	
2.13	LLT Calo	Annecy	
2.14	LLT Muon	Marseille	2
2.15	LLT Decision	Clermont	

# Coordinating firmware development

- ▶ Share the same methodology
  - Specifications
  - Simulations
  - Reviews
  - Unitary tests
  - Documentation
  - ...
- ▶ Provide common development tools
  - Quartus with QSYS
  - Versioning
  - Scripts
  - Tracking
  - ....
- ▶ Develop a team spirit

# Next steps

- ▶ Kick off meeting with interested developers:  
requirements, architecture of TELL40 FPGA, tools, ...
- ▶ May 2012:
  - Addendum to the LoI ready:  
cost, schedule, milestones, interested institutes / commitments
- ▶ **End 2012 (R&D milestone)**
  - Validate that the selected Stratix V has enough resource to satisfy the requirements of the most demanding user (VELOPIX)
- ▶ Mid 2013:
  - TDR ready
- ▶ End 2013:
  - deploy a small fraction of the new readout in the pit