Readout board
FPGA features

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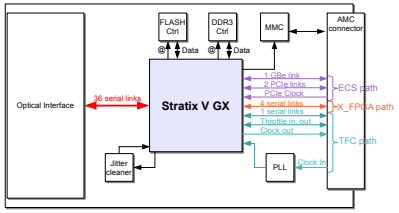
Outline

- **Mapping**
- **Common interface**
- **FPGA features**
- **Conclusion**

Readout board

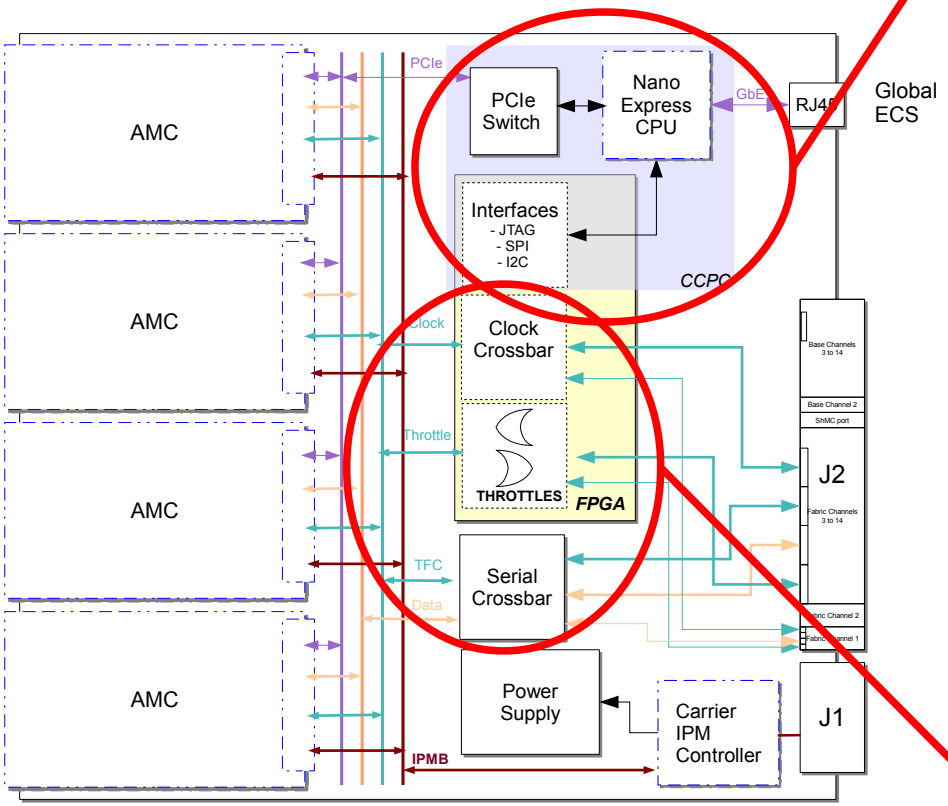
Proposal: scalable board to map all applications



Optics and processing mezzanine board

Flexible and reconfigurable carrier board

CCPC for slow control



Programmable communication matrix

Compliant with ATCA standard format

Mezzanine Card

Component on ATCA Carrier

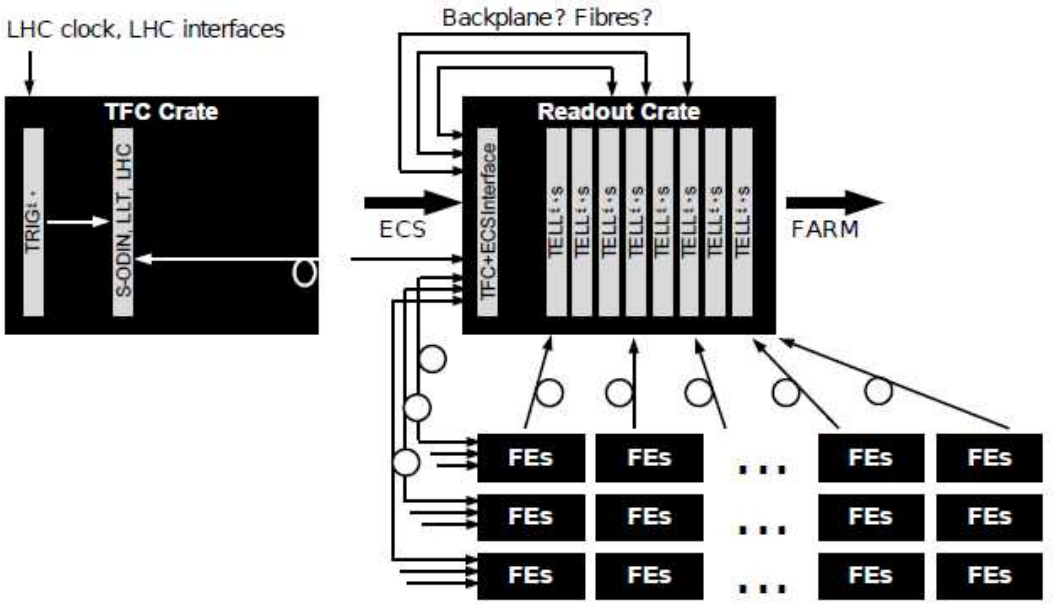
Developments mapping

One generic board

Several firmwares

- Acquisition (TELL40)
- ECS/TFC interface
- TFC
- Interface triggers

Single common development environment



Common development environment

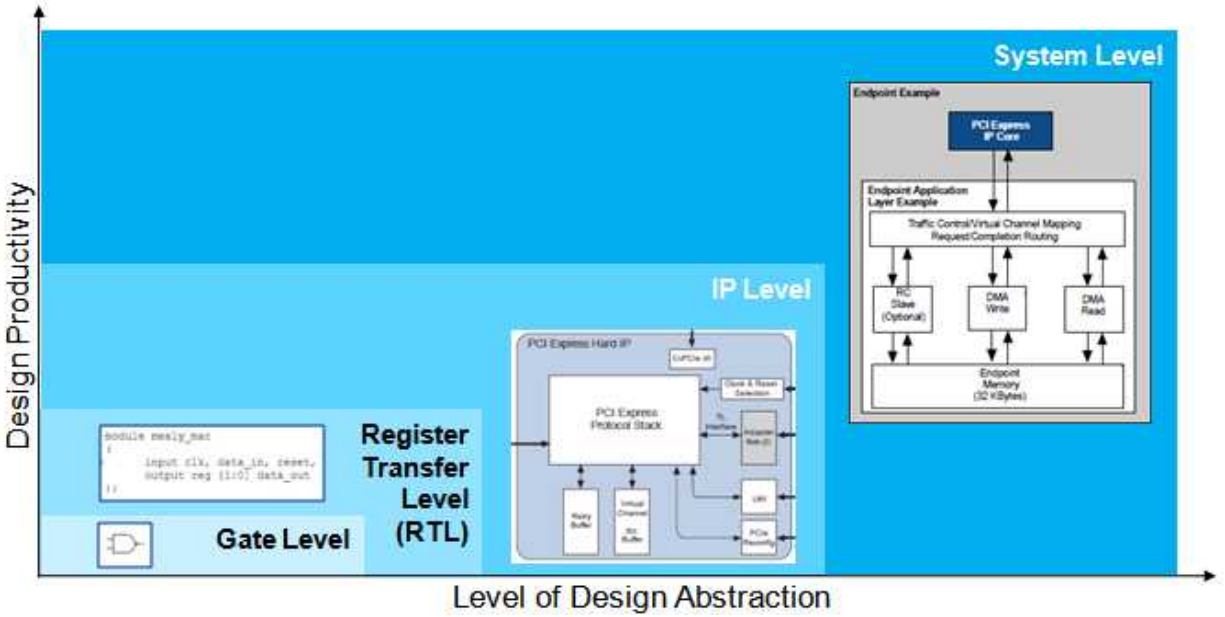
Needs

- If possible simple and unique development tool
- Clear separation between common functions and user code
- Hierarchical approach
- Block reuse
- Quick design
- Test bench for every developed function
- Test bench for the whole board

Marseille proposal

- Quartus + QSYS

Why QSYS ?



Qsys : powerful system integration tool embedded within Quartus

- High level of abstraction for design capture.
- Facilitates design reuse: custom components and systems.

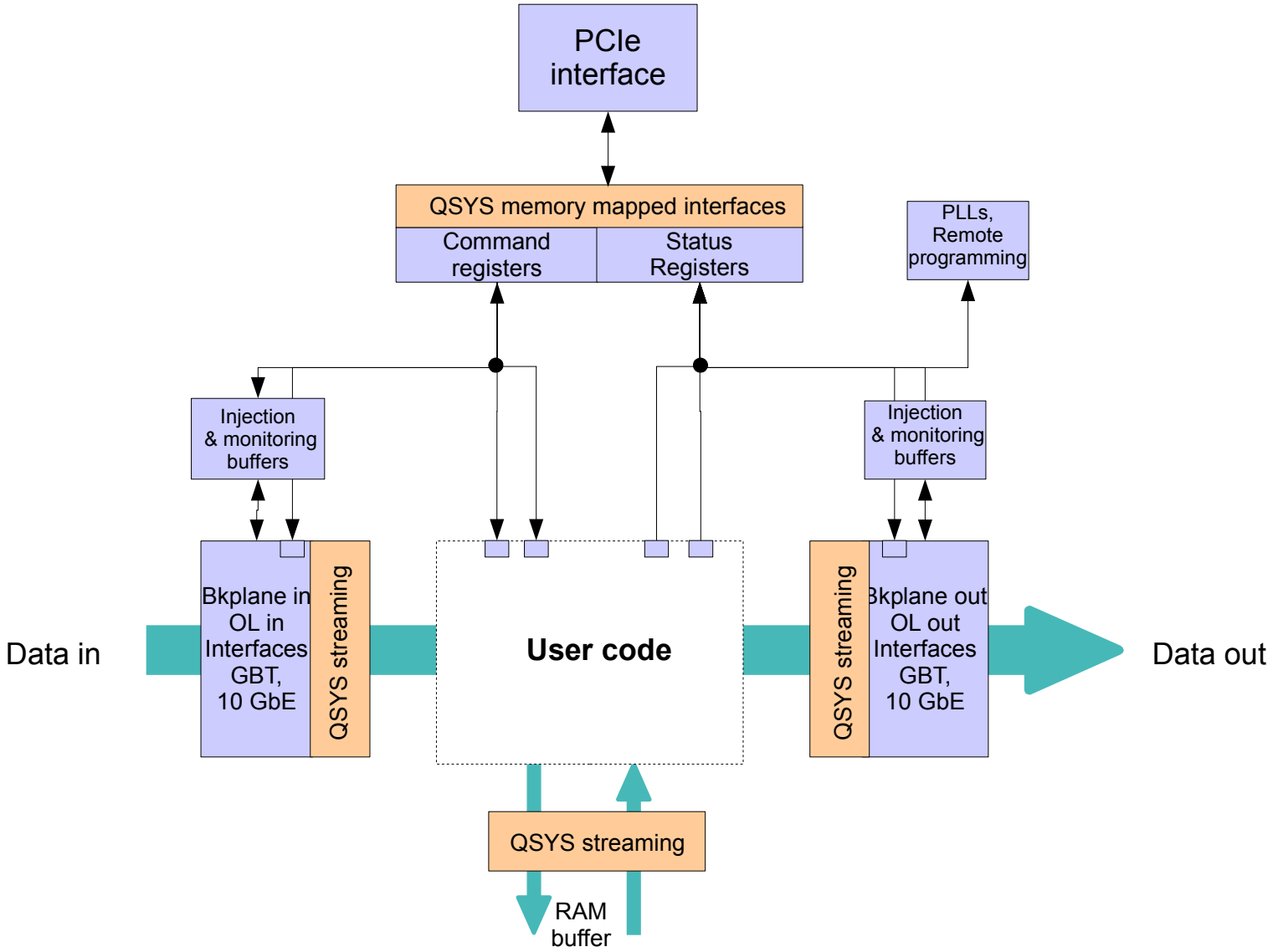
Save time by avoiding writing HDL code for interconnection

- Automatically creates high-performance interconnect logic.

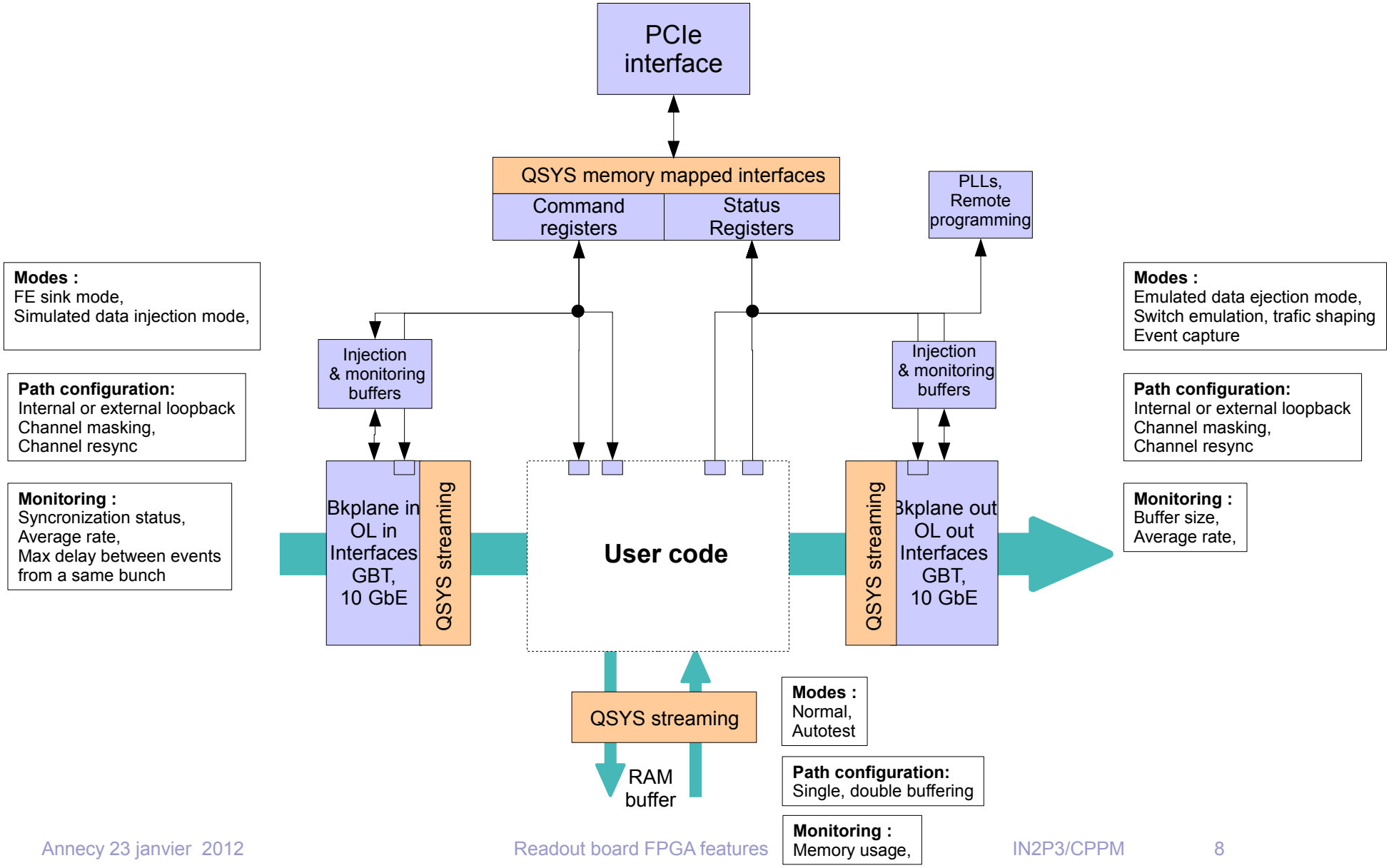
Easy way to normalize interfaces in the system

- Standard interfaces
- Documentation maintained and already available

Common interface inside FPGA



Common interface features



FPGA dimensionning

Does it fit ?

- Most demanding design : Tell40 + velopix
- Are current resources over or under dimensioned ?

Simulation will give a good estimation

Must be answered before end of year

Stratix V features

Stratix V GX Speed Grades

Feature	Core Speed -2	Core Speed -3	Core Speed -4	Units
Transceiver speed	-1: 14.1 (C) -2: 12.5 (C) -3: 8.5 (C)	- -2: 12.5 (C,I) -3: 8.5 (C,I)	- - -3: 8.5 (C,I)	Gbps
PCIe Gen1 with ECC	x1/x2/x4/x8	x1/x2/x4/x8	x1/x2/x4/x8	-
PCIe Gen2/3 with ECC	x1/x2/x4/x8	x1/x2/x4/x8	-	-
DDR3	1066	667	533	MHz
QDRII+	550	500	450	MHz
RLDRAM III	800	667	533	MHz
LVDS I/O	1.4	1.25	1.0	Gbps

ALTERA.

5SGXEA7N2F45C3N

Best compromise between
speed,
number of links,
matrix size.

Features	5SGXA3	5SGXA4	5SGXA5	5SGXA7	5SGXA9	5SGXAB	5SGXB5	5SGXB6
Logic Elements (K)	340	420	490	622	840	952	490	597
Registers (K)	513	634	740	939	1,268	1,437	740	902
14.1-Gbps Transceivers	12, 24, or 36	24 or 36	24, 36, or 48	24, 36, or 48	36 or 48	36 or 48	66	66
PCIe hard IP Blocks	1 or 2	1 or 2	1, 2, or 4	1, 2, or 4	1, 2, or 4	1, 2, or 4	1 or 4	1 or 4
Fractional PLLs	20 (1)	24	28	28	28	28	24	24
M20K Memory Blocks	957	1,900	2,304	2,560	2,640	2,640	2,100	2,660
M20K Memory (MBits)	19	37	45	50	52	52	41	52
Variable Precision Multipliers (18x18)	512	512	512	512	704	704	798	798
Variable Precision Multipliers (27x27)	256	256	256	256	352	352	399	399
DDR3 SDRAM x72 DIMM Interfaces	4	4	6	6	6	6	4	4

Stratix V GX pin migration

Possibility to increase or decrease matrix size with same pinout

Package	Stratix V GX								Stratix V GT		Stratix V GS					Stratix V E	
	A3	A4	A5	A7	A9	AB	B5	B6	C5	C7	D3	D4	D5	D6	D8	E9	EB
EH29-H780	✓										✓	✓					
HF35-F1152 (2)	✓	✓	✓	✓							✓	✓	✓				
KF35-F1152	✓	✓	✓	✓													
KF40-F1517 / KH40-H1517	✓	✓	✓	✓	✓	✓						✓	✓	✓	✓		
NF40 / KF40-F1517 (3)			✓	✓					✓	✓							
RF40-F1517							✓	✓									
H40-H1517																✓	✓
RF43-F1760							✓	✓									
NF45-F1932			✓	✓	✓	✓								✓	✓		
F45-F1932																✓	✓

Notes to Table 1–5:

(1) All devices in a given row allow migration.

(2) All devices in this row are in the HF35 package and have twenty-four 14.1-Gbps transceivers.

(3) The 5SGTC5/7 devices in the KF40 package have four 28.05-Gbps transceivers and thirty-two 12.5-Gbps transceivers. Other devices in this row are in the NF40 package and have forty-eight 14.1-Gbps transceivers.

Conclusion

Urgent verifications:

- 10 Gbits Ethernet
- Size of FPGA sufficient for Tell40 Velopix ?
- Validate development method in a multi-user context

Hardware schedule

- Prototype AMC40 board manufactured end of March
- Prototype ATCA40 board manufactured end of July
- No dependency of hardware on firmware

TELL40 simulation must start now

- Results condition FPGA optimum choice