A Radiation Detector Design Mitigating Problems Related to Sawed Edges

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Desired Radiation Detector Properties

- Backside illuminated having 100 % Fill Factor
- Fully depleted and adjustable to any thickness above 40 µm
  - TAIKO process: no lithography on the backside & no wafer bonding required
- Very thin dead layer in order to have high QE for low energy X-rays and UV photons
  - Conducting backside layer and bulk must be of opposite doping type
- Due to the thin structure the conducting backside layer must be:
  - Biased from the front side
  - Processed after the front side is finished
  - Formed with a maskless implant and annealed with a laser
- No interface dark noise generation from the sawed edges
- Low power consumption
TAIKO process
Prior work by Max-Planck Institute

Fig. 3b from US Patent no. 4837607 by J. Kemmer and G. Lutz.

- “There is no contacting of the main surface required.”
- “between the diode formed by the large-area region $p^+$ and the semiconductor body $k$ and the adjacent, undepleted semiconductor body $k$, there is only a very small or no voltage difference in the border zones of the arrangement. Thus, in certain circumstances, it is possible to implant the large-area region $p^+$ in large area manner without photolithography.”
Cross-section of a proposed p-i-n diode

Simulated structure

Suggested edge structure

p-i-n diode

V1 = -20 V
V2 = +15 V
V3 = 0 V
V4 = +15 V

Neutral area
~ 1 V

Hole flow
Electron flow

Depleted edge area

p+ backside layer ~ 1 V

p+ n+
Top view of the proposed p-i-n diode

- neutral area
- depleted area
- anode
Simulation results on the proposed p-i-n diode

Electrostatic potential distribution in the simulated p-i-n diode. The border of the neutral area on the left next to the detector edge is depicted by a white line. Elsewhere the detector is fully depleted.
Electron current distribution in the simulated p-i-n diode. The electrons generated at the depleted edge and flowing from the neutral area through the depleted bulk is represented by the yellow arc located beneath the p+ ring at $V_1$. No interface generated electrons reach the n+ doped active detector area at $V_4$.

Electron density distribution in the simulated p-i-n diode. The neutral area next to the detector edge and the flow of electrons from the neutral area to the n+ ring at $V_2$ can be easily identified.
Hole current distribution in the simulated p-i-n diode. A large reverse bias potential at the outermost p⁺ ring at $V_1$ punch-through biases the p⁺ backside layer as well as depletes the bulk. The punch through hole current is represented by the yellow column beneath the p⁺ ring at $V_1$.

Hole density distribution in the simulated p-i-n diode. The punch-through hole current from the p⁺ backside layer to the p⁺ ring at $V_1$ is represented by the green column beneath the p⁺ ring at $V_1$. 
Neutron transmutated silicon wafers to be used

Horizontal electron leakage flow from the sawed edges

Depleted edge area can be much larger than simulated due to bulk doping inhomogeneity

Use Neutron Transmutated Silicon (NTS) Wafers!
Cross-section of a proposed SDD structure
Top view of the proposed SDD structure

- Neutral area
- Depleted area
- Anode
Modified Internal Gate (MIG) detector enables:

- Non-Destructive Correlated Double Sampling (NDCDS)
- Total removal of interface generated dark noise
Cross-section of a proposed simple matrix detector
Top view of the proposed simple matrix detector

neutral area

depleted area
Thank You!

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