Development and characterisation of sensor prototypes for the Belle II Pixel Detector

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Outline

- SuperKEKB and Belle II
- Pixel Detector (PXD) and its characteristics
- DEPFET: the working principle and the pixelated matrix
- Readout electronics and mechanics
- The PXD9 and prototypes production
- Characterisation instruments and methods
- Summary and future developments
The DEPFET collaboration

- CNM/IAFE, Barcelona
- Charles University, Prague
- DESY, Hamburg
- IFCA, Santander
- IFIC, Valencia
- IFJ PAN, Krakow
- IHEP, Beijing
- KIT, Karlsruhe
- KEK-PF, Tsukuba
- LMU, Munich
- MPI Munich,
- MPG HLL, Munich
- University of Barcelona
- University of Bonn
- University of Heidelberg
- University of Giessen
- University of Göttingen
Nano beam scheme → smaller beam size (~nm) & increased beam currents (x2)
- \( \mathcal{L} = 8 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1} \) (40 times larger than in KEK)
- \( E_{e^-} = 7 \) (8) GeV & \( E_{e^+} = 4 \) (3.5) GeV
  (\( \beta \gamma = 0.42 \) (KEK) → 0.28 (SuperKEK))
- \( E_{cm} = 10.58 \text{ GeV} - Y(4S) \)

Changes involving the Vertex Detector (VXD):
- Four layers of Double Sided Si-Strip Detector (DSSD) with a larger radius
- Two layers of DEPFET pixel detector (PXD)
The Pixel Detector of Belle II

- Fast detector to keep occupancy small
- High spatial resolution
- Very short distance from the IP
- Minimum thickness and large signal
- Radiation hardness

<table>
<thead>
<tr>
<th></th>
<th>Inner layer (L1)</th>
<th>Outer layer (L2)</th>
</tr>
</thead>
<tbody>
<tr>
<td># modules</td>
<td>8</td>
<td>12</td>
</tr>
<tr>
<td>Distance from IP (cm)</td>
<td>1.4</td>
<td>2.2</td>
</tr>
<tr>
<td>Thickness (µm)</td>
<td>75</td>
<td>75</td>
</tr>
<tr>
<td>Total # pixels</td>
<td>$3.072 \times 10^6$</td>
<td>$4.608 \times 10^6$</td>
</tr>
<tr>
<td>Pixel size (µm²)</td>
<td>55, 60 x 50</td>
<td>70, 85 x 50</td>
</tr>
<tr>
<td>Sensitive area (mm²)</td>
<td>44.8 x 12.5</td>
<td>61.44 x 12.5</td>
</tr>
<tr>
<td>Sensor length (mm)</td>
<td>90</td>
<td>123</td>
</tr>
</tbody>
</table>
The DEPFET working principle

- **fully depleted bulk**
- **potential minimum for electrons**
- **the charges collected in the internal gate modulate the transistor current**
- **internal amplification** $g_q \sim 0.3 - 1.0 \text{ nA/e}^-$
- **non-destructive readout**
- **low power consumption**
- **the charge stored in the internal gate is removed by a “reset” contact**
- **Clear-gate structure used to lower the potential barrier between the internal gate and the clear**
- **DEPFETs of different flavours optimised for various applications exclusively at the MPS Semiconductor Laboratory**
The DEPFET half ladder

- High **readout speed** required to keep the number of hit pixels low at each readout frame \( \rightarrow 20 \, \mu s \rightarrow 100 \, \text{ns/electrical row} \)

- The **4-fold readout** is used:
  - 4 rows connected in parallel to gate and clear
  - Number of drain lines increases of the same factor

- Three different ASICs to readout the matrix (made in radiation hard technology):
  - **Switcher** – activates rows and clears internal gate with fast voltage pulses up to 20 V, provided with JTAG interconnectivity tests
  - **Drain Current Digitizer (DCD)** – amplification, compensation for pedestal currents, noise reduction
  - **Data Handling Processor (DHP)** – pedestal and common mode correction, data reduction and triggered readout scheme

9W for half ladder (8W at EOS)
The readout chain

- Power Patch Panel (PPP) for power filtering and impedance matching
- Data Handling Hybrid (DHH) for interconnection of the half-ladder to the outside world →
  - Clock signal from the BELLE II environment
  - Slow control master for the ASICs
  - Multiplexing data from DHP into optical link
  - ONSEN (ONline SElection Nodes) for tracking information from the SVD and definition of ROI within the PXD data

More on the DAQ and events reconstruction in P. Kodyš’ poster, Session 10
The PXD9 mechanics

- Air cooling tubes (Al-coated Carbon fibers)
- 8 silver coated pipes for dry air
- Air flow holes
- Kapton flex
- Positioning screw
- Cooling Block
  - Blue: CO₂ capillaries
  - Yellow: air channels
Beam Test at DESY – January 2014

- 4 SVD layers
- 1 PXD6 L1 half ladder (480x128 pixels, 50x50 \(\mu m^2\) pixel size and 50 \(\mu m\) thickness)
- 6 pixel detector telescope
- 1 - 5 GeV electrons
- Magnetic field (1 T)
- CO\(_2\) cooling, slow control, environmental sensors
- Alignment, tracking algorithms, ROI selection

First test with the full DAQ of the VXD

The PXD9 technology

The technology
• SOI wafer production
• 14 masks
• 10 implantations
• 2 poly-Si layers
• 3 metal layers
• Backside thinning
• Passivation

The PXD9 wafer
• 29 wafers in total
• 6 PXD9 half ladder per wafer
• 34 small PXD9 matrices
• Many diodes and capacitances
• Many test structures
Die testing method

Each testing stage involves a different measurement system and method, with possibility of rework

- IV diode characteristics between bulk and p+ implantations after Al1 allow detection of discontinuities in poly-Si and lateral shorts in the metal

- Transfer characteristics of sensor after Al2 mandatory → need to develop a very fast testing system
  - Only last four rows (1000 drains – last electrical row) to look for shorts among drain lines
  - Full characterisation of sensor (1000 x 192 tests)

- Discontinuities and 2D and 3D shorts among adjacent nets in the periphery of the silicon module developing a suitable system after Cu and wafer cutting
Wafer-level testing of PXD9 (after Al2)

Keithley SCS 4200

- 5 SMUs for static voltages

Keithley picoammeter 2612B

- #1 Keithley picoammeter 2612B
- #2 Keithley picoammeter 2612B

Keithley multiplexer card 7001-C via 96 pole ribbon cable with DIN connectors

Mainframe Keithley 7002

- 1
- 2
- 3
- 4

Keithley multiplexer card 7001-C via 96 pole ribbon cable with DIN connectors

conversion board

- 2 DIN connectors

126 drain line per step (7 SMUs)

18 drain lines per SMU

Testing time for 1000 drain lines reduced to < 30 minutes!
The Electrical Multi Chip Module (EMCM)

- Technology prototype development
- Yield measurements
- Debug of bump bonded control and readout ASICs
- Mechanical prototype for SMD mounting, flip-chipping, Kapton attachment

- Four iterations of EMCM with different layouts
- 4 EMCM and 3 PXD9 L1 design structures (customised for testing purposes) per wafer
- Many additional test structures

bump bonded steering and r/o ASICs

3 metal layers on periphery

4 layer kapton cable attached and wire bonded to Si-Module for I/O and power

screw through Si mounting to cooling structure

space for small DEPFET Matrix

load capacitor bank for switcher test

wire bond connections to small matrix
bias connections of matrix via kapton

long “drain” lines connected to DCD input,
more passives to emulate load of DEPFET cell, EMC tests
Some numbers:
• test points = 25522
• nets = 15036
• open tests = 10486
• short tests = 773080

Technical difficulties:
• probes number
• testing time
• probing pad size
• collision-free software
• hit mark quality

The solution:
Custom development of a flying needle system via R&D in collaboration with the company atg Luther & Maelzer
• Electrical 2D and 3D tests possible
• Typical testing time for a full wafer shortened to 3h
• Extremely high accuracy
• Output files containing list of faults detected in each DUT
Assembled die electrical characterisation

- 6 Switcher and 4 DCDs/DHPs
- Passive components
- PCB for signal probing connected via wire bonds to Al pads
- Jig for Kapton fixing and PCBs mounting

\[ f_t = 305 \text{ MHz} \]
Prototypes and sensors current status

Metal system optimisation

- 3 iterations of EMCM with 12 different technologies produced and tested
- Many info on the technology from additional test structures available on wafer
- Best ILD1 identified with 100% yield → needs confirmation
- Further EMCM(4) produced and currently under test
- Electrical characterisation of a fully populated module (i.e. all ASICs and Kapton) currently ongoing

PXD9 characterisation

- AI1
  - Detection of discontinuities and lateral shorts with possibility of repair

- AI2
  - Development of a complex switching system with probe card
  - Measurement of transfer characteristics
  - Possibility of rework in case of faults

- Cu
  - Periphery testing after Cu using the atg prober for final pre-assembly quality assurance and yield determination
Summary and future developments

- The DEPFET PXD detector promises an excellent spatial resolution of ~ 10 µm and an occupancy as low as 1%, due to a fast readout (50kHz) and a large number of pixels (~ 8Mpix);

- The technology used for the production of the DEPFET PXD is extremely complex and yet fully functional;

- The SOI technique allows full control on the thickness of the DEPFET ladders, which have been thinned down to 75 µm (0.2% X₀), minimizing multiple scattering;

- The final VXD DAQ has been tested and proves to be working;

- Best technology for the metal system identified after three EMCM productions;

- Characterisation system for full wafer testing within hours with extremely high probing accuracy developed;

- Final sensor production completed up to the metallisation;

- Metal system production starting in October 2014.
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Thank you for your attention!