Contribution ID: **61** Type: **Poster Presentation**

# Low-area trim DAC in 40nm CMOS technology for pixel readout chips used in hybrid detectors.

*Wednesday, September 10, 2014 2:00 PM (1h 40m)*

The recent directions of development in hybrid pixel detectors working in single photon counting mode are nanometer or 3D technologies that support the trend of making pixels smaller and more functional at the same time. Usually single pixel in readout electronics for X-ray detection comprises of charge amplifier, shaper and discriminator that allow to classify events occurring at the detector as true or false hits by comparing obtained signal with threshold voltage, which minimizes the influence of noise effects. However, making the pixel size smaller often causes problems with pixel to pixel uniformity [1] and additional effects like charge sharing become more visible [2].

To improve channel-to-channel uniformity or implement an algorithm for charge sharing effect minimization, a small area trimming DAC working in each pixel independently is necessary [3]. However, meeting the requirement of small silicon area often results in poor linearity and even non-monotonicity of DAC [4]. In this paper we present a low-area monotonic thermometer-coded 6-bit DAC with novel binary-to-thermometer decoder.

Monte Carlo simulations were performed on the design proving that under all conditions designed DAC is inherently monotonic. Presented DAC was implemented in the 40nm CMOS technology in the prototype readout chip with 432 pixels working in single photon counting mode, with two trimming DACs in each pixel. The area of single 6-bit DAC is about 28 μm x 10 μm. Measurements and chips' tests were performed to obtain reliable statistical results covering temperature and range characterization of the DACs, together with the tests with X-ray radiation.

This work was supported by National Science Center, Poland under Contract DEC-2011/01/B/ST7/05155

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**Session Classification:** Session 10: Posters 1 (Particle Physics, Pixel Detectors and Lifesciences)

**Track Classification:** Advances in Pixel Detectors and Integration Technologies