Experimental results for Cherwell MAPS sensors.

M.Borri (STFC)
on behalf of the Arachnid collaboration.

- Cherwell family.
- The ALICE ITS upgrade.
- The SRS DAQ-system.
- Results for Cherwell.
- Future and conclusion.
Cherwell family.

- Cherwell is a CMOS monolithic active pixel sensor (MAPS).
- It is designed by the CMOS Sensor Design Group at Rutherford Appleton Laboratory (RAL).
- The design of the Cherwell family exploits the **deep P-well technology**.
- Deep p-well allows for a more complex in-pixel processing while preserving charge collection efficiency (e.g. strixel).
- A deep P implant shields the N-wells used as substrate for PMOS transistors.
- The deep P-well technology was patented by the CMOS Sensor Design Group at RAL in collaboration with the foundry Tower Jazz.
- The **strixel approach** incorporates amplifiers, comparators and memories within the pixel matrix.
- This allows for a reduction of the dead area of the chip.
Cherwell prototypes.

Cherwell1 (2010)
- General purpose R&D chip.
- Pixels designed for tracking and vertexing applications.
- These pixels are a demonstrator of strixel approach.
- Pixels are also designed for digital calorimetry applications (e.g. linear collider experiments).

Cherwell2 (2013)
- Pixels designed for tracking and vertexing applications.
- Produced as part of the R&D for the ALICE upgrade.
- Full strixel approach.

Cherwell3 (2014)
- Optimized version of Cherwell2.
- Produced as part of the R&D for the ALICE upgrade.

The goal is to optimize:
- diode layout.
- radiation hardness.
- power consumption.
ALICE ITS upgrade.

- ALICE is one of the main experiments at the Large Hadron Collider.
- ALICE focuses on the physics of strongly interacting matter at extreme energy densities (i.e. Quark Gluon Plasma).
- The **Inner Tracking System** (ITS) allows for track finding and primary vertex reconstruction.
- The ITS upgrade is scheduled during the second long shut-down of the LHC (2018-2019).
- The upgrade is based on the LHC plans to increase the instantaneous luminosity.
- For Pb-Pb collisions, \( L = 6 \times 10^{27} \text{ cm}^{-2} \text{s}^{-1} \) with collision rate of 50 kHz.

### Aims of the upgrade:
- A total of seven pixel layers.
- Reduction of material budget.
- Faster read-out.
- Smaller radius beam-pipe (first layer closer to interaction point).

**MAPS** are the technology of choice for the ITS upgrade.
General requirements.

- MAPS match the majority of the requirements for the tracking systems.
- Small spatial resolution due to high granularity (e.g. 20 μm × 20 μm).
- Low material budget due to low power consumption and sensor thickness.
- There are limitations to radiation tolerance and moderate read-out time.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Inner barrel</th>
<th>Outer barrel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intrinsic spatial resolution</td>
<td>5 μm</td>
<td>10 μm</td>
</tr>
<tr>
<td>Max. silicon thickness</td>
<td>50 μm</td>
<td></td>
</tr>
<tr>
<td>Chip size</td>
<td>15 mm × 30 mm</td>
<td></td>
</tr>
<tr>
<td>Max. dead area on chip</td>
<td>2 mm (rφ), 100 μm (z)</td>
<td></td>
</tr>
<tr>
<td>Max. power density</td>
<td>300 mW/cm²</td>
<td>100 mW/cm²</td>
</tr>
<tr>
<td>Max. integration time</td>
<td>10% at 50 kHz Pb-Pb</td>
<td>99%</td>
</tr>
<tr>
<td>Max. detection efficiency</td>
<td>10⁻⁵</td>
<td></td>
</tr>
<tr>
<td>Max. fake hit rate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TID radiation hardness</td>
<td>700 krad</td>
<td>10 krad</td>
</tr>
<tr>
<td>NIEL radiation hardness</td>
<td>10¹³ nₑq/cm²</td>
<td>3 × 10¹⁰ nₑq/cm²</td>
</tr>
</tbody>
</table>

![ITS radiation levels graph](image)

![Pie chart](image)
Detector technology.

0.18 μm CMOS process by TowerJazz.
ALICE R&D focuses on assessing radiation hardness, and studying the deep p-well approach to design circuits that minimize power consumption and integration time.

- **Transistor size**: 0.18 μm, gate oxide thickness of 4 nm; increased hardness to ionizing dose.
- Feature size and metal layers: reduces digital circuitry located at the periphery of the chip.
- Deep p-well: complex in-pixel processing.
- **High resistivity**: a sizable part of the epitaxial layer can be depleted; increased hardness to NIEL.
- **Epitaxial thickness**: up to 40 μm; increases the amount of ionized charge.
- Stitching: production of large area sensors, reduces gaps between sensors; easier sensor alignment on a stave.
Cherwell2

- The pixel circuitry allows for correlated double sampling (CDS) and is operated in rolling-shutter mode.
- The chip features pixels with **different source followers** (different transistor M11).
- Cherwell2 exists in two read-out flavours: analogue (Cherwell2.3) and digital (Cherwell2.1).
- An additional digital version of the chip (Cherwell2.2) features pixels with a poly-implant surrounding the collecting diode.
- Chips have been produced in **different materials** and **epitaxial thicknesses**.
- Known issues: 1 faulty bias-pad, 1 faulty output-pad.
- From simulation, the **faulty bias-pad** seems not to affect the chip functionality.
- The **faulty output-pad** required a re-working of the timing diagrams to read-out the chip (→ longer integration time).

### Wafer variants

<table>
<thead>
<tr>
<th>Epi-thickness</th>
<th>Resistivity</th>
<th>Total thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 µm</td>
<td>&gt;30 Ωcm</td>
<td>700 µm</td>
</tr>
<tr>
<td>18 µm</td>
<td>&gt;1 kΩcm</td>
<td>700 µm</td>
</tr>
<tr>
<td>20 µm</td>
<td>&gt;6 kΩcm</td>
<td>50 µm</td>
</tr>
<tr>
<td>20 µm</td>
<td>&gt;2 kΩcm</td>
<td>700 µm</td>
</tr>
<tr>
<td>30 µm</td>
<td>&gt;1 kΩcm</td>
<td>450 µm</td>
</tr>
</tbody>
</table>

### Devices Under Test (DUT)

<table>
<thead>
<tr>
<th>Detector</th>
<th>Cherwell2.3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>analogue</td>
</tr>
<tr>
<td>Pixel size</td>
<td>20×20 µm²</td>
</tr>
<tr>
<td>Pixels matrix</td>
<td>128×128</td>
</tr>
<tr>
<td>Pixel variant</td>
<td>M11@0.18 µm, col 0-63</td>
</tr>
<tr>
<td></td>
<td>M11@0.35 µm, col 64-127</td>
</tr>
<tr>
<td>Epi-thickness</td>
<td>18 µm</td>
</tr>
<tr>
<td>Epi-resistivity</td>
<td>&gt;1 kΩcm</td>
</tr>
<tr>
<td>Integration time</td>
<td>14 ms (nominal 32 µs)</td>
</tr>
</tbody>
</table>
SRS system.

- The SRS system is the DAQ-system to test Cherwell2.
- Scalable Readout System (SRS) is a general purpose read-out system.
- It has a modular topology:
  - Two Front-End Cards (FECs) contain most of high-complexity components (e.g. FPGA).
  - Adapter Cards interfacing FECs with the proximity board.
  - Proximity board sends/receives signals to/from master/slave FEC.
  - Carrier board plugged onto proximity.
- Software and hardware were customized at Daresbury Laboratory to test Cherwell2.
- Customization based on initial work by ITS community.
Photon transfer curve (PTC).

- PTC is a standard technique for the characterization of imaging sensors.
- Images for different intensities of lights are acquired.
- The signal mean ($\mu$) and standard deviation ($\sigma$) are calculated for each intensity.
- Points [$\mu$, $\sigma$] are plotted in log-log scale forming a photon transfer curve.

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<td>Correlated double sampling</td>
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<td>Pedestal subtraction</td>
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- **Read noise** any source of noise that is not a function of signal.
- **Shot noise** is the standard deviation of the number of interactions per pixel.
- **Fixed pattern** noise is the pixel-to-pixel difference in sensitivity.
- **Full-well capacity** defines the amount of charge an individual pixel can hold before saturating.

![Photon transfer curve diagram](image)
PTC results.

Parameter	Formula	Expectation
Gain, $k$	$10^{-p_0/p_1}$	$\sim 0.12$ [ADC/e]
Read noise	$\sigma_{ped}/k$	$\sim 30$ [e]
Lin. F-W	$\mu_{max}/k$	$\sim 6000-8000$ [e]

- Measured parameters are substantially different from expectation.
- Gain is at least a factor of 2 lower than expected.
- Read noise and full-well are at least a factor of two higher than expected.
- These can be addressed to an over estimate of the diode capacitance during design.
Iron-55 technique.

- Radioactive sources are a way to test the signal collection of detectors.
- Fe-55 produces a signal similar to a MIP traversing a 20 µm epitaxial layer.

$$\text{^{55}_{26}Fe^{29} + e^-} \xrightarrow{\Delta E=231.21 \text{ keV}} \text{^{55}_{25}Mn^{30} + \nu_e}$$

28% probability of emission of X-rays at 5.9 keV.

- Data analysis technique as in ITS-upgrade community.
- Clustering based on S/N of individual pixels.
- S/N > 5 for seed, S/N > 3 for neighbor.

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<td>Common-mode subtraction</td>
</tr>
<tr>
<td>Masking</td>
</tr>
<tr>
<td>cds = reset - sample</td>
</tr>
<tr>
<td>s = cds - pedestals</td>
</tr>
<tr>
<td>reject common-mode noise</td>
</tr>
<tr>
<td>reject dead and noisy pixels</td>
</tr>
</tbody>
</table>

Data analysis: signal extraction

Correlated double sampling: $\text{cds} = \text{reset} - \text{sample}$
Pedestal subtraction: $s = \text{cds} - \text{pedestals}$
Common-mode subtraction: reject common-mode noise
Masking: reject dead and noisy pixels
Fe55 results.

- S/N for seed pixels is always $\lesssim 32$ ($\lesssim 28$).
- The most probable value (MPV) is 16.8 (14.7).
- Charge sharing occurs mostly between two pixels.
- This is an effect of low S/N.
Fe55 results.

- Calibration peak extracted from the seed signal distribution.
- Calibration peak fully collects charge from X-rays.
- Charge collection efficiency (CCE) for cluster: \[
\frac{\text{cluster peak}}{\text{calibration peak}} = 90.0\% \ (91.2\%).
\]
Future.

Cherwell3
- Optimized version of Cherwell2.
- It allows for masking of individual pixels.
- Improved digital circuitry to save power.
- **Four different types of diodes** implemented.
- Chip received from TowerJazz.
- Currently upgrading SRS system to test the chip.

Test beam coming up @ CERN SPS. 27th October - 2nd November.
Conclusion.

- Cherwell family has been a competing technology for the ALICE ITS upgrade.
- Designers developed deep P-well and pioneered the 0.18\(\mu\)m process.
- Both are now adopted by other technologies for the ALICE ITS upgrade.
- Cherwell2 performance is impaired by the capacitance of the collecting diode.
- Faulty pads required a longer integration time.
- Cherwell3 was optimised based on Cherwell2 results and will be tested soon.
BACK-UP
• It allows for CDS and is operated in rolling-shutter mode.
• Two pixel matrices for tracking and vertexing.
• Both variants have same pixel circuitry: 4T structure.
• Reference matrix has read-out circuitry at the end of column.
• Strixel matrix has read-out circuitry embedded in columns.
• Reference matrix tested with PTC, Fe-55 and beam tests.
• Strixel matrix has been under test only recently.
• Substantial difference between reference and strixel.

Reference matrix main results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>[ADC/e]</td>
<td>0.17</td>
</tr>
<tr>
<td>Read-noise</td>
<td>[e]</td>
<td>12</td>
</tr>
<tr>
<td>Spatial resolution</td>
<td>[µm]</td>
<td>3.7</td>
</tr>
<tr>
<td>Tracking efficiency</td>
<td>[%]</td>
<td>99.7</td>
</tr>
</tbody>
</table>