Adaptive Gain Integrating Pixel Detector

“AGIPD, a high dynamic range fast detector for the European XFEL”

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Outline

- Intro – detector challenges
- AGIPD concepts
- ASIC
- Experiments
- Summary
Detector challenges

Constraints and challenges for the detector:

- Sufficient radiation hardness (>10 MGy)
- Low noise (<500 e)
- High dynamic range (up to $10^4$ 12 keV photons)
- XFEL timing compliant
- Lowest possible dead area
- Vacuum compatible
- Central hole

Key features of the European XFEL

- Very high peak brilliance and intensity (>10$^{32}$ pht/pulse)
- Highly coherent fast pulses (< 100 fs)
- 4.5 MHz pulse repetition rate
- 2700 images per train
Detector structure

AGIPD 1M consists of 16 detector modules:

Digital part: FPGA daughter board on carrier board

Analogue part: 64 ADC channels on a two board system

Vacuum board with a flexible connection

Detector head: 512x128 pixel sensor bump bonded to 8x2 ASICs

Data transfer on one of 4 10G compatible standard ethernet links via TCP/UDP

ASIC with charge integrating readout and analogue frame storage behind each pixel

Si-Sensor with (200μm)^2 pixels
Mechanical concept

- PCB as vacuum barrier
- Control PCB’s
- Digital PCB’s with FPGA, RAM and 10GbE
- Analogue PCB’s with ADC

Module
Focal plane
Movable quadrants to adjust beam hole
Semi-ridged PCB’s allow 2-dim. move
Each readout chip contains a square matrix of 64 x 64 pixels, read out on four ports. The ASIC structure includes:

- **Sensor**
  - Preamp RST
  - C_f, high
  - C_f, mid
  - C_f, low
  - C_couple
  - CDS stage
  - Preamplifier stage
  - Dynamic gain switching
  - V_ref

- **Writing chain**
  - Charge sensitive preamplifier with 3 selectable gains
  - Gain switching control circuit and a DAC to encode the switch settings

- **CDS stage**
  - CDS RST
  - C_f, CDS

- **Discriminator**

- **Analogue memory of 2 x 352 cells (value and gain)**

- **Double column buffer**
  - (interleaved, precharging signal to bus)

- **Analogue multiplexer**

- **Pixel buffer (charge sensitive)**

- **Double column buffer (x64)**

- **Readout chain**
  - PXB RST
  - C_f, PXB
  - Storage cell matrix
  - Pixel buffer
  - Cmd based IF, periphery, DACs

- **Offchip driver (Fully differential Amplifier)**

- **Command line based interface (Digital control circuit)**
ASIC: characterization

**Non-linearity**

- (RMS) 0.26 % - (MAX) 0.4 x12.4 keV @ 46 x12.4keV
- (RMS) 0.30 % - (MAX) 10.5 x12.4 keV @ 1105 x12.4keV
- (RMS) 0.44 % - (MAX) 48.9 x12.4 keV @ 4632 x12.4keV

**Gain Ranges**

- **HIGH gain range (x12.4 keV):** 50
- **MED gain range (x12.4 keV):** 1200
- **LOW gain range (x12.4 keV):** 5000 (+5000)

**Graph**

The graph shows the non-linearity of the ASIC with different gain ranges and their corresponding values at various x12.4 keV levels.
ASIC: characterization

AGIPD1.0 - Chip 1 - Noise over Dynamic Range (x12.4 keV) - LASER (IR)

Noise performance
- Noise (x12.4 keV)
- Poisson limit

ENC = 265e- RMS

5 % Shot-to-Shot fluctuation
ASIC: AGIPD 1.0 layout

Single pixel of $(200\mu m)^2$ with bump bonds

Digital buffers, power buses

Interface pads $200\times80 \mu m$ rectangle – convenient wirebonding

Analog multiplexer and buffers, power buses

I/O ports - LVDS input, differential output, bias DACs, digital control circuit
ASIC: Pixel layout

Memory array
352 cells

Analogue channel – CSA, CDS, discriminator, gain bit logic, switches, pixel buffer

Column switch

Memory cell switches

Analogue value capacitor

Memory cell

Gain bit capacitor
Experiments: AGIPD 0.4 @P10

Image of the direct beam

Single photon sensitivity @7.05 keV

- Average intensity: 0.3 photons per 200 ns
- Count rate: 1.5 Mcps/pixel or 37.5 Mcps/mm²
- RMS noise of this pixel: 320 electrons.
Experiments: AGIPD 0.4 @P01

- 40 bunch mode (192 ns bunch spacing)
- Photon energy: 14.4 keV
- High-resolution monochromator and KB-mirror used

Experiments: AGIPD 1.0 @P10

From prototypes to the full scale ASIC

Single shot imaging synchronized to PETRA III running at 5.2 MHz

Averaged image
Experiments: AGIPD module @APS

Single module test system and DAQ software
Single bunch imaging – a challenge to find processes fast enough

Experimental setup

- Drilled equidistant holes into a DVD
- DVD covered with zinc paint to increase absorption
- Mounted DVD on a fast electric motor
- Measurement of hole to hole frequency with diode and oscilloscope: 1.208kHz

Experiments: AGIPD module @APS
Experiments: AGIPD module @APS

Calculation for burst imaging

- APS bunch spacing: \[ t = 154 \text{ns} \]
- Number of pixels crossed during burst of 352 images: \(~ 8\)
- Pixel size: \( 200 \mu\text{m} \)

\[ V_{\text{disc, AGIPD}} = 29.51 \text{m/s} \]

\[ V_{\text{disc, Laser}} = 29.83 \text{m/s} \]

Result from laser measurement

Single bunch imaging is possible even at a repetition rate of 6.5MHz!!
AGIPD systems

• First 1M, SPB beamline
• Second 1M, MID beamline
  • Carbon copy of 1st 1M system with flange adapter
• AGIPD 4M, SFX station on SPB beamline
  • Needs redesign of boards
  • New/revised mechanics needed
• 2-module downstream detector
  • Only for SPB beamline
• Single module systems
  • Mechanics can be a lot simpler (no moving parts)
• Dedicated PETRA/PSI systems?
  • Would single modules be sufficient?
• AGIPD 2.0?
  • New ASIC?
  • New sensor?
Summary

● Adaptive gain approach is tested and working
● High dynamic range allows for direct imaging of the synchrotron beam along with single photon sensitivity
● Burst imaging up to 6.5 MHz frame rate
● First single module system successfully tested at APS

Ongoing activities:

• Wafer testing
• Edgeless sensors (talk by Jiaguo Zhang) and TSVs
• Design of additional boards and mechanics for different AGIPD systems
• ASIC developments
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There are open positions for PostDocs and Master/PhD students!
http://photon-science.desy.de/research/technical_groups/detectors/index_eng.html
Backup
Detector structure

Si-Sensor with pixels 200μm squared

Digital PCBs for preprocessing and data transfer adapted to train cycle

Analogue PCBs for filtering and digitization

Interconnections and power board to adapt to mechanical needs and provide power

Off detector DAQ for data handling

ASIC with electronics to store and transfer the charge

X-rays

Detector structure
One megapixel system without vacuum tank

Wing layout and downstream detector

Modules and quadrants
ASIC: prototype development

AGIPD 0.1 Jan. 2009  AGIPD 0.2 May 2009  AGIPD 0.3 Nov. 2010  AGIPD 0.4 Nov. 2011  AGIPD 1.0 Apr. 2013

- No pixels
- 3 readout blocks consisting of:
  - Readout chain (Preamp + CDS stage)
- 3 different kinds of leakage current compensation
- 16 x 16 pixels
- 100 storage cells
- No leakage current compensation
- Different combinations of preamps and storage cell architectures

- 16 x 16 pixels
- 200 storage cells
- Radiation hard storage cell design
- High speed command based control interface
- Improved discriminator and CDS buffer

- 16 x 16 pixels
- High sensitivity preamp (Cf = 60 fF)
- 352 storage cells
- Double-column readout
- New multiplexer
- New off-chip buffer
- No command based control circuit

Full-scale chip:
- 64 x 64 pixels
- High sensitivity preamp (Cf = 60 fF)
- 352 storage cells
- Double-column readout
- High speed command based control interface
- Ready for TSV

First imaging tests with the AGIPD prototype chips in an X-Ray box. The 'A' was made from copper. From left to right: AGIPD0.2, AGIPD0.3, AGIPD0.4, AGIPD1.0 – AGIPD0.2 „A“ in addition to the fragment of an AGIPD logo made of Sn soldering wire.
ASIC: characterization

Values measured with chiptester box
Single module test system

Single module system in the lab with housing – existing and new design

Old

New design

New cooling block

Fans

Front

Back
AGIPD single module compact design