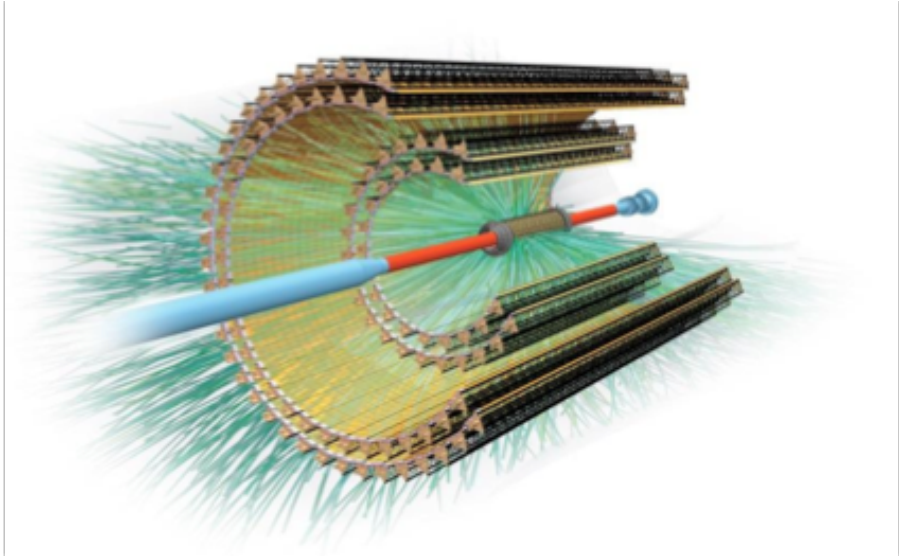
A Large Ion Collider Experiment



Development of CMOS pixel sensors for the upgrade of the ALICE inner tracking system

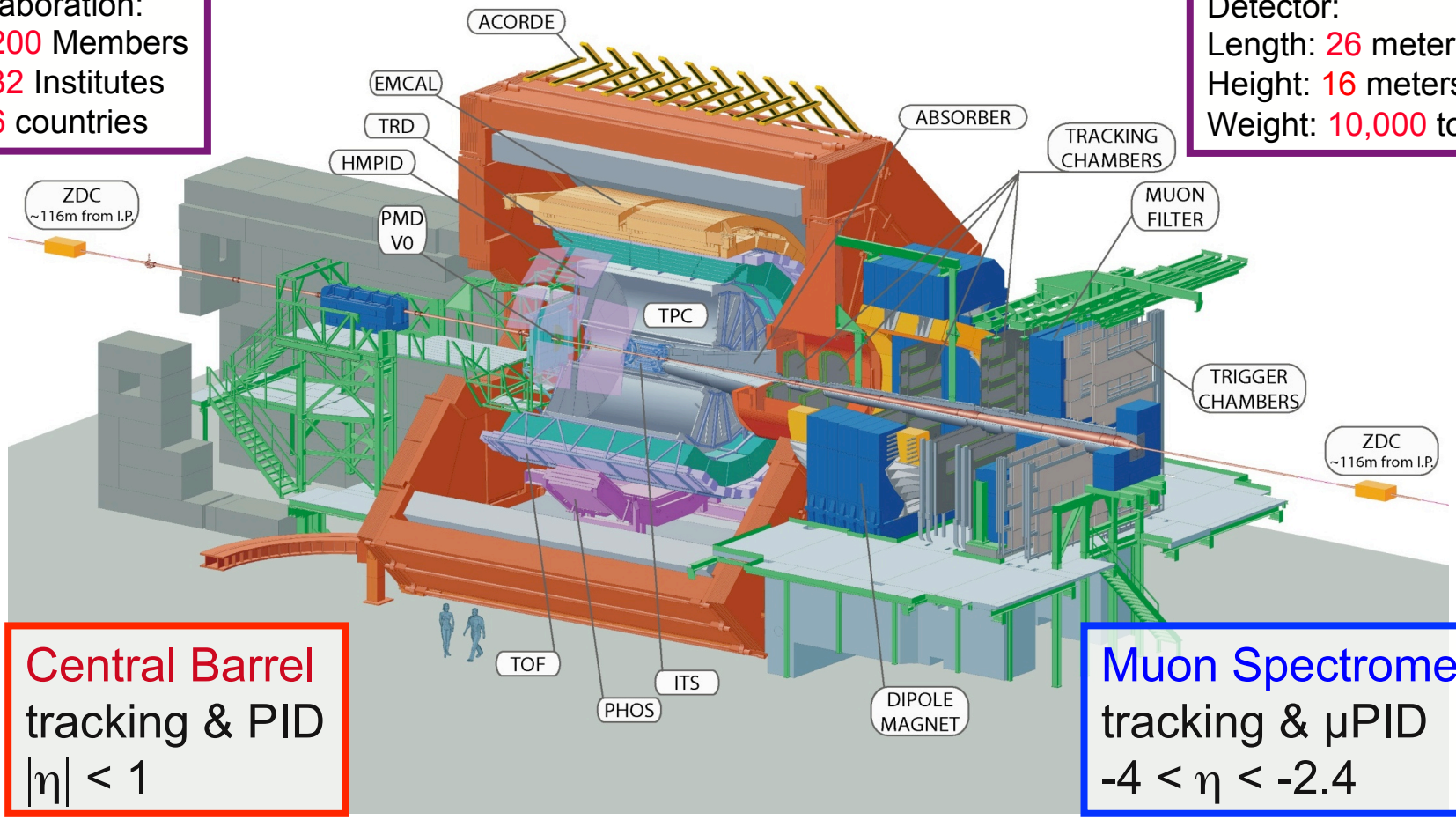
OUTLINE

- ALICE setup and Upgrade Strategy
- Inner Tracking System Upgrade
  - Requirements and performance
  - Pixel technology and R&D
  - Full scale prototypes
- Summary

A LARGE ION COLLIDER EXPERIMENT

Collaboration:
> 1200 Members
> 132 Institutes
> 36 countries

Detector:
Length: 26 meters
Height: 16 meters
Weight: 10,000 tons



Central Barrel
tracking & PID
$|\eta| < 1$

Muon Spectrometer
tracking & μPID
$-4 < \eta < -2.4$

Goal of ALICE: Experimental study of the phase diagram of the hadronic matter in ultra relativistic heavy ion collisions

ALICE UPGRADE STRATEGY

Physics program requires 10 nb^{-1} of integrated luminosity of Pb-Pb collisions wrt. the approved program of 1 nb^{-1}

Physics signals of interest are rare but not triggerable

- Low p_T (below 1 GeV/c), high combinatorial background
- Increase rate capabilities for minimum bias heavy-ion collisions to 50 kHz – 100 kHz

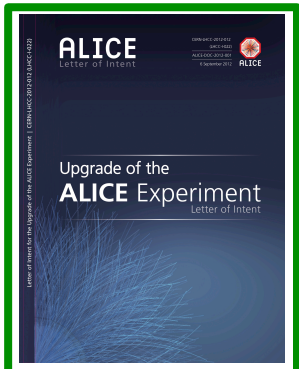
ALICE runs at high luminosity

- Factor 100 increase in statistics (for untriggered probes)
- Requires smaller beam pipe, new detectors: ITS, MFT, upgraded TPC read-out chambers and readout electronics upgrade for other detectors
- New combined online-offline framework: O^2

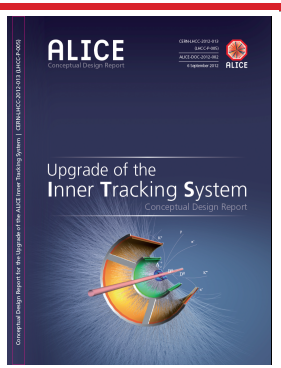
Preserve ALICE uniqueness

- Low p_T measurements and particle identification

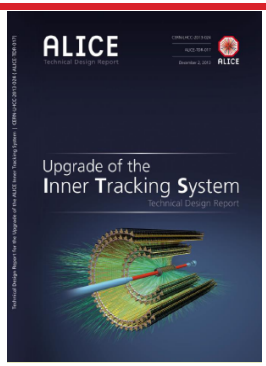
Upgrade in the 2nd LHC Long Shutdown (LS2) 2018/19



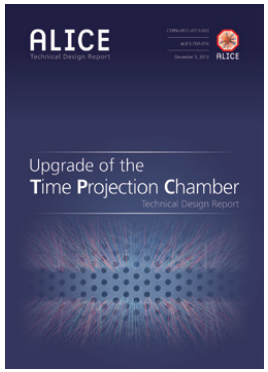
CERNLHCC-2012-012, LHCC-I-022, 2012.



CERN-LHCC-2012-005, LHCC-G-159, 2012.



CERN-LHCC-2013-024 ; ALICE-TDR-017



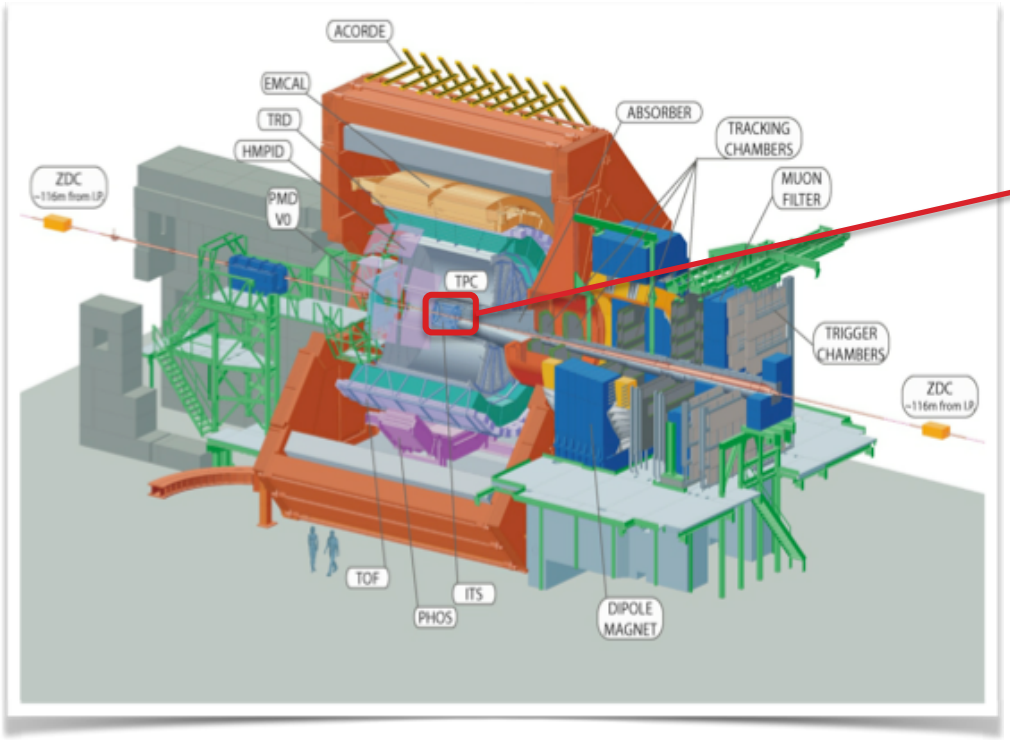
CERN-LHCC-2013-020 ; ALICE-TDR-016

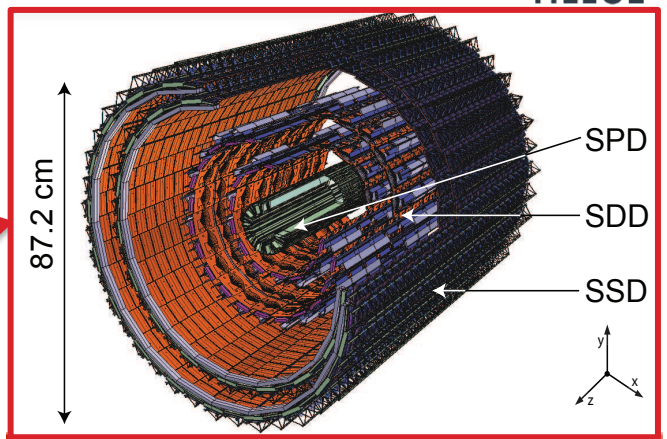
CERN-LHCC-2013-019 ; ALICE-TDR-015

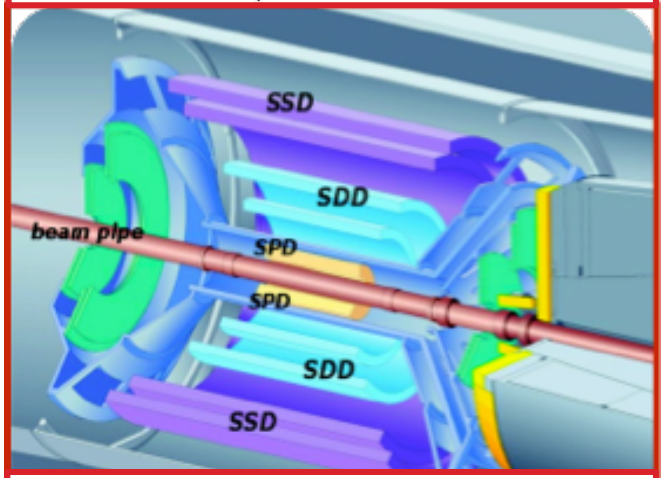
CERN-LHCC-2013-014 ; LHCC-I-022-ADD-1

Full list and details of upgrade strategy: ALICE LoI, CERN-LHCC-2012-012

ALICE INNER TRACKING SYSTEM BEFORE LHC LS2







The current Inner Tracking System (ITS) contains 6 layers of Si detectors:
2 layers of Silicon Pixel Detectors (SPD)
2 layers of Silicon Drift Detectors (SDD)
2 layers of Silicon Strip Detectors (SSD)

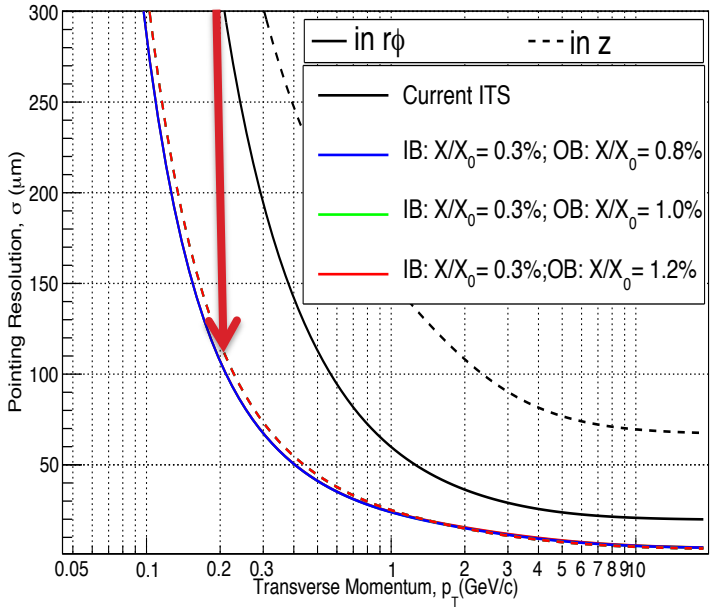
- Tracking and particle identification
- Secondary vertex reconstruction (c,b decays), track impact parameter resolution:
  < 60 μm (rφ) for p_T > 1 GeV/c in Pb-Pb
- Prompt L0 trigger capability < 800 ns (SPD), eg. high multiplicity trigger in pp

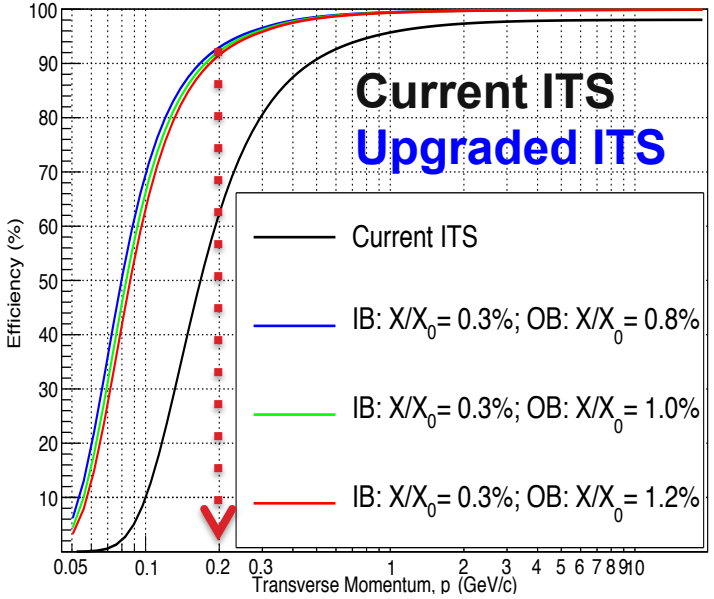
MOTIVATION FOR A NEW INNER TRACKING SYSTEM

- Improve impact parameter resolution by factor ≈ 3(5) in r-φ(z)
  - move closer to IP (position of first layer): 39 mm → 22 mm
  - reduce material budget X/X_0 / layer: from ~1.14% …
    … to 0.3% (inner layers) and to 0.8 % (outer layers)
  - reduce pixel size: 50 μm × 425 μm→*O*(30 μm × 30 μm)
- Improve tracking efficiency and p_T resolution at low p_T
  - increase granularity: 6 layers → 7 layers
- Fast readout (now limited at 1 kHz with full ITS):
  - Pb-Pb: up to 100 kHz
  - pp: several 100 kHz
- Fast insertion/removal
  - possibility to access for yearly maintenance

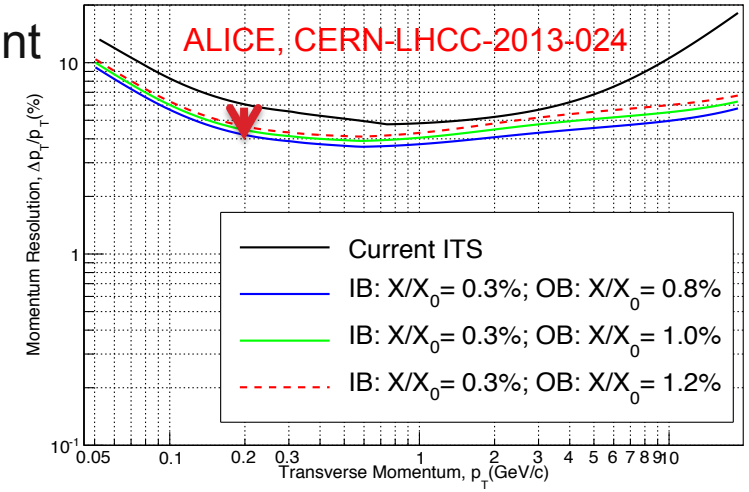
The new ALICE ITS will fully replace the present ITS !

PRESENT AND UPGRADED ITS PERFORMANCE





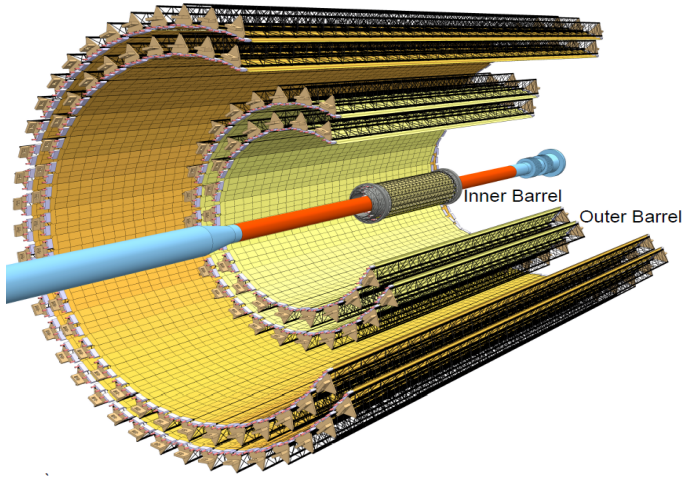
- Standalone track resolution improvement factor ~3(5) in rφ(z) at p_T ~ 200 MeV/c
- Standalone tracking efficiency ~ 90 % at p_T ~ 200 MeV/c
- Improvement in momentum resolution for standalone tracking



LAYOUT OF THE UPGRADED ALICE ITS

- 7 layers layout:
  - 3 layers of Inner Barrel
  - 4 layers of Outer Barrel

~ 12.5 Gigapixels, binary readout
~ 10 m^2 of silicon



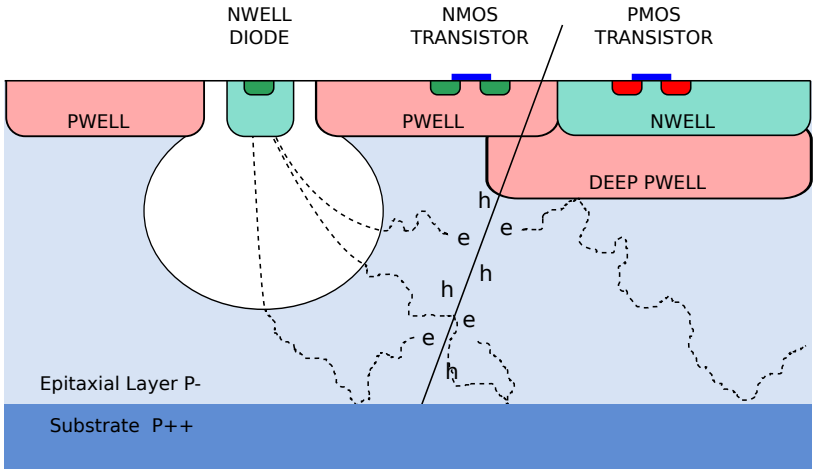
- Radial coverage: 22 mm to 400 mm

- η coverage: $|\eta| \leq 1.22$, for tracks from 90 % most luminous region

- Expected radiation level (innermost layer, including a safety factor 10):
  700 krad (TID) and 1×10^{13} 1 MeV n_{eq} (NIEL)

PIXEL TECHNOLOGY

- Requirements:
  - very thin sensors
  - very high granularity
  - cover large area
  - withstand modest radiation level
- Choice:
  - monolithic silicon pixel sensors using TowerJazz 0.18 µm CMOS Imaging Process
    - high-resistivity (1-6 kΩcm) epitaxial layer on p-type substrate
    - deep p-well to shield PMOS: true CMOS circuitry in the pixel



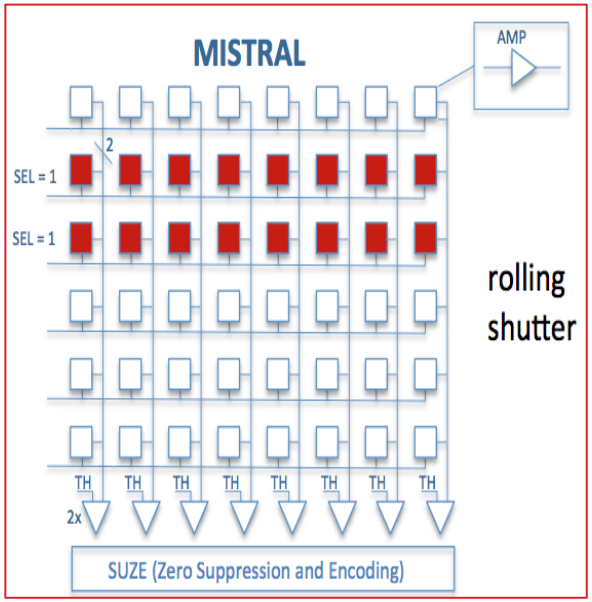
ALICE, CERN-LHCC-2013-024

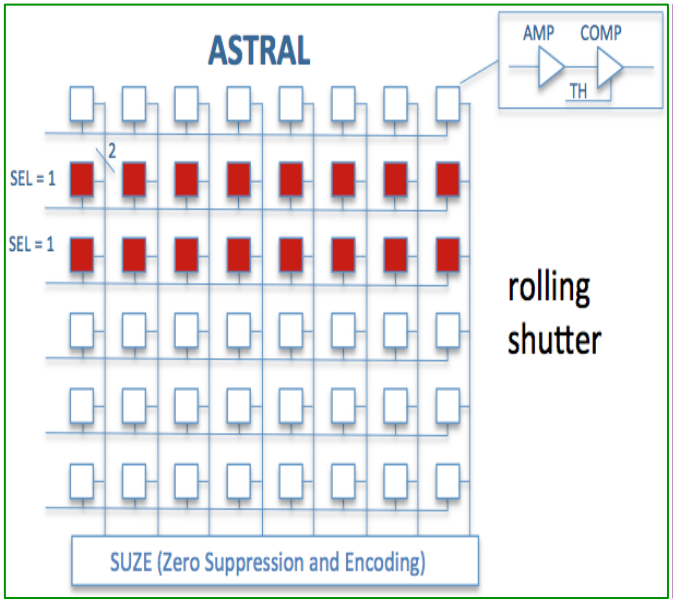
Nwell diode output signal: V ~ Q/C

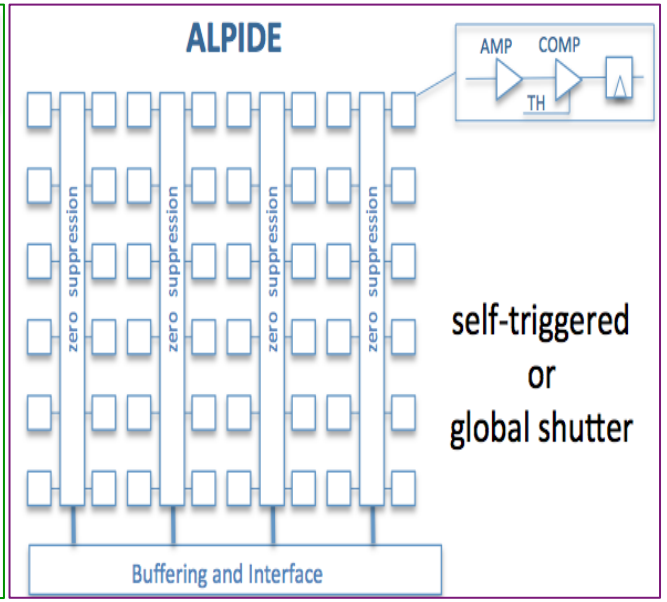
- minimize charge spread over different pixels
- minimize capacitance
- small diode surface (~ 100x smaller than pixel area) and large depletion volume
- Moderate bias voltage on the substrate can increase depletion zone around the Nwell charge collection diode

PIXEL CHIP VERSIONS UNDER DEVELOPMENT

ALICE, CERN-LHCC-2013-024







- Three pixel chip architectures under development: MISTRAL / ASTRAL and ALPIDE
  - MISTRAL/ASTRAL: based on the ULTIMATE chip of the STAR PXL detector
- Decision on the ALICE Pixel Chip architecture for the ITS Upgrade: beginning of 2015

Specifications:

- Chip size: 15 mm x 30 mm
- Pixel pitch: ~ 30 µm
- Si thickness: 50 µm
- Spatial resolution: ~ 5 µm
- Power density: < 100 mW/cm^2
- Integration time: < 30 µs

PIXEL CHIP R&D

Dedicated R&D to develop an ALICE pixel chip since 2011

Several small scale and recently full-scale prototypes have been realized to …

- … improve Signal-over-Noise ratio (SNR)
- … implement different read-out and front end architectures
- … investigate radiation hardness

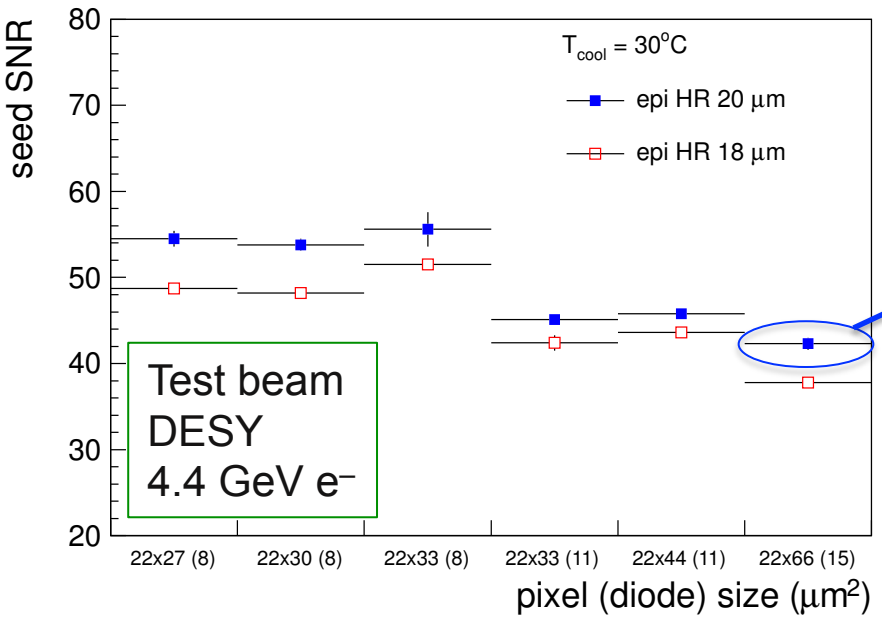
Architecture	Analogue prototype	Digital prototype	
		Small-scale	Full-scale
ASTRAL / MISTRAL	MIMOSA-32-X MIMOSA-34	MIMOSA-22THR-X AROM-0/1	FSBB A0 FSBB M0
ALPIDE	Explorer-0 Explorer-1	pALPIDE	pALPIDEfs

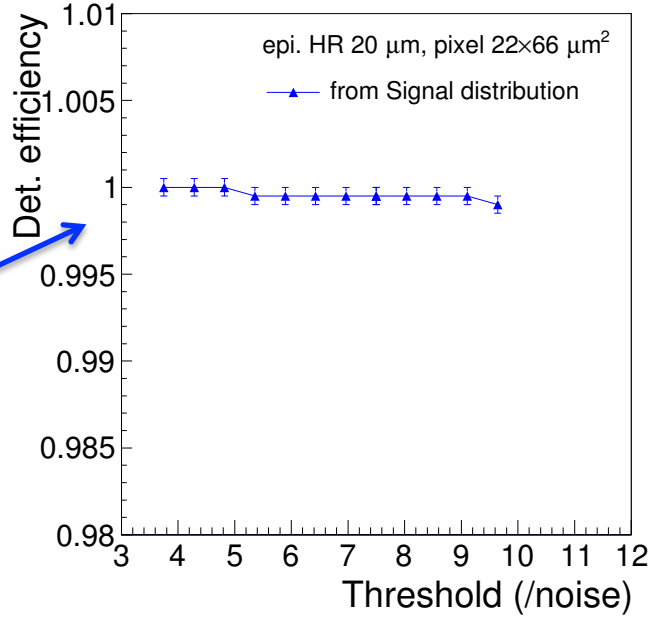
FSBB: Full Scale Building Block = 1/3 of a full chip

PIXEL CHIP R&D

ASTRAL / MISTRAL – MIMOSA-34

ALICE, CERN-LHCC-2013-024





- Analogue, no in-pixel pre-amplification and CDS circuitry

  CDS: correlated double sampling

  – sensing node optimisation: pixel size, epitaxial layer characteristics

- Pixel size varies from 22 × 27 µm² to 22 × 66 µm²

- High detection efficiency even for large 22 × 66 µm² pixels

PIXEL CHIP R&D

ALPIDE – EXPLORER 1

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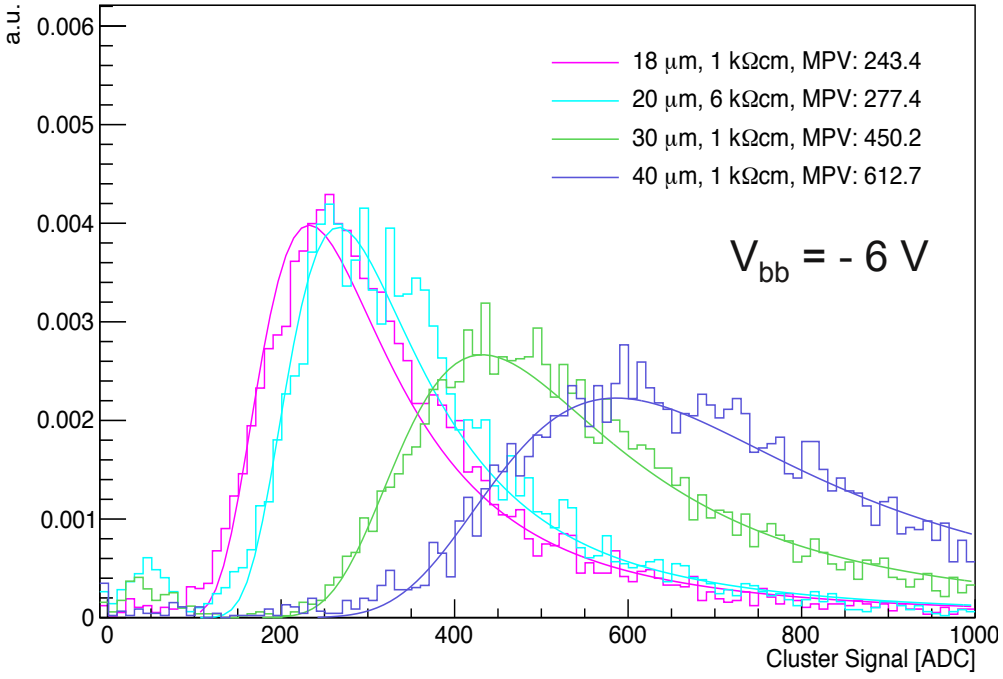
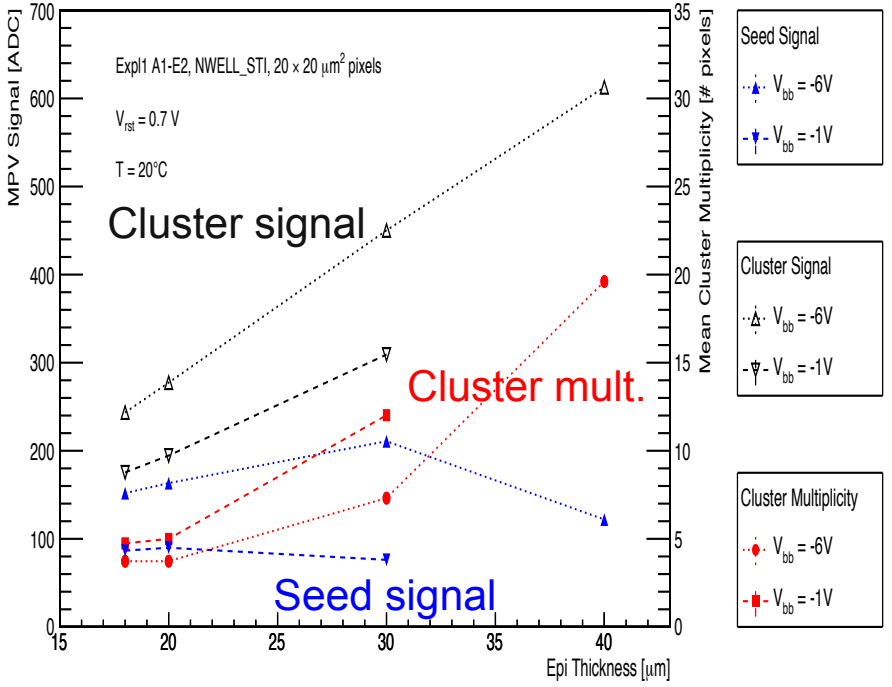




- Analogue, variable integration and readout time, 20 and 30 µm pitch
  - Study: charge collection, reverse bias, noise, epitaxial layer thickness
- Cluster charge increases linearly with the epi. layer thickness
- Optimum value of back bias depends on epi. layer thickness
  largest seed SNR: HR-30 for V_{bb} = −6 V, HR-20 for V_{bb} = −1 V

PIXEL CHIP R&D

Digital prototypes

ASTRAL/MISTRAL – MIMOSA22THR

- in-pixel pre-amplification and CDS circuitry
- parallel column readout and discriminators at end of column
- 22 × 33 μm^2 pixels
- … to validate upstream part of MISTRAL and most of ASTRAL readout

ALPIDE – pALPIDE

- in-pixel front-end
- binary readout
- in-matrix sparsification
- 22 μm pitch
- … for optimization of in-pixel front-end with binary readout and priority encoder

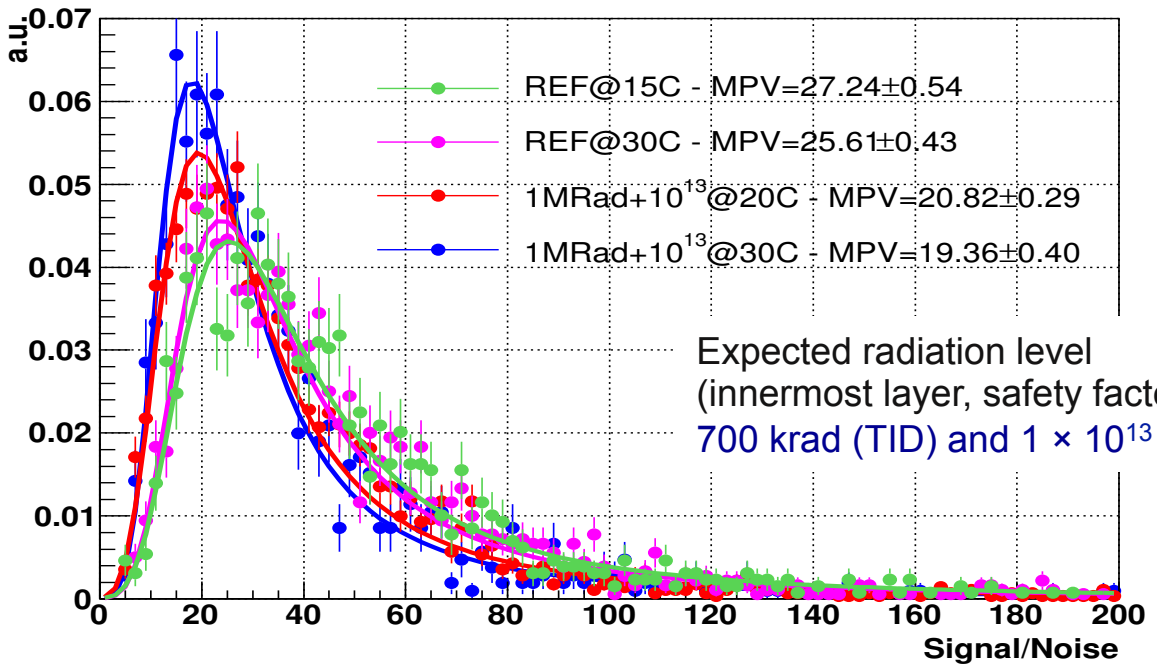
Achieved at the DESY test beam measurements (3 to 6 GeV *e*− and *e*+ beams):

- Detection efficiency: > 99 %
- Fake hit rate: ≈ 10^{-8}/(event×pixel)
- Spatial resolution ≈ 5 μm
- Performance of small scale digital prototypes complies with ALICE requirements

PIXEL CHIP R&D

ASTRAL / MISTRAL – MIMOSA-32ter, Radiation hardness

ALICE, CERN-LHCC-2013-024



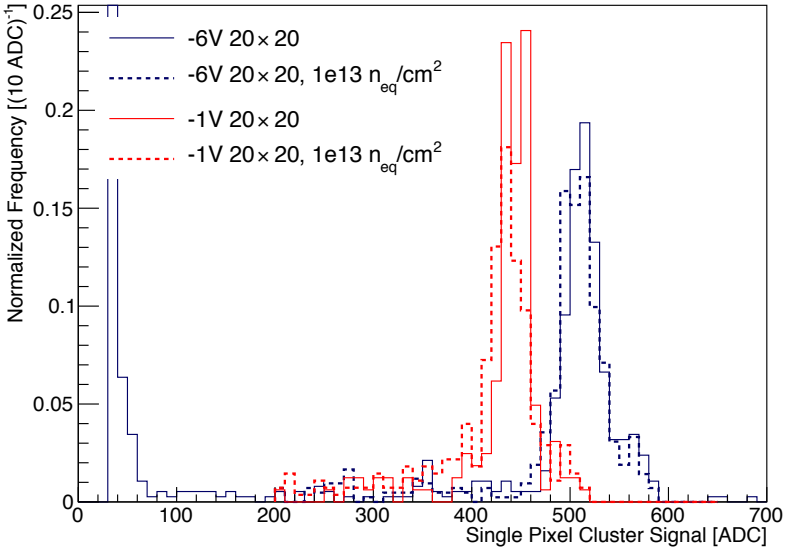
Expected radiation level
(innermost layer, safety factor 10):
700 krad (TID) and 1 × 10^{13} 1 MeV n_{eq} (NIEL)

Analogue, in-pixel pre-amplification and average noise subtraction
– in-pixel circuitry optimisation, radiation hardness

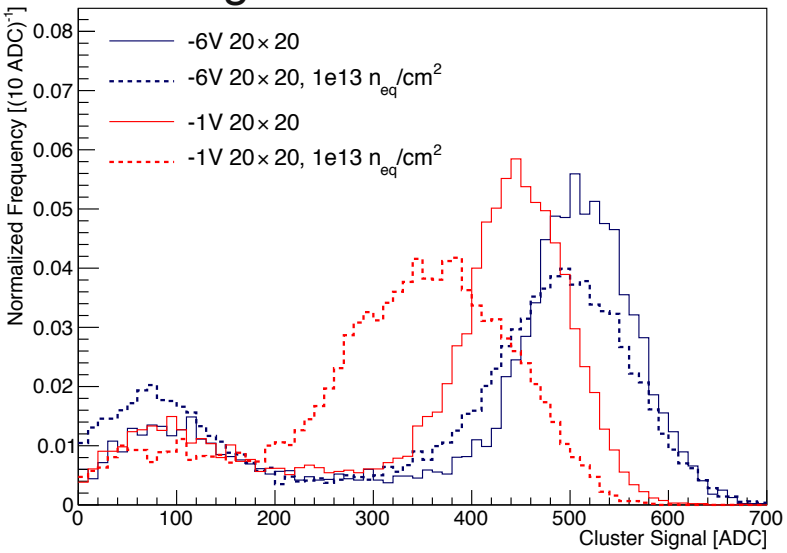
In-pixel circuitry is adequate for the expected radiation levels

PIXEL CHIP R&D

Explorer-0 radiation hardness



^{55}Fe signals



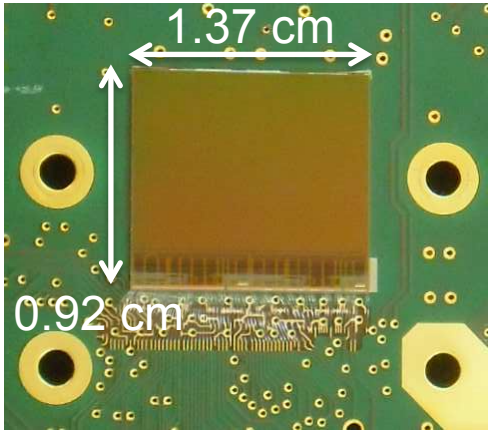
ALICE, CERN-LHCC-2013-024

Explorer 0 irradiated to 1x10^{13} 1MeV n_{eq} cm^{-2}

- 2 bias settings (-1V, -6V), N-well diode: 7.6 μm^2 with 1.04 μm spacing
- Single pixel cluster signal remains stable at a level of a few percent
- Noise increases by 5-15% (different pixel sizes and diode geometries)

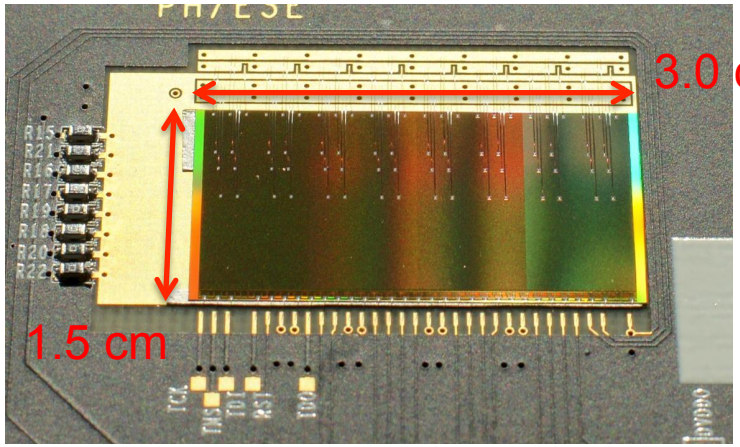
PIXEL CHIP R&D

Full scale prototypes



Chips received from foundry in late Q2/2014

Laboratory and beam-tests are on-going



MISTRAL FSBB (M0):

- 1.37 x 0.92 cm^2
- 416 * 416 pixels, 22 x 33 µm^2
- Double-row read-out at 160 MHz clock frequency
- On-chip 3-stage sparsification
- 2 versions fabricated, each with 2 slightly different sub-arrays

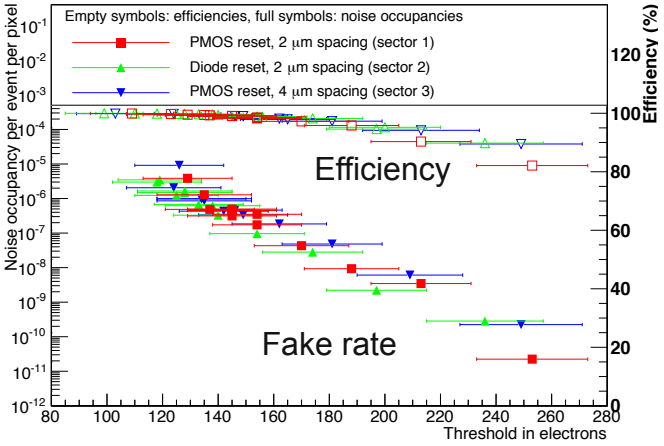
Full scale ALPIDE prototype chip:

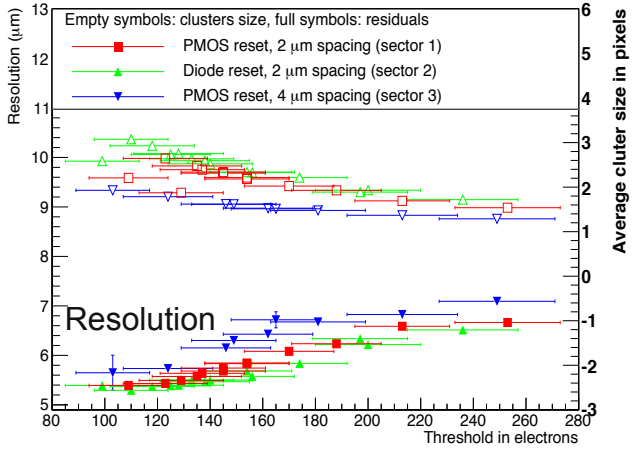
- 3 x 1.5 cm^2
- 1024 * 512 pixels, 28 x 28 µm^2
- In-pixel discriminator and sparse priority encoder readout
- Matrix divided into 4-sub sectors with different pixel types

FIRST RESULTS OF THE FULL SCALE PROTOTYPES

ALPIDE:

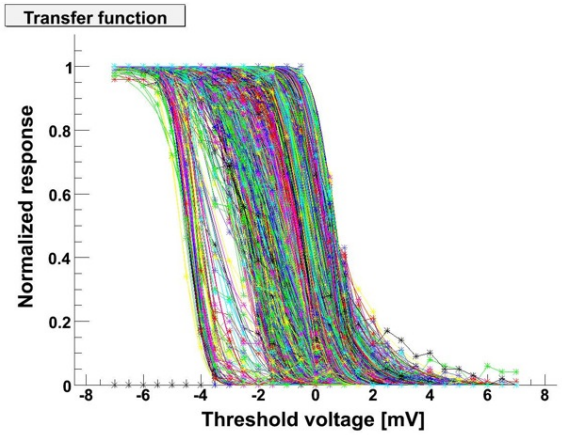
- Currently: test beam at CERN PS
- Efficiency close to 100% (first measured at BTF Frascati)
- Low fake hit rates
- ENC noise: 5-10 e, threshold RMS: 5-20 e
- Resolution ~ 5.5 µm, incl. 3 µm error on tracking
- Soon: back bias and irradiated results



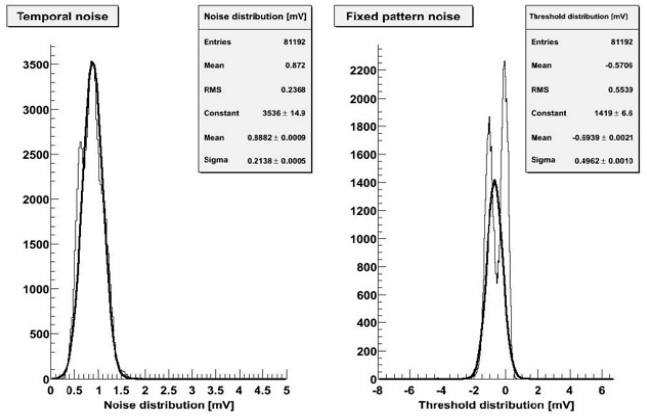


MISTRAL FSBB:

- Currently: lab. characterization
- Fabrication yield satisfactory
- Uniformity: similar chip-to-chip TN and FPN
- Test beam: CERN SPS in Oct 2014



Temporal noise (TN) Fixed Patter Noise (FPN)



SUMMARY

- The new ALICE ITS with 7 layers of monolithic silicon pixel detectors will be installed during LS2 of the LHC in 2018/19 completely replacing the present ITS

- Different architectures for the pixel chip have been explored
  - performance of small scale digital prototypes complies with requirements of pixel chip

- Full-scale prototypes are currently being characterized leading to a decision on the ALICE Pixel Chip architecture for the ITS Upgrade in the beginning of 2015