Low Resistance Strip Sensors & Slim Edges Combined RD50 Experiment

CNM (Barcelona), SCIPP (Santa Cruz), IFIC (Valencia)

Contact person: Miguel Ullán

Outline

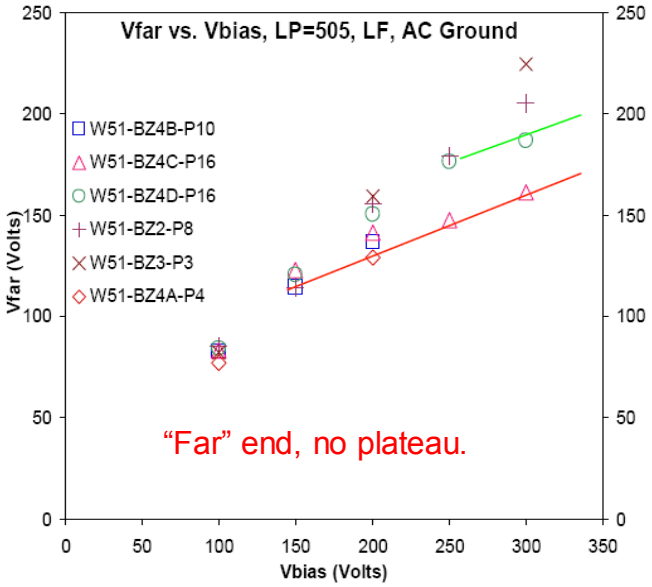
- Motivation
- Proposal
- Initial experiments
- PTP designs
- Final wafer design
- Slim edges experiment
- Status

Motivation

- In the scenario of a beam loss there is a large charge deposition in the sensor bulk and coupling capacitors can get damaged
- Punch-Through Protection (PTP) structures used at strip end to develop low impedance to the bias line and evacuate the charge

But…

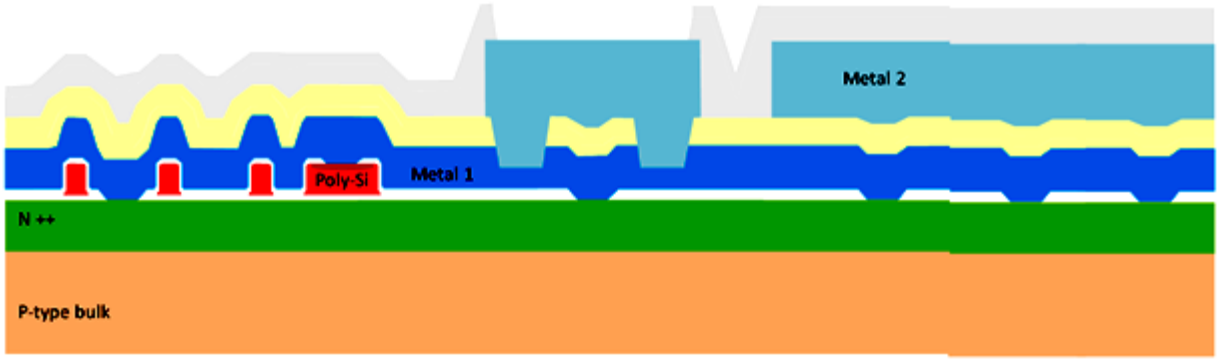
- Measurements with a large charge injected by a laser pulse showed that the strips can still be damaged
  - ➢ The **implant resistance** effectively isolates the "far" end of the strip from the PT structure leading to the large voltages

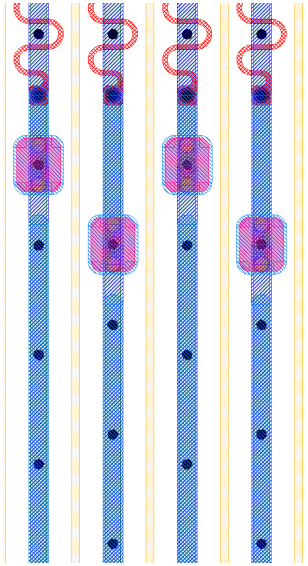


C. Betancourt, et al. "Updates on Punch-through Protection" ATLAS Upgrade week, Oxford, March 31, 2011.

Proposed solution

- To reduce the resistance of the strips on the silicon sensor.
- Not possible to increase implant doping to significantly lower the resistance. Solid solubility limit of the dopant in silicon + practical technological limits (~ 1 x 10^{20} cm^{-3})
- Alternative: deposition of Aluminum on top of the implant:
  - $R_{\square}(Al) \sim 0.04\,\Omega/\square \Rightarrow 20\,\Omega/cm$





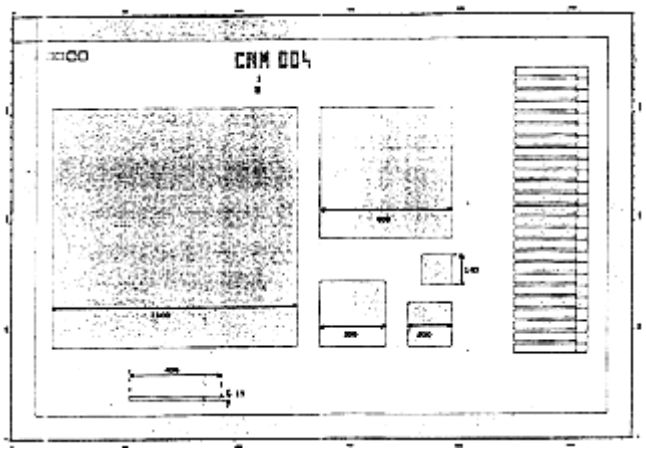
Metal on implant

- Metal layer deposition on top of the implant before the coupling capacitance is defined.
  - Double-metal processing to form the coupling capacitor
  - A layer of high-quality dielectric.
    - Deposited on top of the first Aluminum (not grown)
    - Low temperature processing (not to degrade Al: T < 400 ºC)
- MIM capacitors
  - Low temperature deposited isolation
    - PECVD (300-400 ºC)
    - Risk of pinholes (Yield, Breakdown)
    - > 20 pF/cm ➔ ~ 3000 Å
- Experiments performed at CNM to optimize the MIM cap.

Initial experiments

- 6 wafers batch of MIM capacitors
  - Different sizes
    - C1: 1100 x 1100 μm^2 = 1.20 mm^2
    - C2: 600 x 600 μm^2 = 0.36 mm^2
    - C3: 300 x 300 μm^2 = 0.09 mm^2
    - …

    (short strips ~ 0.5 mm^2)



- Low-temperature deposited isolation
  - PECVD (300-400 ºC). 3 technological options:
    - Op1: 3000 Å of SiH_4-based silicon oxide (SiO_2) deposited in 2 steps ("Silane")
    - Op2: 3000 Å of TEOS-based oxide deposited in 2 steps ("Tetra-Etil Orto-Silicate")
    - Op3: 1200 Å + 1200 Å + 1200 Å of TEOS-based ox. + Si_3N_4 + SiH_4-based ox.
  - Use of a multi-layer to avoid pinholes

MIM results

- All 3 options give good MIM capacitors
- Yield for the largest caps (> 1 mm^2). Best for nitride

%	Silane	TEOS	Nitride
C1	81%	86%	94%

- I_{LEAK} < 3 pA @ 20 V for the largest cap (C1) in all options
- Capacitance (pF/mm^2, pF/cm)

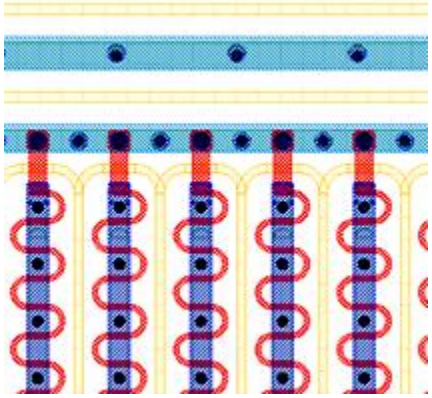
C1	Silane	TEOS	Nitride
pF/mm2	122	119.4	110.3
pF/cm	24.4	23.9	22.1

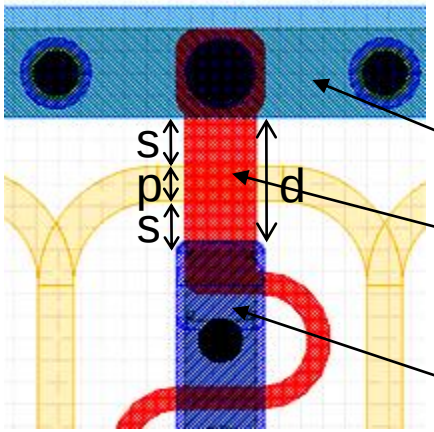
- Breakdown Voltage (V)

V	Silane	TEOS	Nitride
C1	158	154	215

PTP design

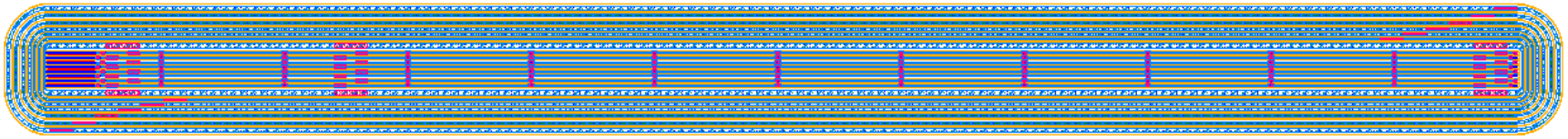
- Reduce implant distance to bias ring to favor punch-through effect at low voltages
  - Not tried before at CNM
  - Very dependent on surface effects (difficult to simulate)
- Poly resistor between the implant and bias rail ("transistor effect").
- Compromise between PT effect and early breakdown
- Design of experiments varying p, s $\Rightarrow$ d

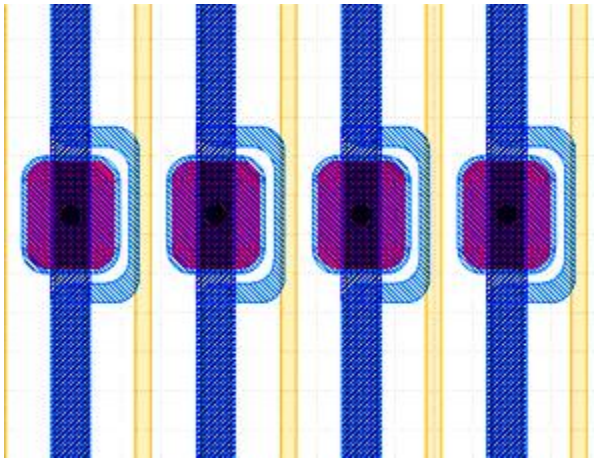




Test structures

- Test structure to measure potential along the implant under laser injection



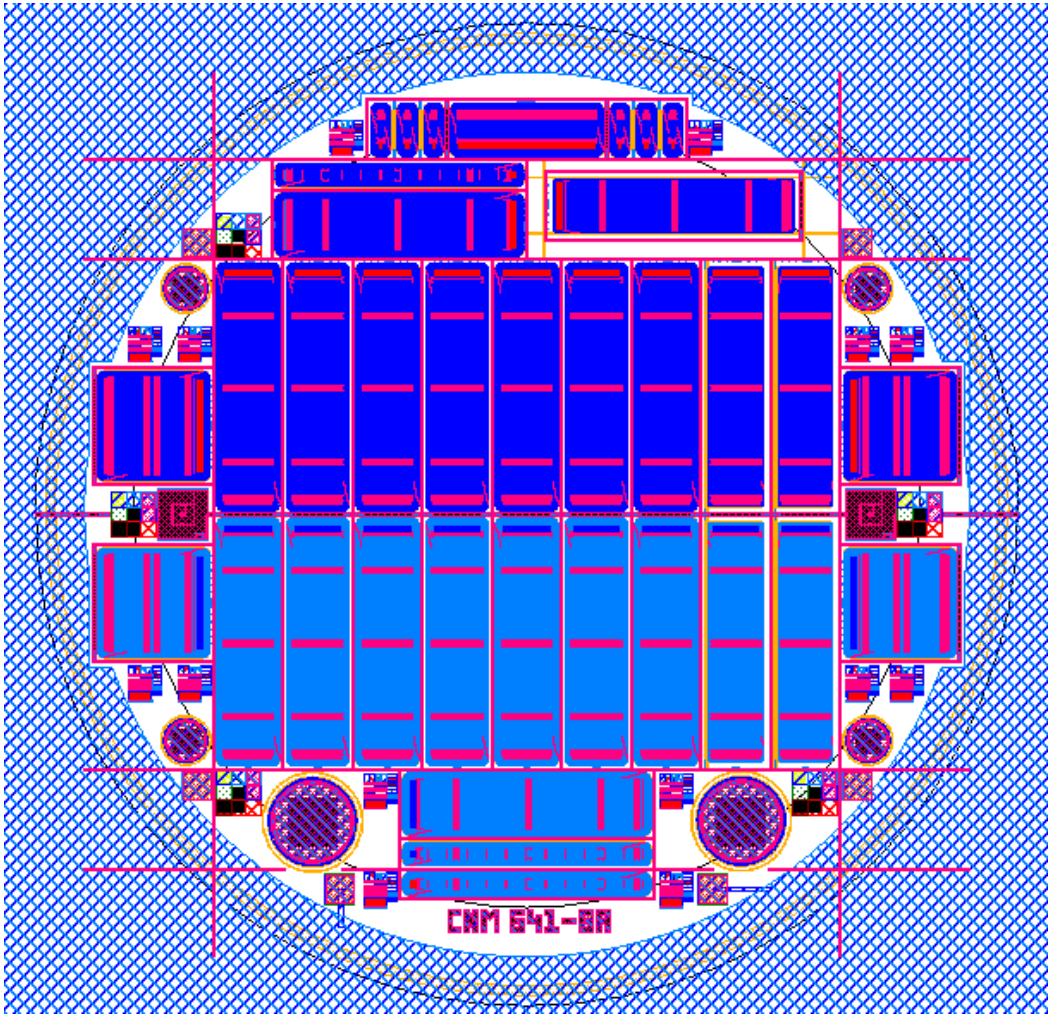


- Test structures for more precise optimization of PTP geometry

Final wafer design

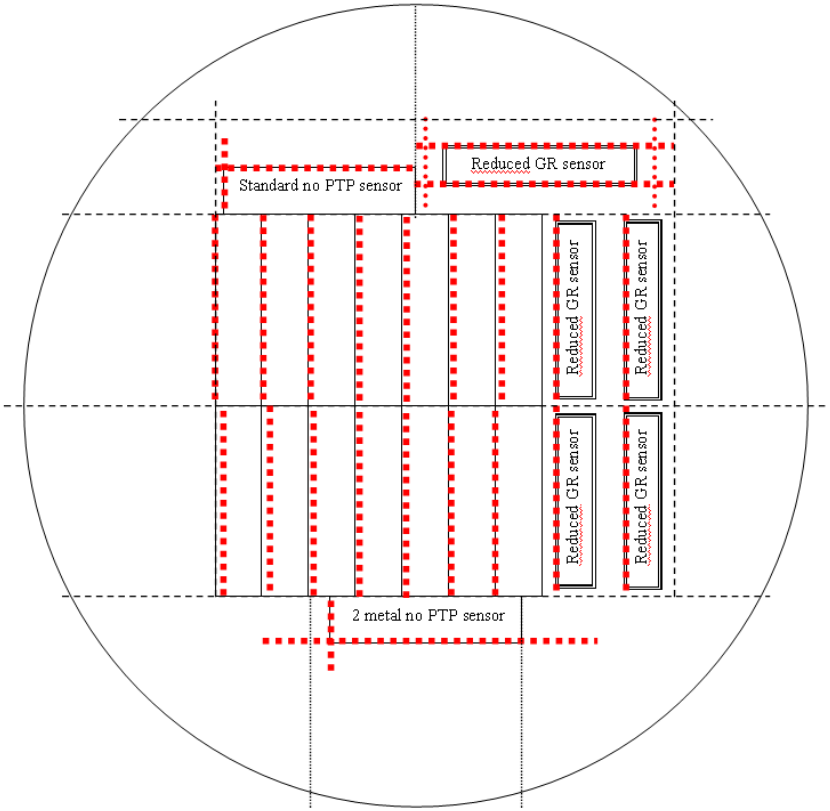
- 10 mini ATLAS-barrel-like sensors
  - 64 channels, ~2.3 mm long strips
  - With a metal strip on top of the implant and connected to it to reduce R_{strip}
  - Each sensor with a different PTP geometry (with poly bridge)
- 10 extra standard sensors for reference (no metal in implant)
  - Identical to the ones above but without metal strip
- Extra test structures
  - Precise PTP optimization (+DoE)
  - Accurate measurement of potential grading along the strip
- Deep trenches designed at different distances from bias ring to experiment on slim edges
- Some extra designs to try full 4-edges cutting of sensors with deep trenches

Final wafer design



Slim Edges experiment

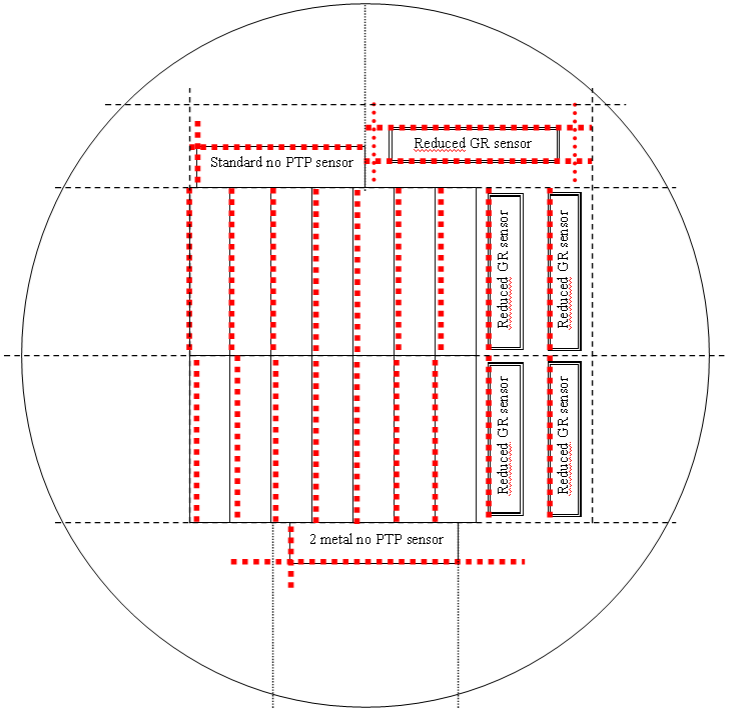
- 3 extra wafers in the batch for Slim Edges experiment
- New mask designed for Aluminum removal in the back side to act as mask for DRIE
- Si deep etch from the back
- Trenches 30 um wide and:
  - Opt 1: 10 μm deep etch
  - Opt 2: ~250-280 μm deep etch
  - Opt 3: XeF_2 etch at NRL
- ALD deposition of Al_2O_3 after etching to passivate surface

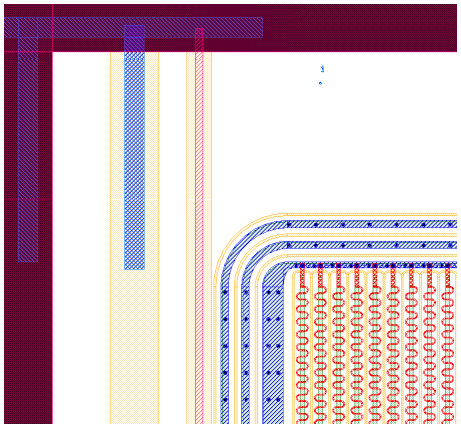


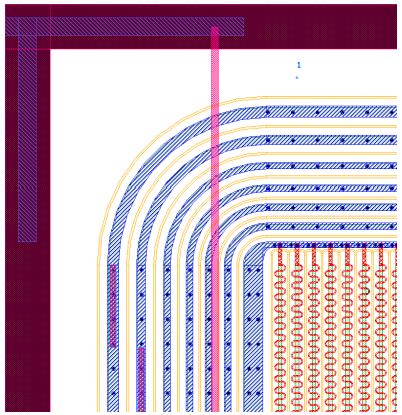
Trench design

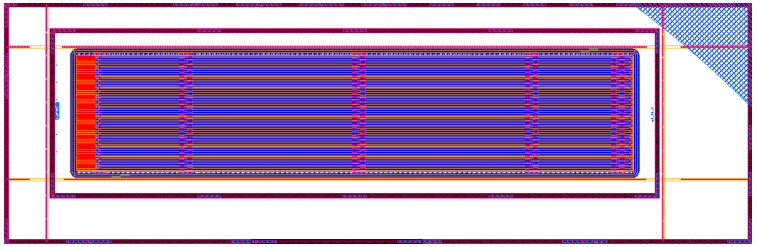
Several trench experiments:

- 2 guard rings sensors and trench cut close to the las GR
- Cut at different GR
- 2 sides cut
- 4 sides cut









Status

- LowRstrip wafer design finished
- 1 additional mask designed for deep trenches for Slim edges experiments
- Masks fabricated
- Run just started in CNM clean room

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- Ready to bill RD50 for the funding (15000 €)
  - ➢ order pending, quotation to be issued by CNM
- Pending agreement with Slim Edges Common Project to contribute for the extra costs for 3 extra wafers with deep trenches and Al_2O_3 passivation

Thank you