

Test beam measurements of CNM 3D pixel detectors

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CNM -IFAE

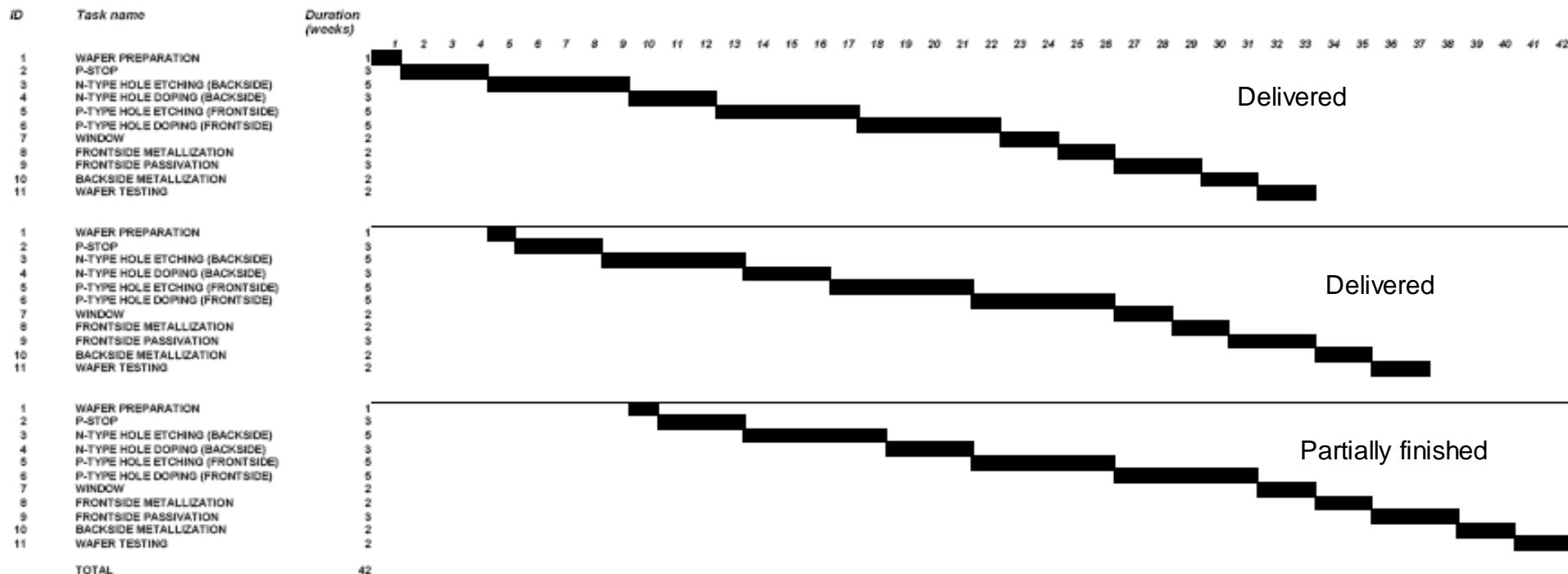


1. 3D detector technology at IMB-CNM
2. CMS mask description
3. Fabrication overview
4. Electrical measurements
5. Future work



Status of production run

Worplan for 3d double side detectors (p-type) - 3 batches of 24 wafers



Total A: 171
 Total B: 17
 Total C: 100

+ back up

Overall yield: 60%

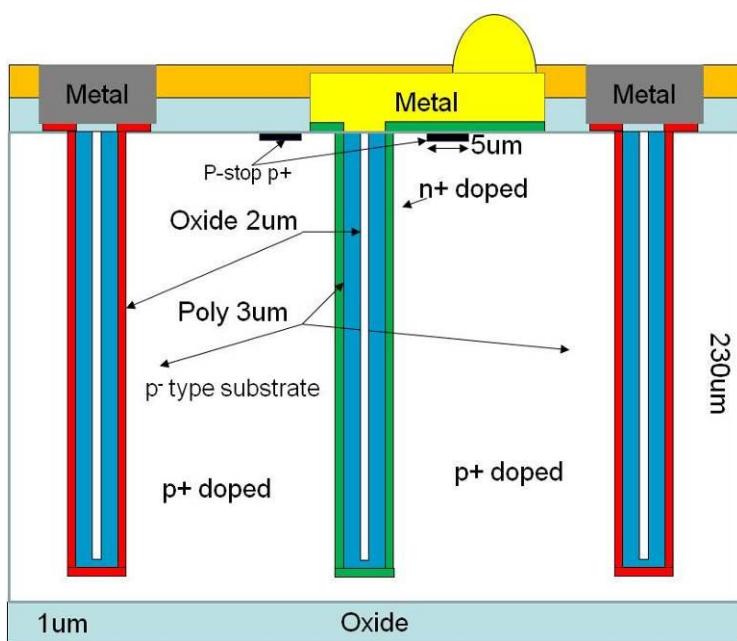


Technologies

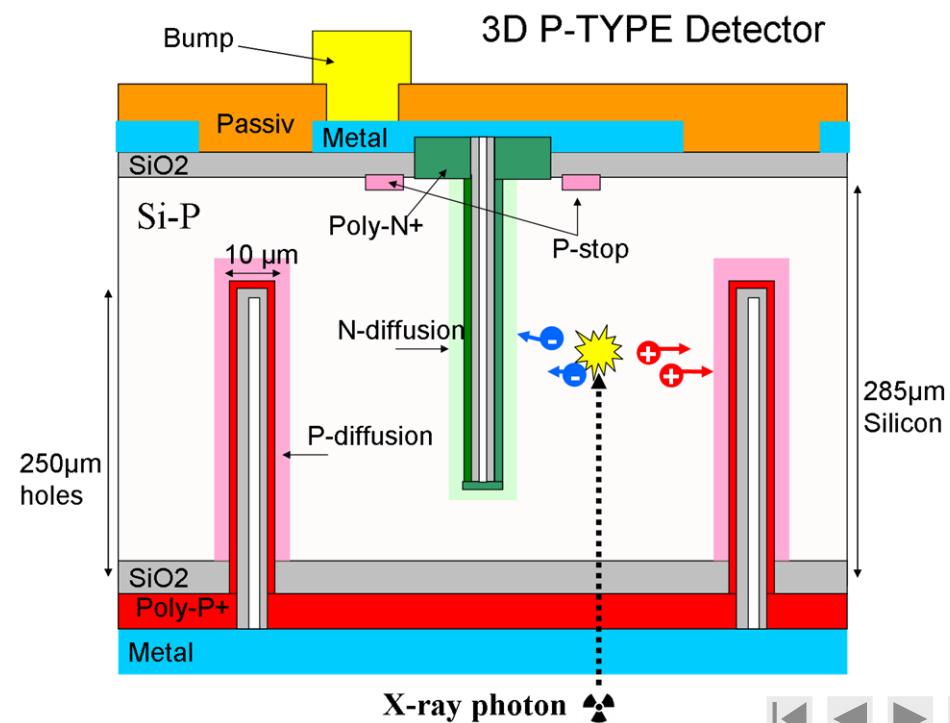
- Array of electrode columns passing through substrate
- Electrode spacing << wafer thickness (e.g. from $10\mu\text{m}$ to $>300\mu\text{m}$)

CNM-IMB has developed both technologies

Single sided



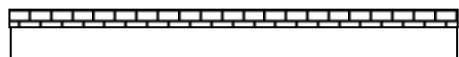
Double sided 3D



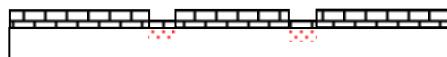
Standard 3D process on p-type wafers

Few years of technology development: double sided

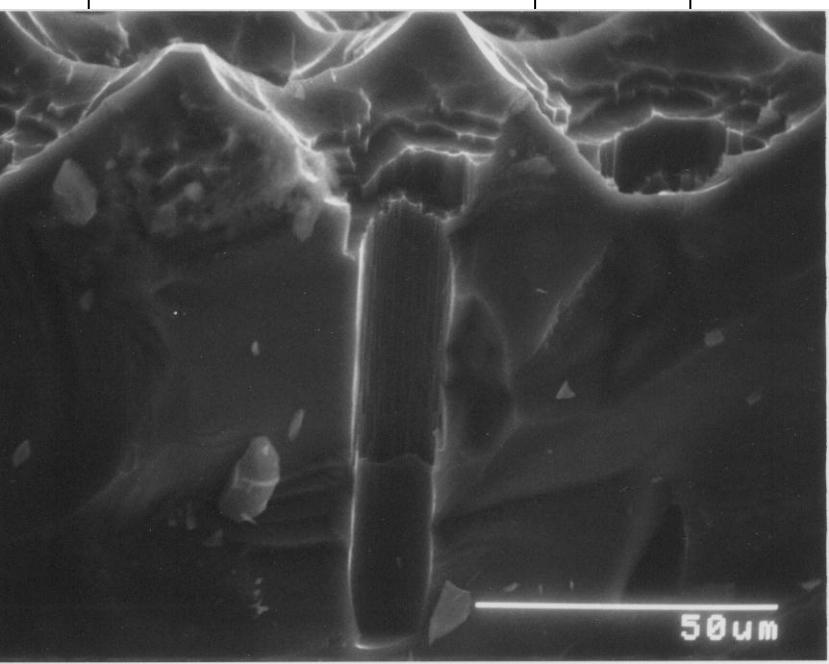
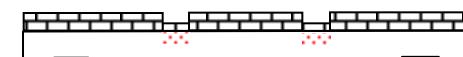
1- wafer preparation



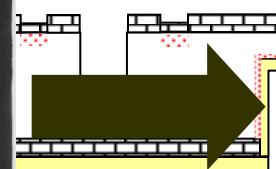
2- p-stop definition



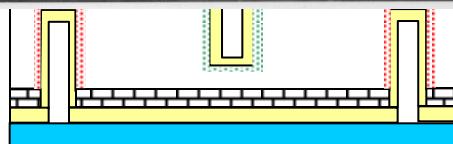
3- holes etching, backside



s etching, front

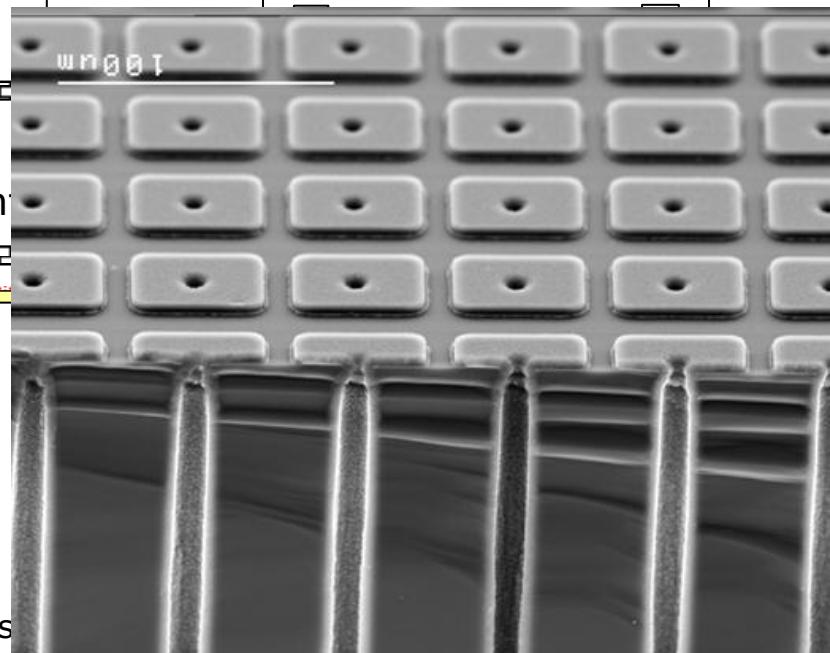


In a nutshell:
levels (9 with back s



passivation,

- Double side process
- Holes: 220-250um deep – Ø 10um
- TEOS oxide passivation
- SiO₂/Si₃N₄ final passivation (front side and backside)

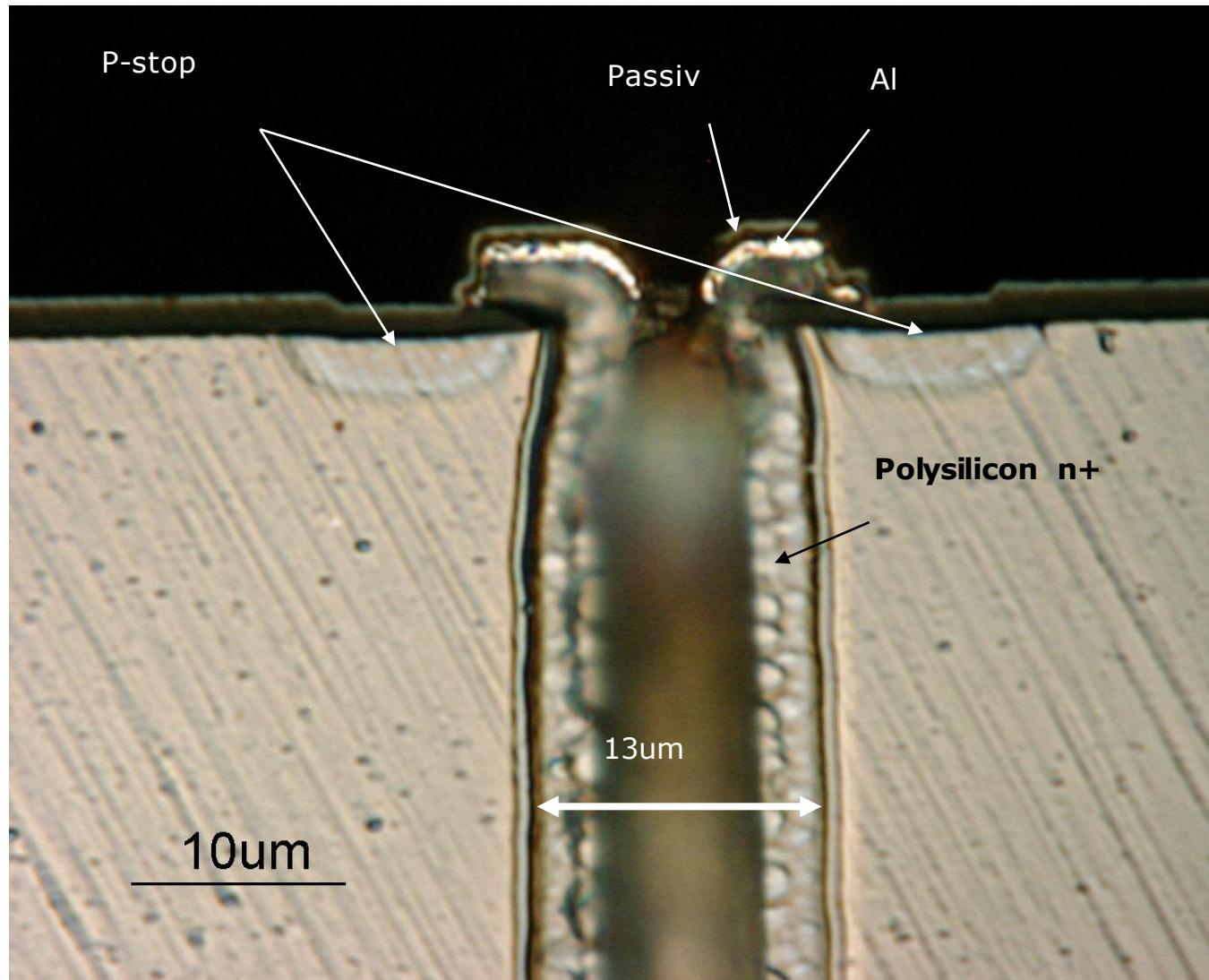


Legend:

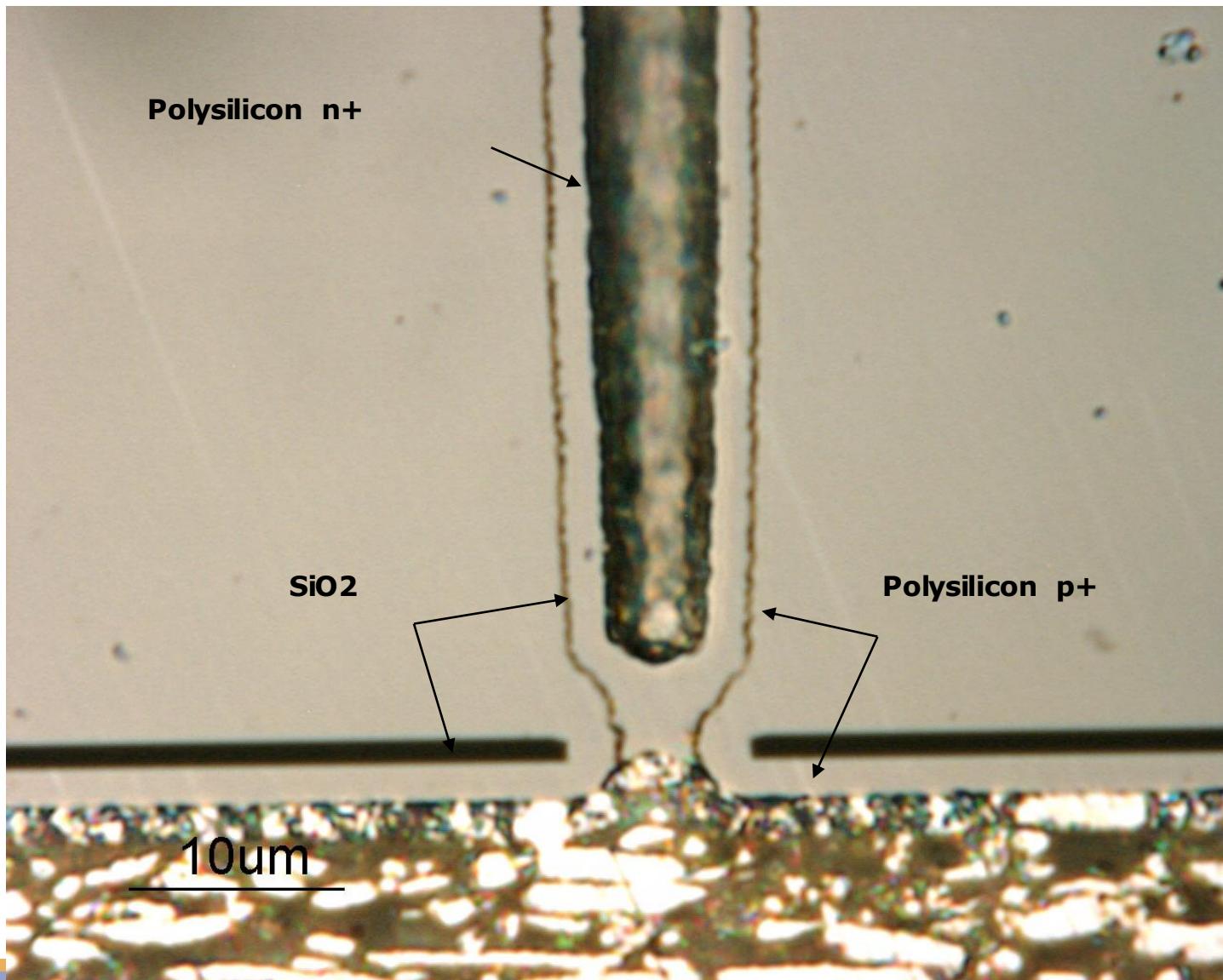
- : Si p⁺
- : Polysilicon
- : Si n⁺
- : Passivation
- : Oxide



Cross section



P-type holes

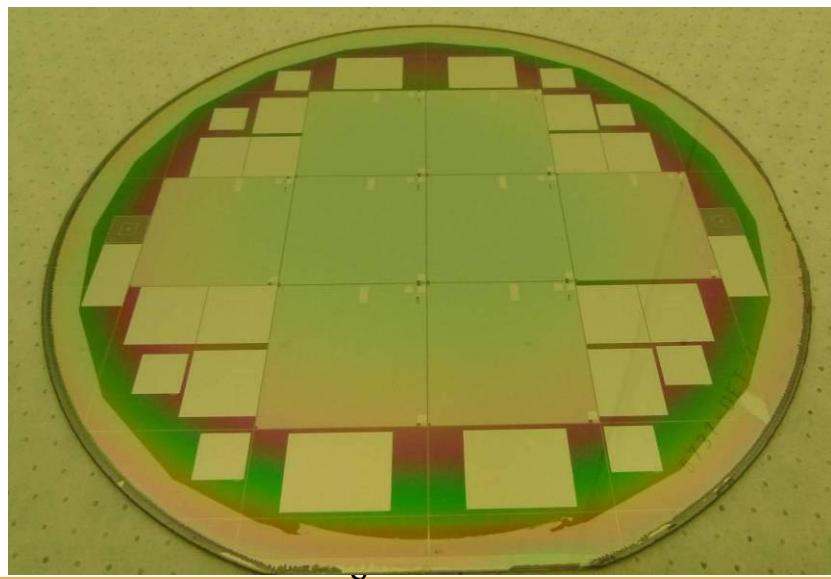
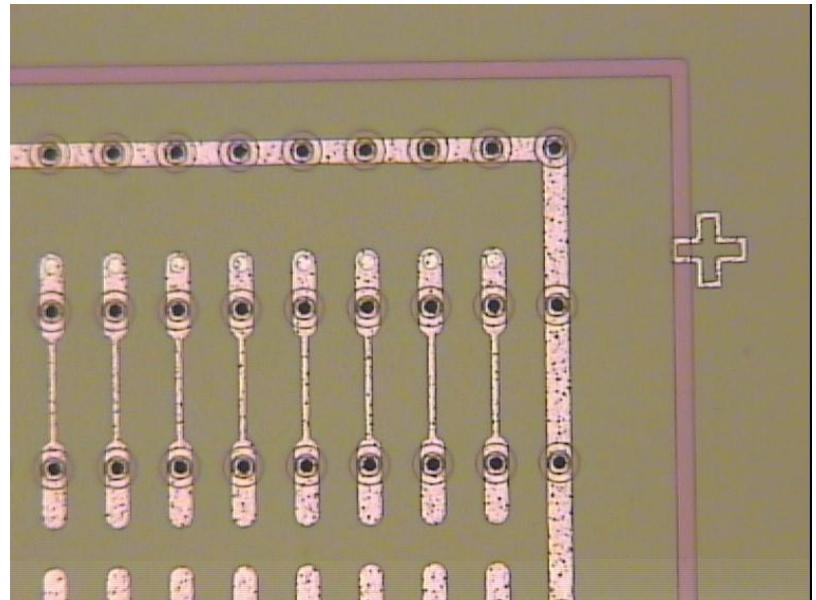


3D FE-I4 Atlas pixels for IBL

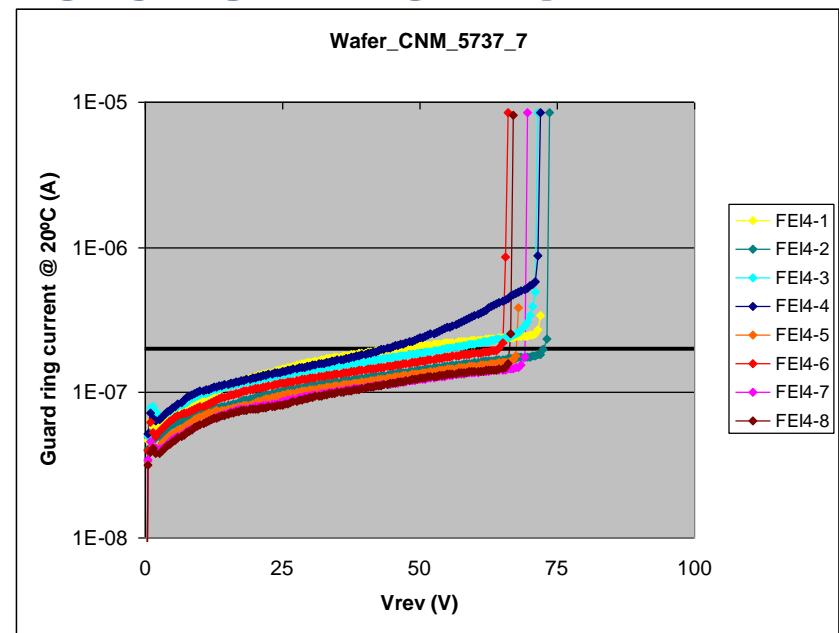
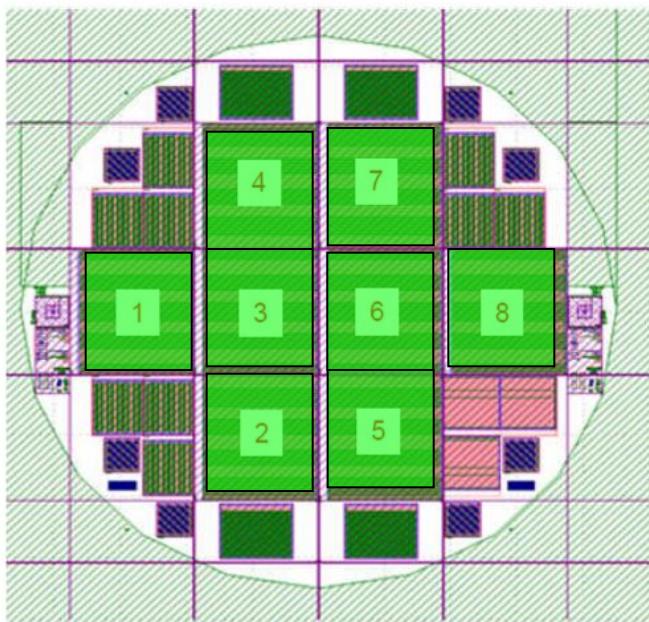
Atlas pixels, FE-I3 and new FE-I4 fabrication and irradiation for Insertable B-Layer and testbeam. In the framework of the Atlas 3D collaboration (<http://test-3dsensor.web.cern.ch/test-3dsensor/>).

Common layout designed in the framework Atlas 3D collaboration (CNM, FBK, SINTEF, Stanford). New FE-I4 design ($2 \times 2 \text{ cm}^2$).

Qualification run finished and tested
Production runs tested and processed at IZM. Ready for flip chip.



Electrical characterization



	Class	GR current @ 25 V (nA)	I(25V) / I(20V)	Breakdown V (V)
S1	A	145.18	1.13	71
S2	A	102.12	1.10	72
S3	A	132.70	1.09	69
S4	A	139.88	1.10	71
S5	A	96.12	1.14	67
S6	A	116.11	1.09	65
S7	A	86.76	1.09	69
S8	A	82.57	1.07	66

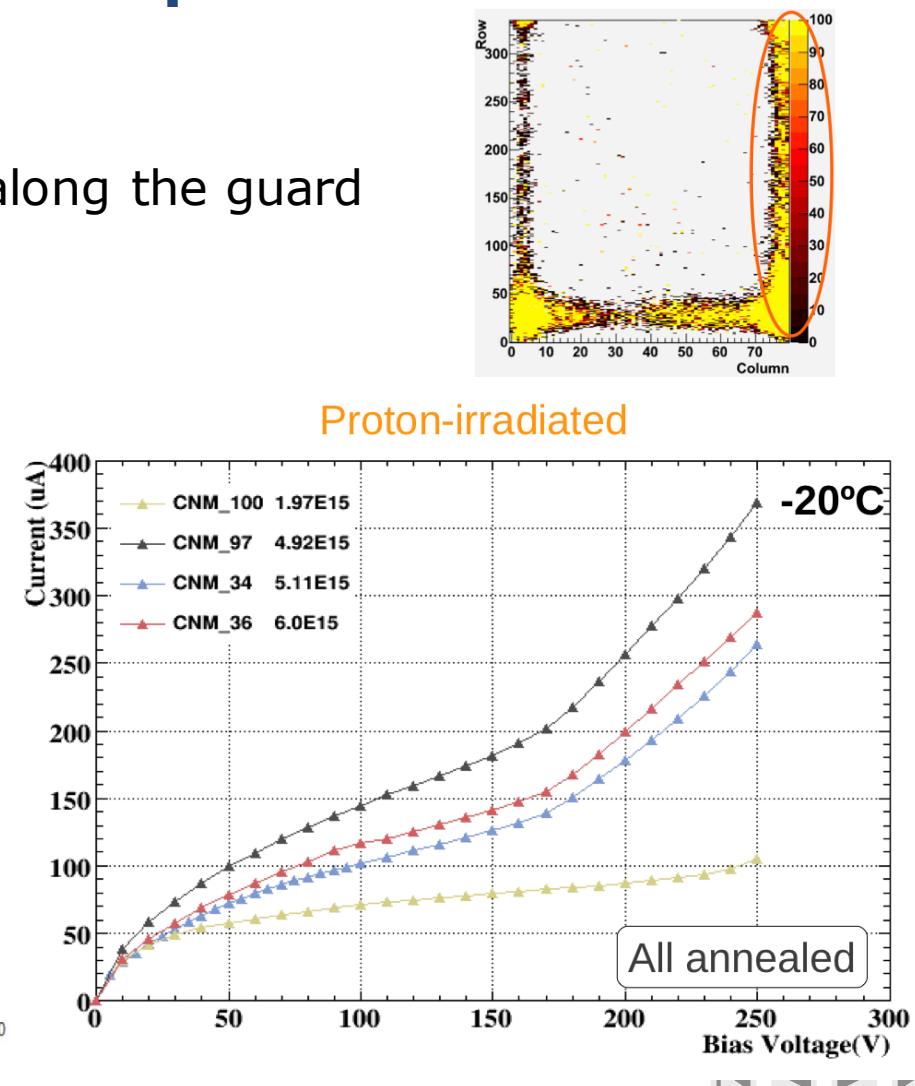
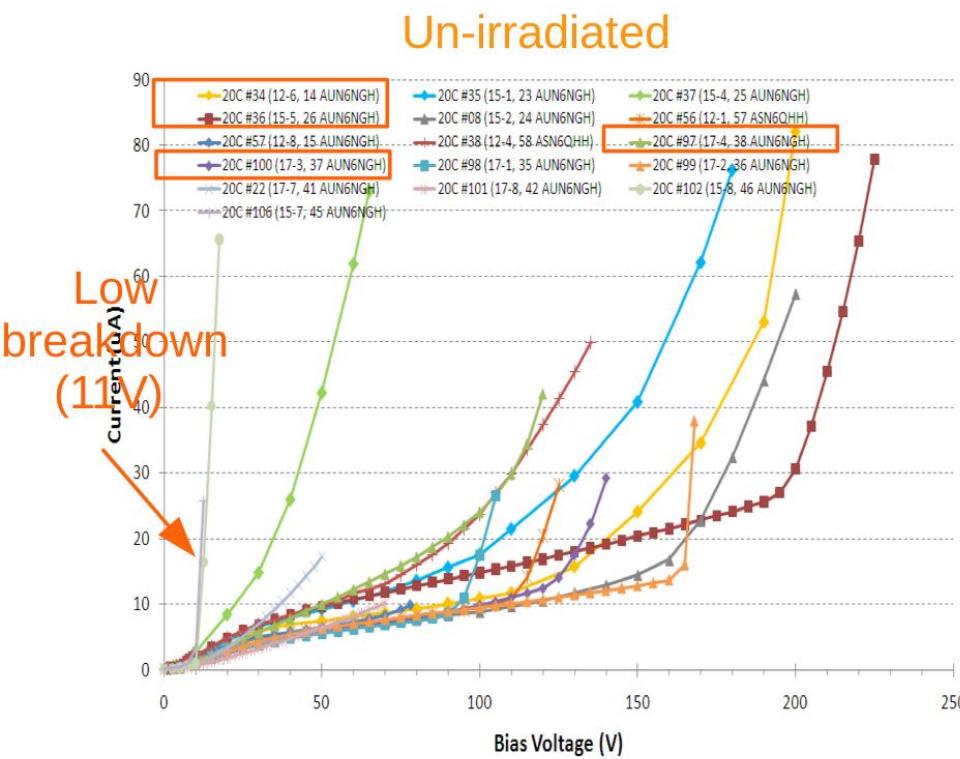
Bow: 60.8μm

class A detectors: 8
class B detectors: 0
class C detectors: 0



Characterization of p-irradiated devices

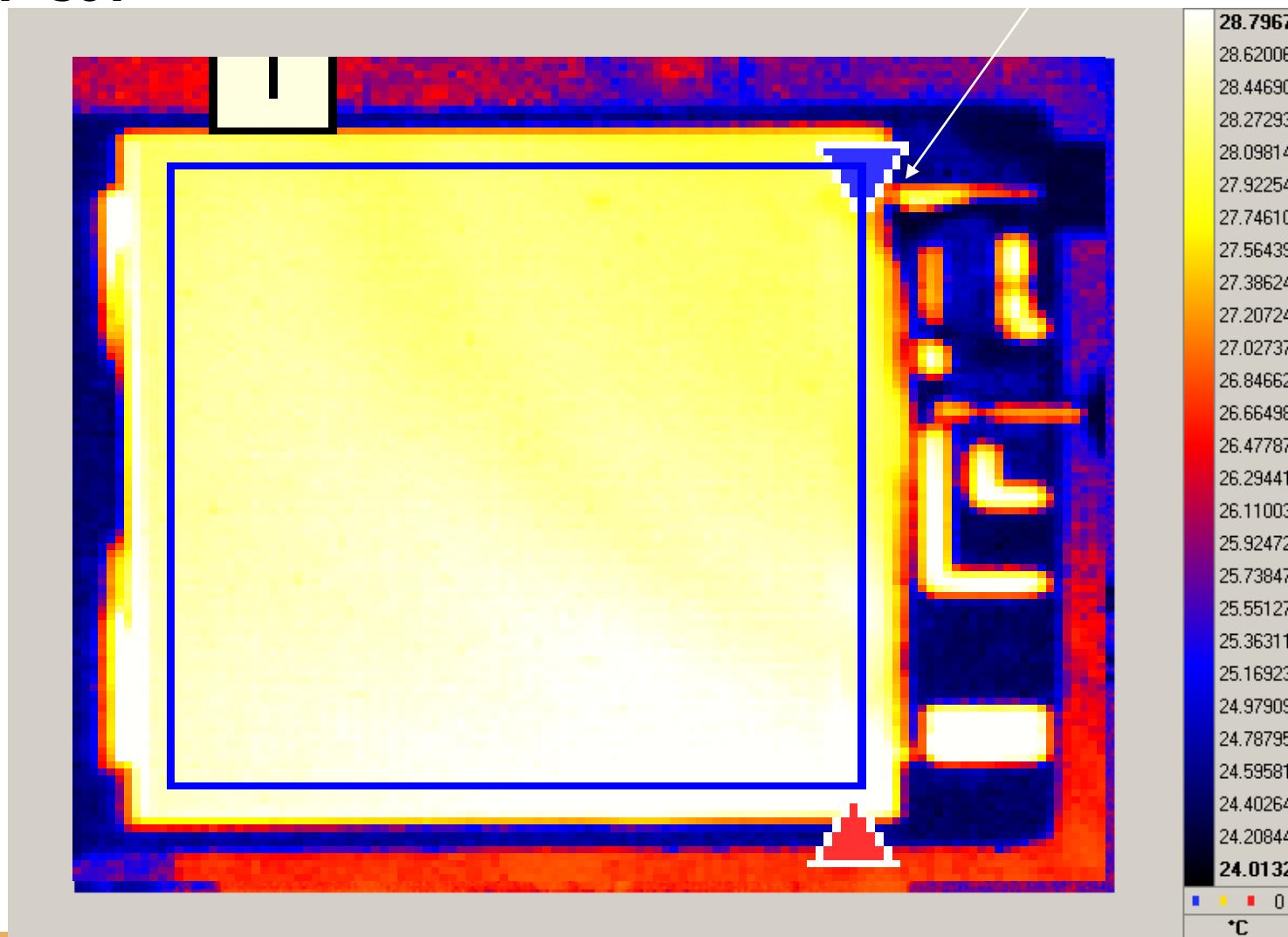
- Leakage current of CNM devices is along the guard ring



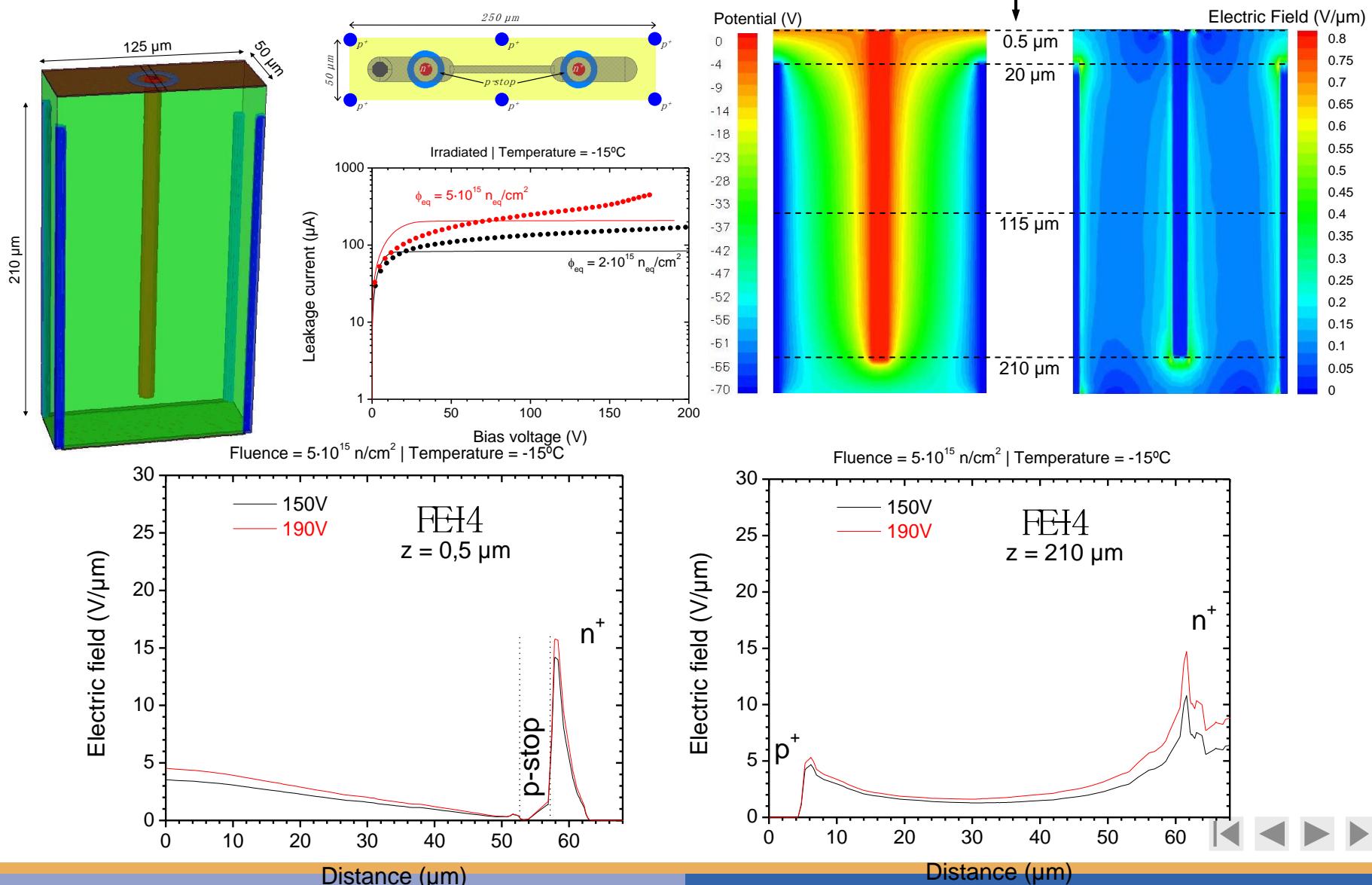
Thermal Image

V=50V

Wire bond

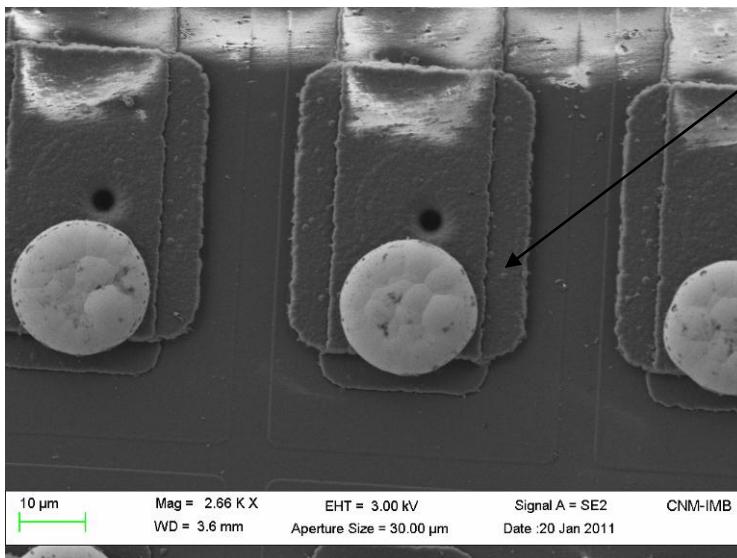


Simulation



UBM deposition

For IBL the UBM is deposited on all wafers at IZM in Germany before the flip chip.

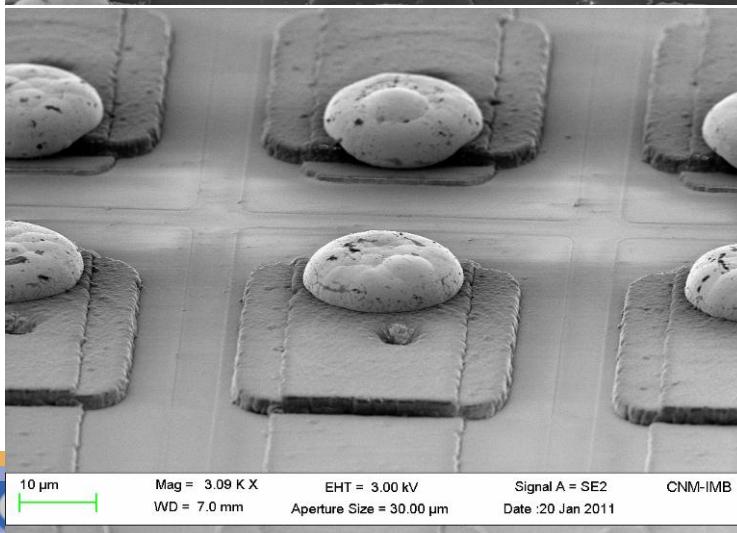


Under bump metallization

CMN and IFAE have developed the technology for UBM deposition Ni/Au and Cu and the flip chip process with SnPb and SnAg bumps.

FE-I3 detectors already bonded.

FE-I4 only dummies bonded.



Electroplating for 50μm-pitch

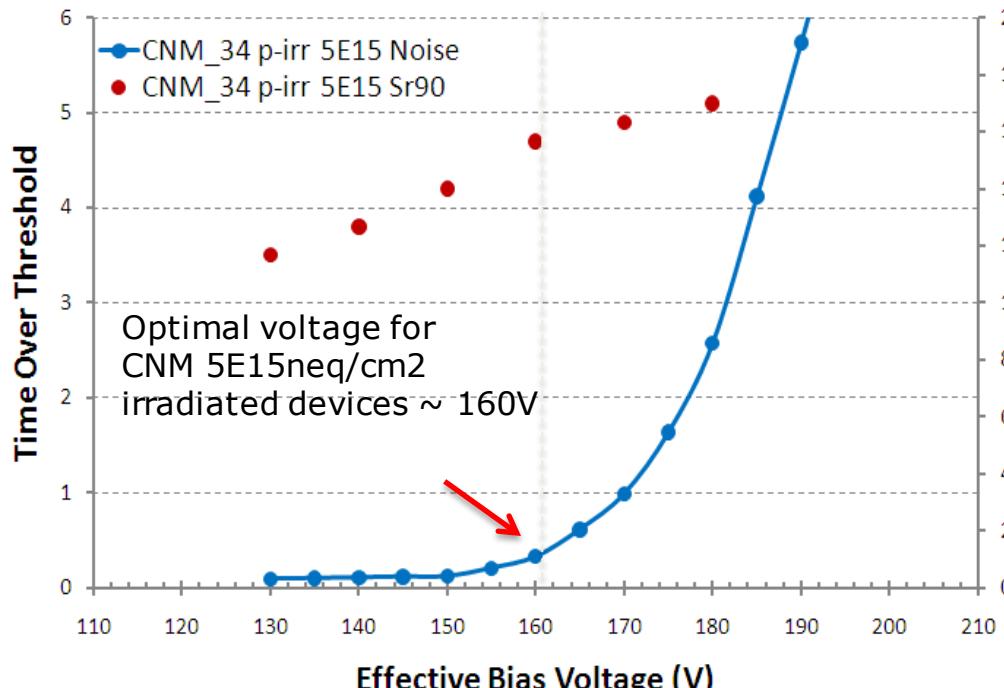
Indium: Under development: FlipChip

Flip chip machine: FC150

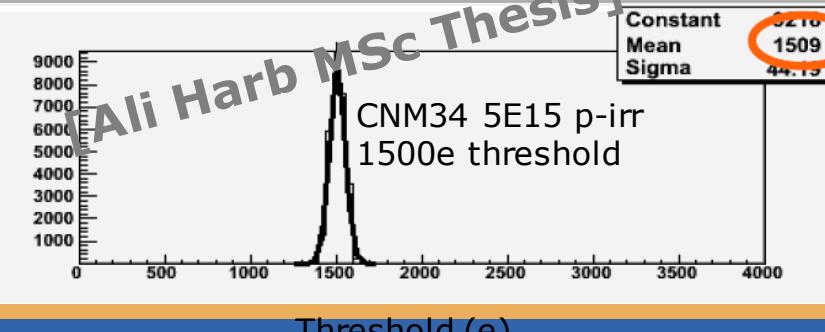
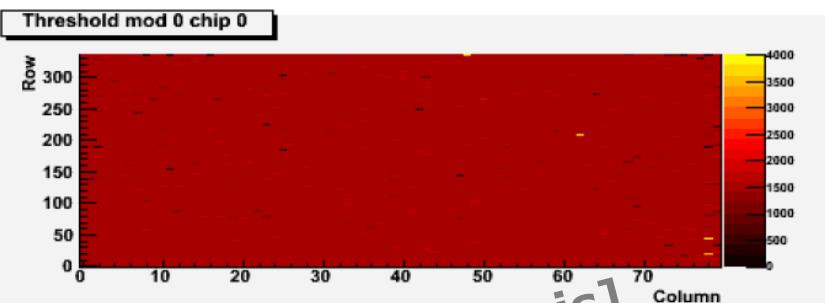
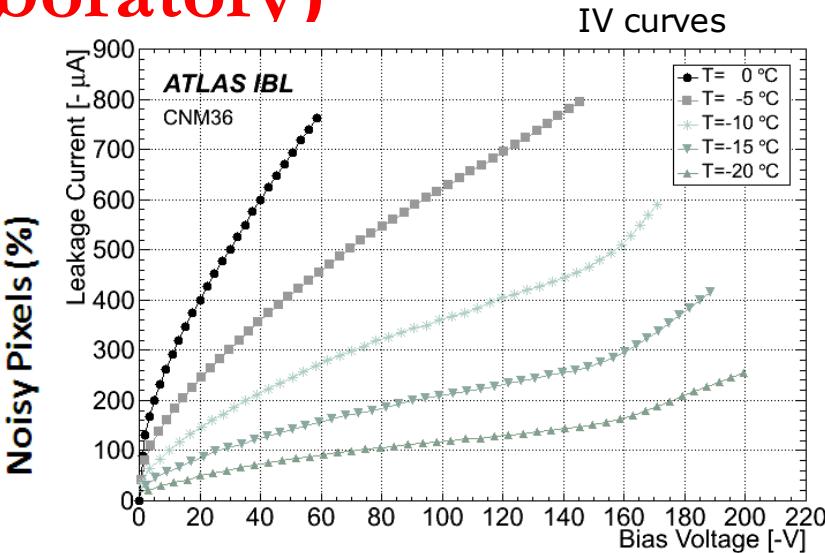
Bump reflow: ATV SRO702



Device Performance (Laboratory)

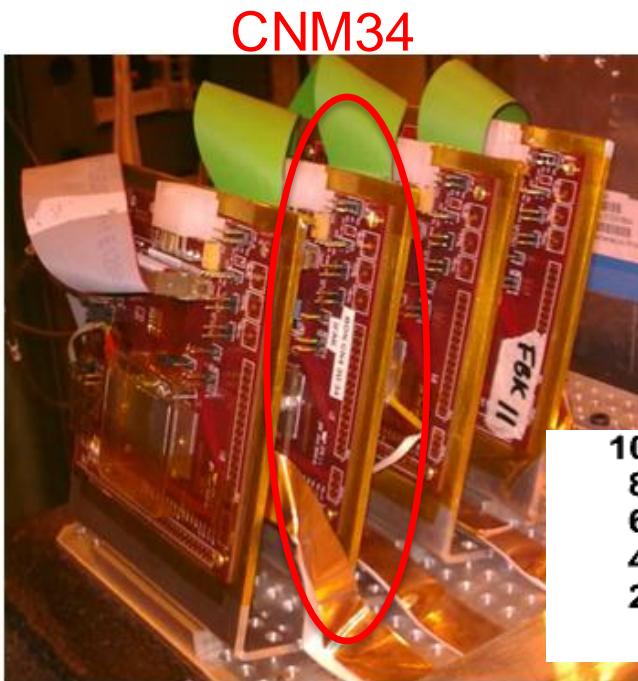


S. Grinstein
<http://dx.doi.org/10.1016/j.nima.2012.03.043>



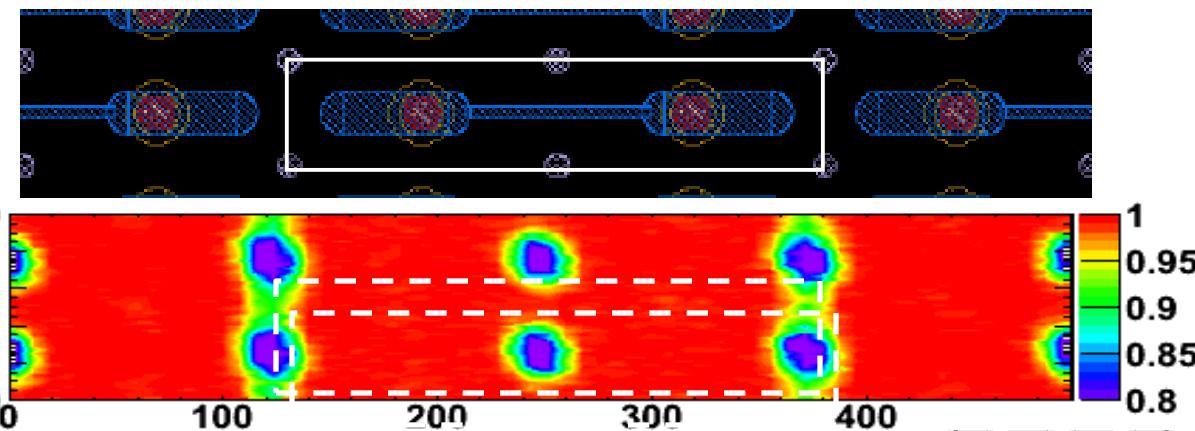
Device Performance (Testbeam)

- Test beam measurements **critical** to study performance of devices
 - ✓ **Efficiency** and position resolution
- Several test-beam periods carried out (DESY, CERN), and different devices tested
 - ✧ p-irr: CNM34, CNM97, CNM36
 - ✧ n-irr: CNM81 and CNM82



CNM81: n-irradiated $5\text{E}15\text{neq}/\text{cm}^2$,
0deg incidence
HV=160V

eff=97.5%



<http://dx.doi.org/10.1016/j.nima.2012.03.043>

Slim edges

Reduce the dead area at the detector edges. **Laser-Scribing and Al₂O₃**

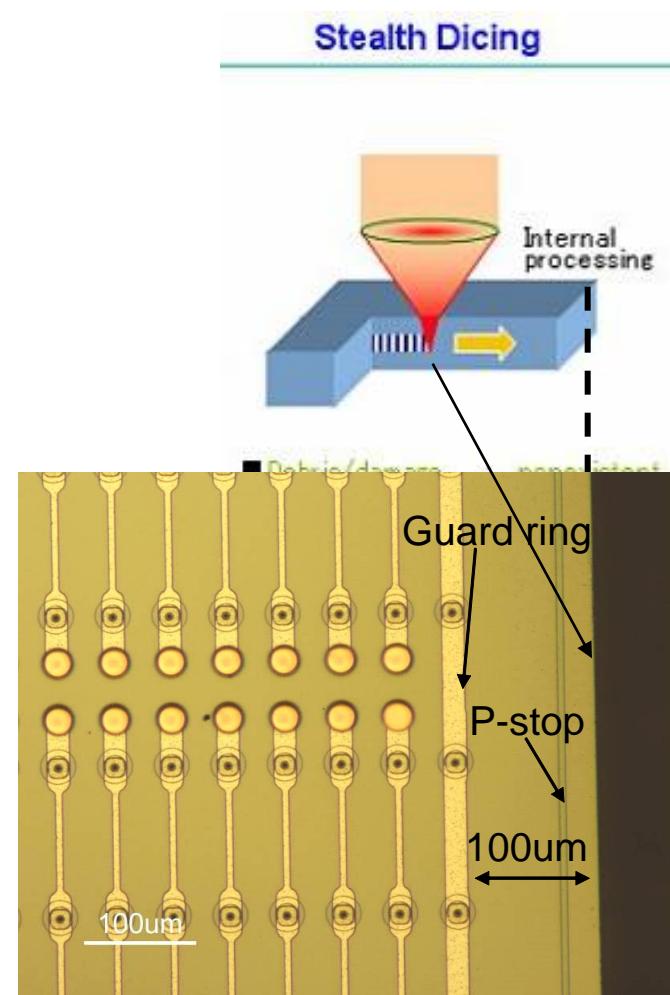
Sidewall Passivation of P-Type

Sensors : (M. Christophersen's)

Negative charges induced by Al₂O₃ deposited by ALD process, isolate the sidewall surface cut in p-type wafers reducing surface current.

First 3D FE-I3 pixels already bump bonded at CNM and waiting for pcb wire bonding and testing at IFAE.

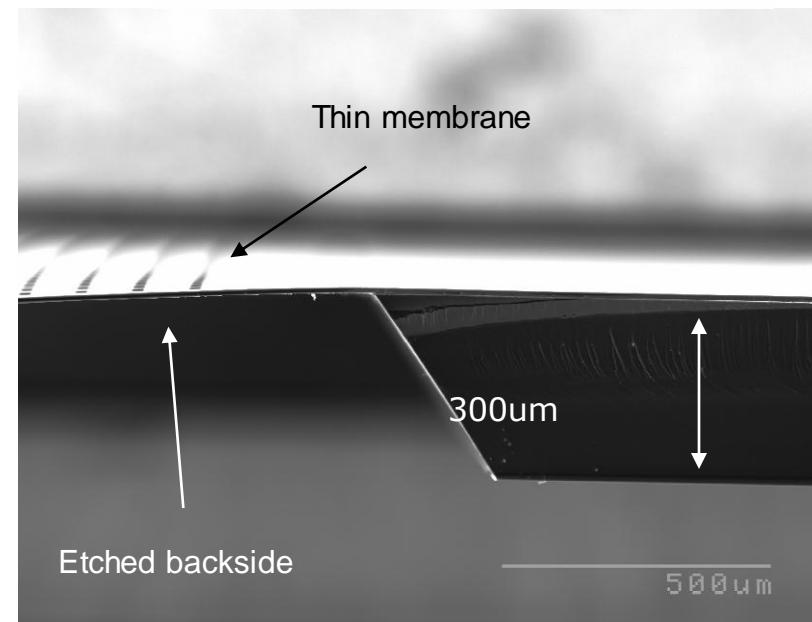
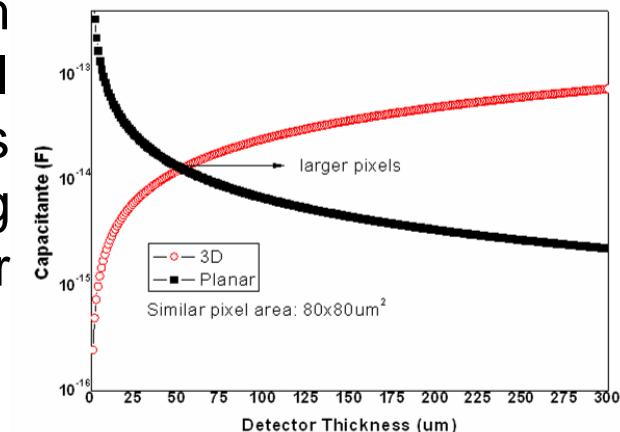
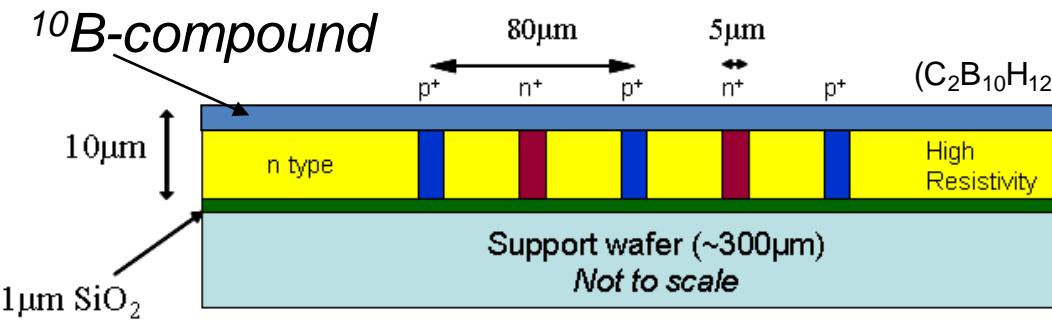
2 more wafers with FE-I4 have been sent to be diced and passivated at NRL.



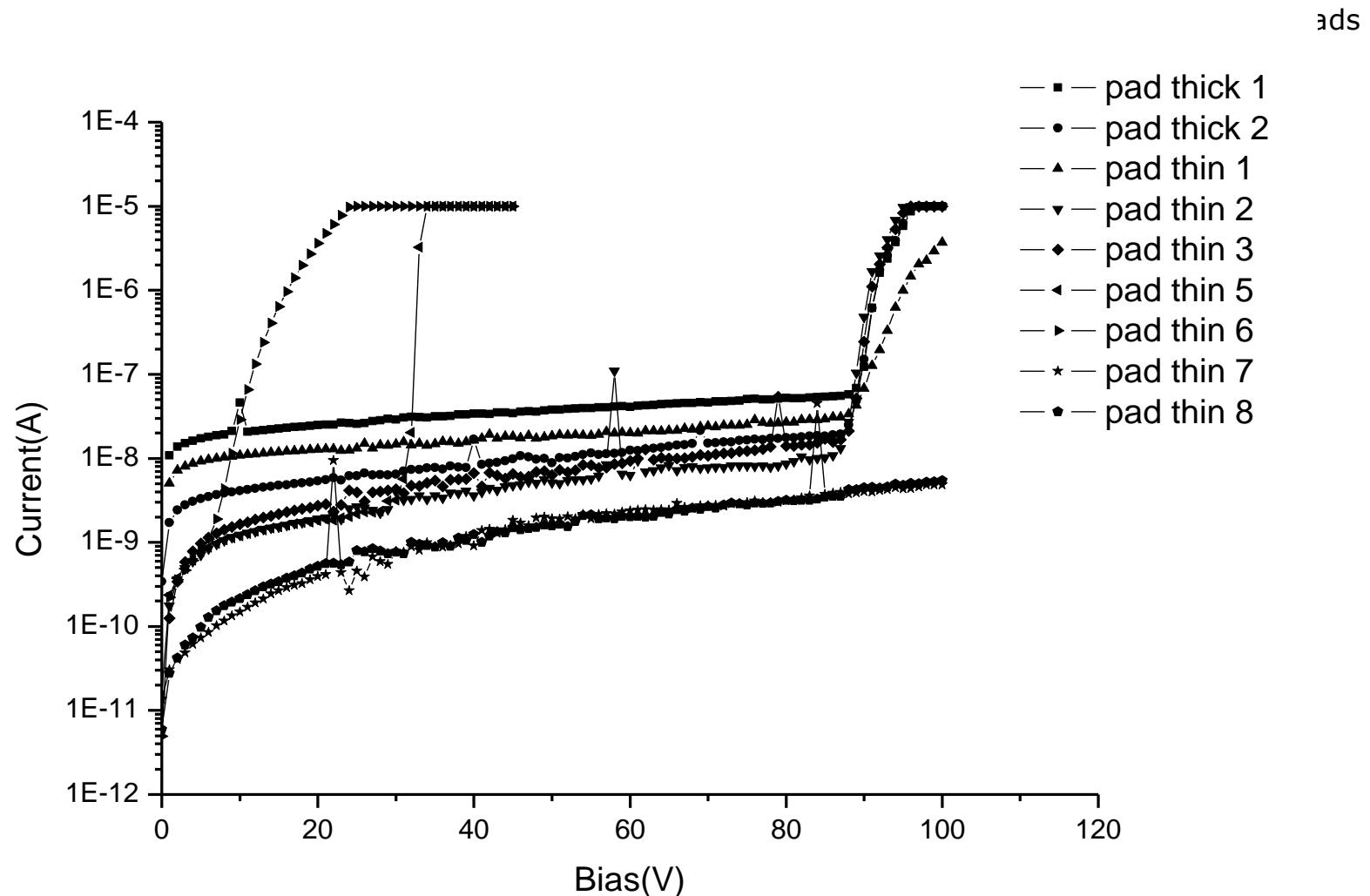
Ultra Thin 3D detectors

The device is a novel ultra-thin silicon detector with only $10\mu\text{m}$ thick active volume, fabricated on a SOI wafer. The collecting electrodes are columns etched through the silicon instead of being implanted on the surface like in the standard planar technology, allowing lower capacitance.

The neutron sensitive element is a boron-based converter layer deposited on the front side of the U3DTHIN which detects the charged particles produced via the $^{10}\text{B}(\text{n},\text{alpha})^{7}\text{Li}$ reaction.



Design and characterization



4 wafers fabricated and all working

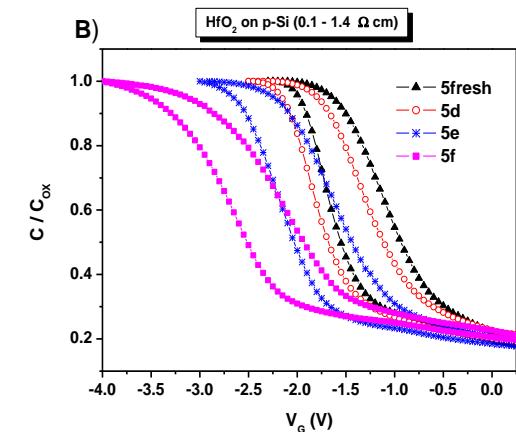
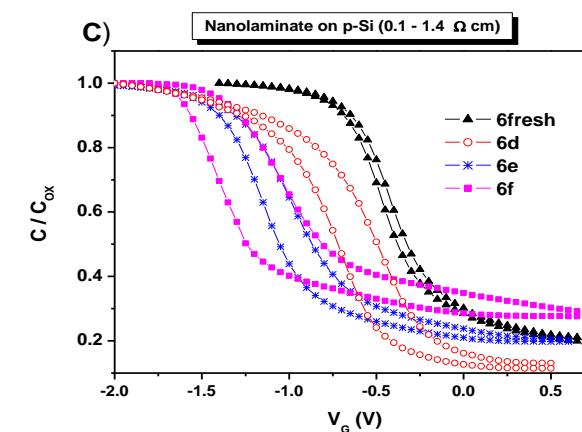
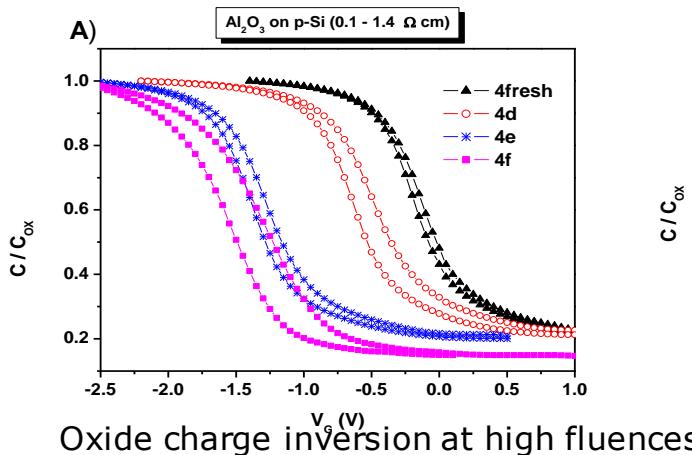
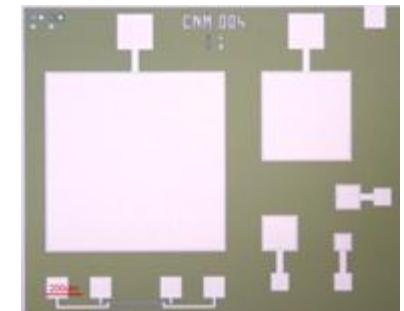
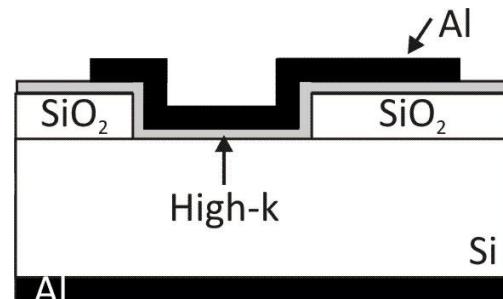


Further work and improvements

- New geometry for the p-stop surrounding the n-type holes.
- Further reduction of the wafer stress: for IBL, wafer bow is <100um.
- Increase fabrication yield: The yield of the finished wafers is 60%; anyway we still suffer from many breakings at the beginning of the process. The problem is still not fully understood. These cause an increase of the cost.
- Slim edges, if this is necessary for the experiment. At present: 200um for IBL on three sides.
- Better aspect ratio of the holes: this could increase the detector efficiency.
- Small production proved to be possible for 3D detectors, the IBL common mask between CNM and FBK proved to be a good approach for the fast track decision. This could be repeated for the upgrade.



Previous work at CNM with high-k dielectrics



H. Garcia et al., 220th ECS Meeting **Physics and Technology of High-k Materials 9** - October 9 - October 14, 2011 , Boston, MA
ECS Transactions, v. 41, no. 3, 2010, pp. 349-359

Irradiations were performed at Takasaki-JAERI in Japan

2 MeV electrons for three different fluences: $\phi = 1 \times 10^{14} \text{ e/cm}^2$, $1 \times 10^{15} \text{ e/cm}^2$ and $1 \times 10^{16} \text{ e/cm}^2$

The total ionizing doses were about 2.5 Mrad-Si, 25 Mrad-Si and 250 Mrad-Si

Irradiation was performed at room temperature and capacitors not biased.

