

# New fabrication run of CMS 3d pixel detectors at CNM

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CNM-IFCA-PSI

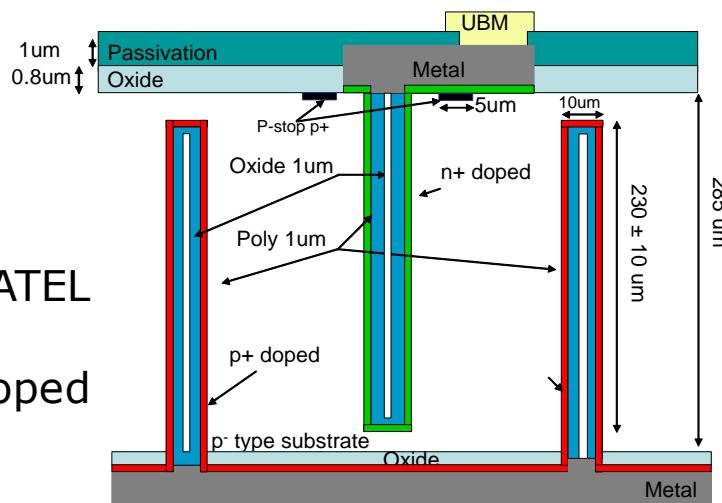


1. 3D detector technology at IMB-CNM
2. CMS mask description
3. Fabrication overview
4. Electrical measurements
5. Future work

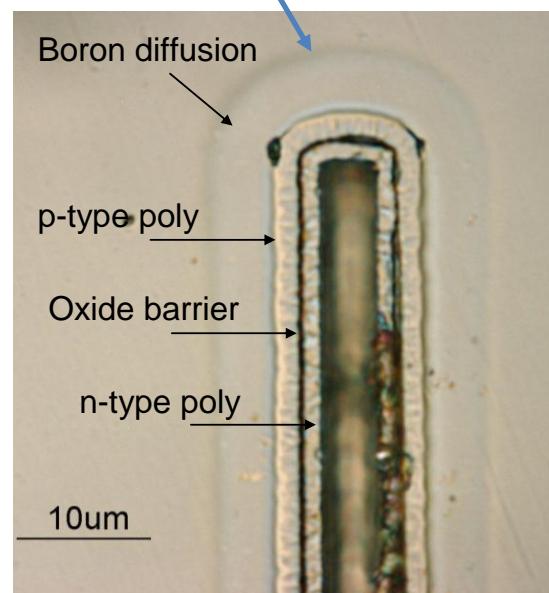
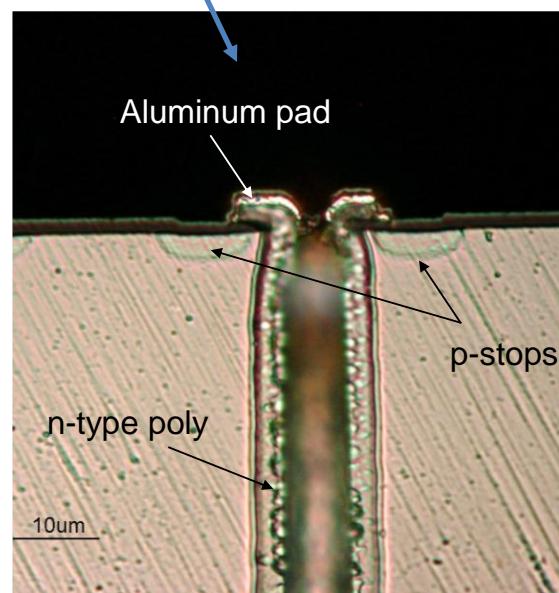
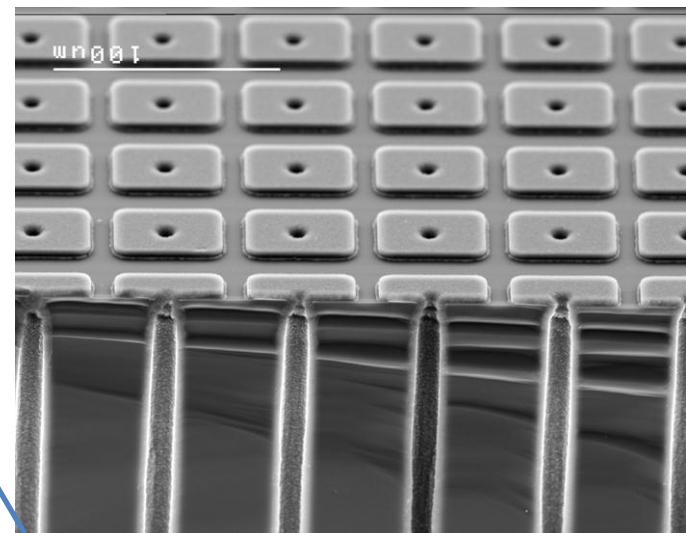
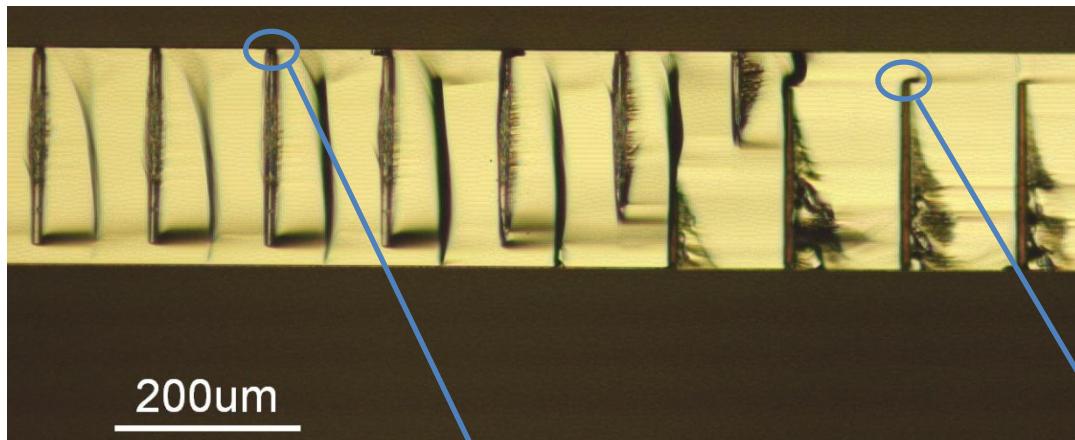


## 3D Technology:

- 4" silicon wafer
- 285um FZ high resistivity wafers (n and p- types)
- All fabrication done in-house
  - ICP etching of the holes: Bosch process, ALCATEL 601-E
  - Holes partially filled with LPCVD polysilicon doped with P or B
  - P-stop ion implantation
- Double side process proposed by CNM in 2006
  - First fabrication of 3D double sided in 2007.
  - Since 2007 runs ongoing continuously.
  - In 2010 CNM started the fabrication on 230um thick wafers.
- Devices tested under extreme radiation fluences.
  - Different test beam successfully carried out on device before and after irradiation at SHLC fluences ( $2 \times 10^{16} \text{ cm}^2 1 \text{ MeV n Eq.}$ ).



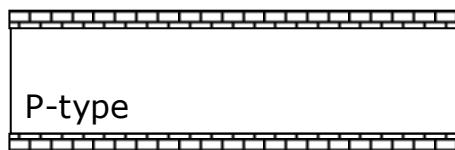
## 3D Technology:



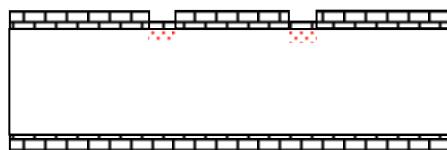
## 3D process with polysilicon resistor grid

8 mask levels + 2 for back side processing (no used)

1- wafer preparation



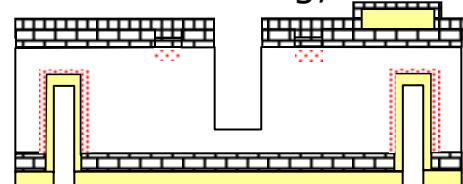
2- p-stop definition



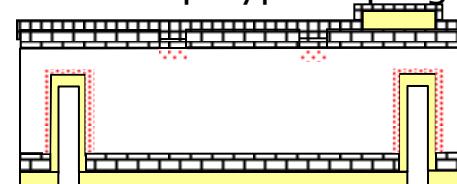
3- polysilicon resistor



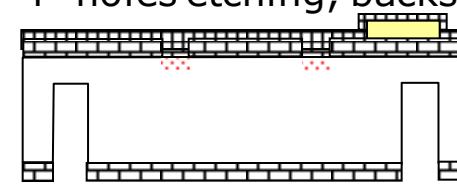
6- holes etching, front side



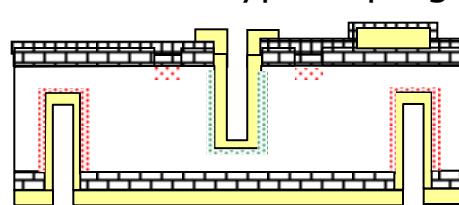
5- holes p-type doping



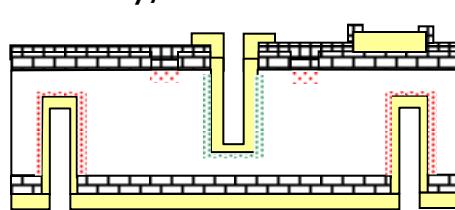
4- holes etching, backside



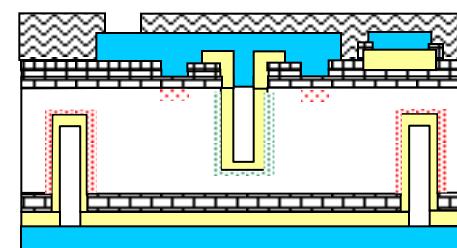
7- holes n-type doping



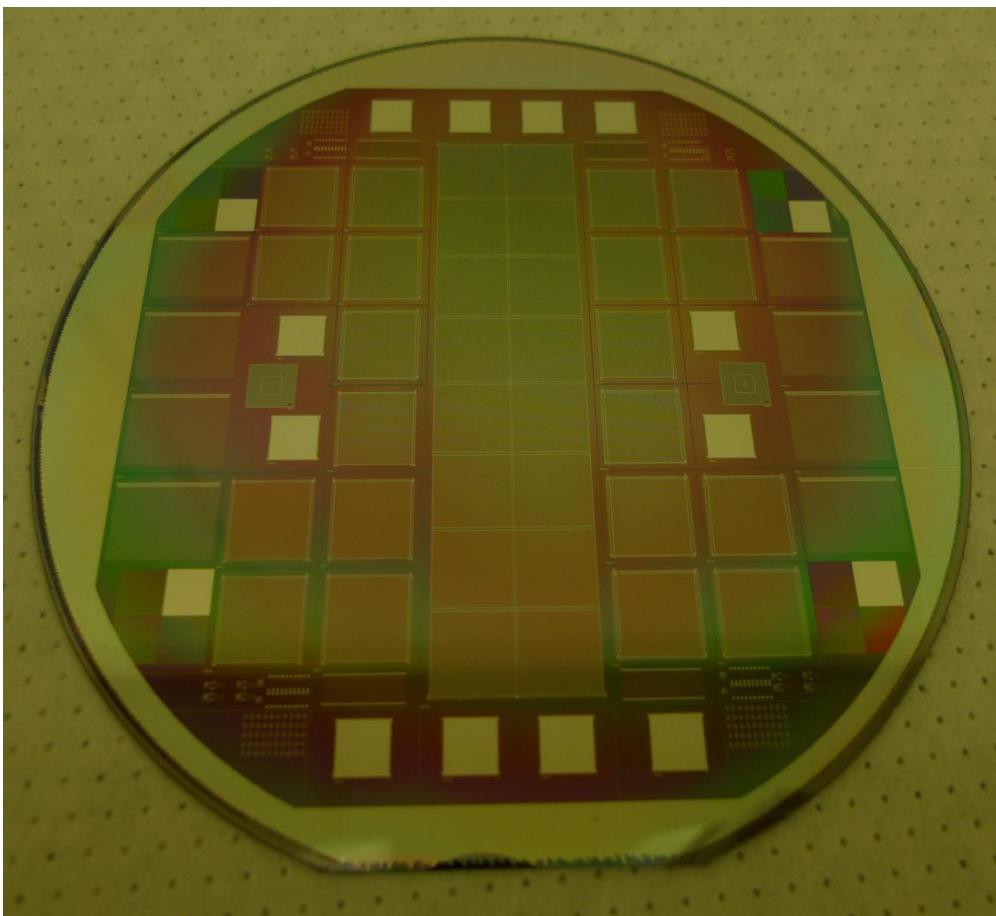
8- Poly/metal contact



9- metallization and passivation



# Production



**6 wafers:**

**Wafers 5,6,7,8:**

- 285 µm thickness

**Wafer 11:**

- 230 µm thickness

**Wafer 3:**

- 285 µm thickness

- Resistor bias

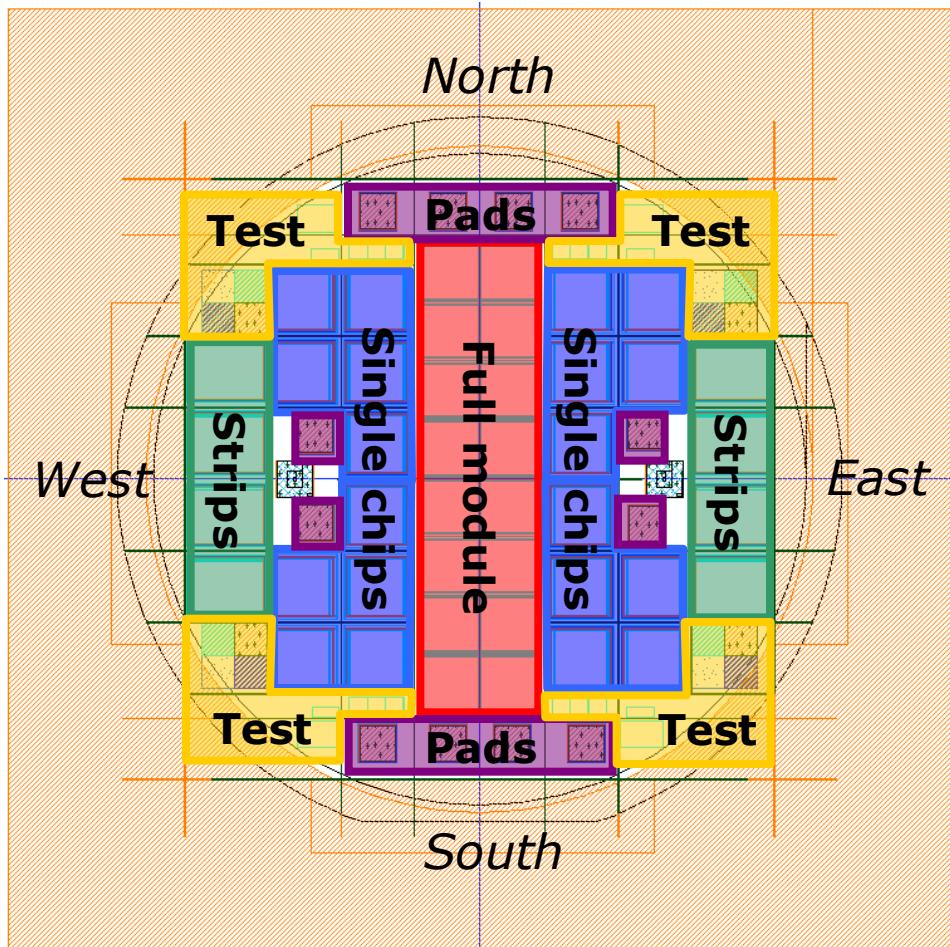
**grid**

**Bows:**

- W3 → - 205.6 µm
- W5 → - 225.4 µm
- W6 → - 235.5 µm
- W7 → - 215.1 µm
- W8 → - 219.6 µm
- W11 → - 257.3 µm



## CMS 3D Mask



Each wafer includes:

- 1 Full module (8x2)
- 4x5 Single Chips
- 8 3D-Strip sensors
- 12 Pads
- Test structures

General parameters

- Holes N:
  - Ø 10um
  - Polysilicon: 16um
  - P-stop:  $R_{int}=10\text{um}$ ,  $R_{ext}=15\text{um}$
- Holes P:
  - Ø 10um on the backside
- Bump pads
  - passivation opening: 15um hexagon
  - UBM: 20um hexagon



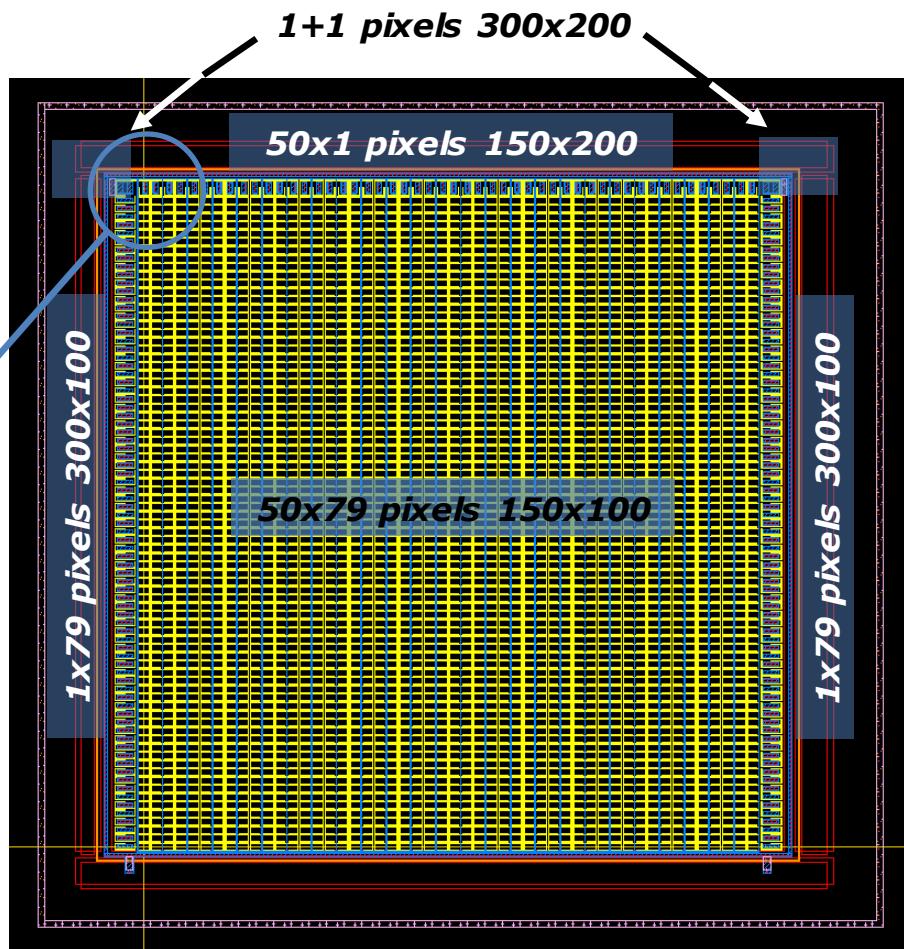
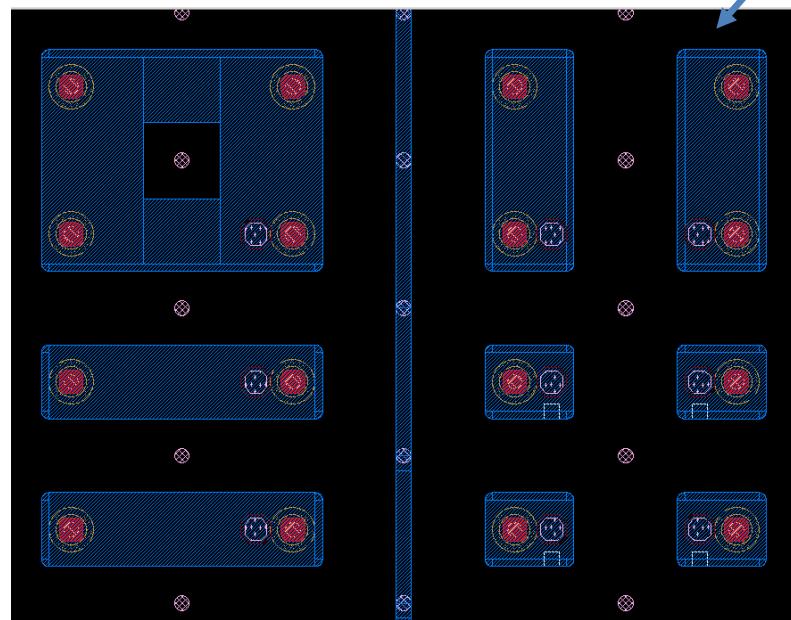
## CMS 3D Mask

Ref.	Name	Qty	Description	Holes-p pattern	Guard ring
1	CMS_MC	1	Large module with a matrix 8x2 detectors	sparse	single
2	CMS_SC_11	5	Single chip detector	sparse	single
3	CMS_SC_12	5	Single chip detector	sparse	double
4	CMS_SC_21	5	Single chip detector	dense	single
5	CMS_SC_22	5	Single chip detector	dense	double
6	3d-strip detector	8	3d-strip detectors with 128 strips of 80um pitch, 15um strip width and single guard ring.		
7	3d-pad detector	12	3d-pad detector with single guard ring.		
8	Test structures	-	Layer deposition test, polysilicon resistance test, hole alignment test.		



## Pixel design

- 50x79 pixels 150x100
- 50x1 pixels 150x200
- 1x79 pixels 300x100
- 1+1 pixels 300x200



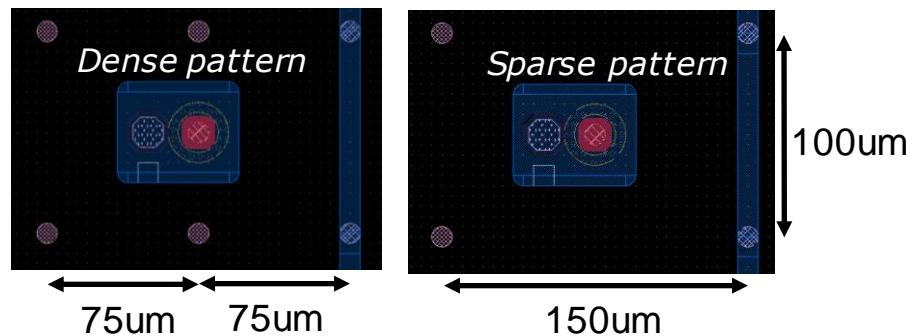
## Holes-p pattern (backside)

Dense pattern:

- Shorter drift distance
- Higher radiation resistance expected

Sparse pattern:

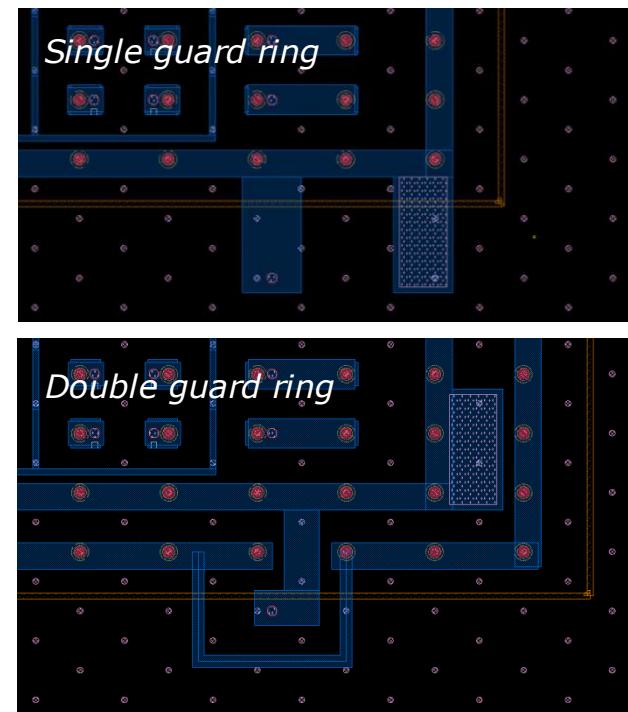
- Lower capacitance
- Lower noise expected



## Guard rings

Two kinds of guard rings:

- Single guard ring
- Double guard ring

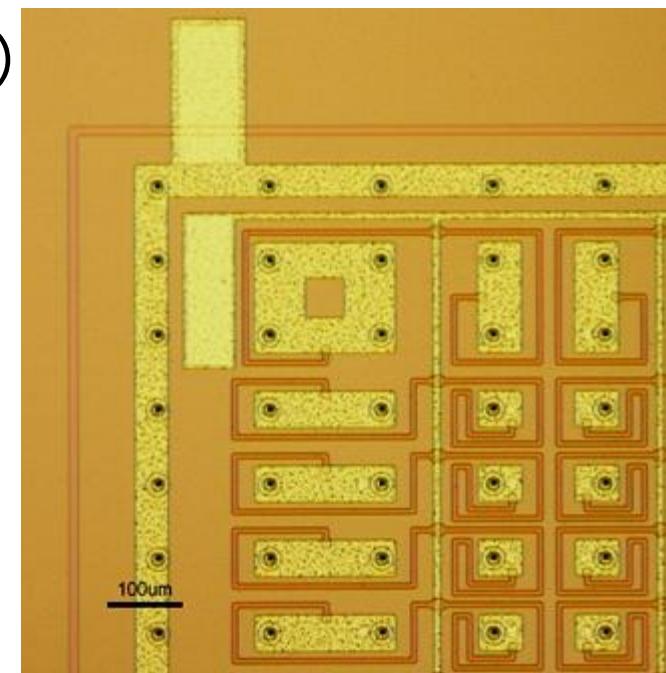
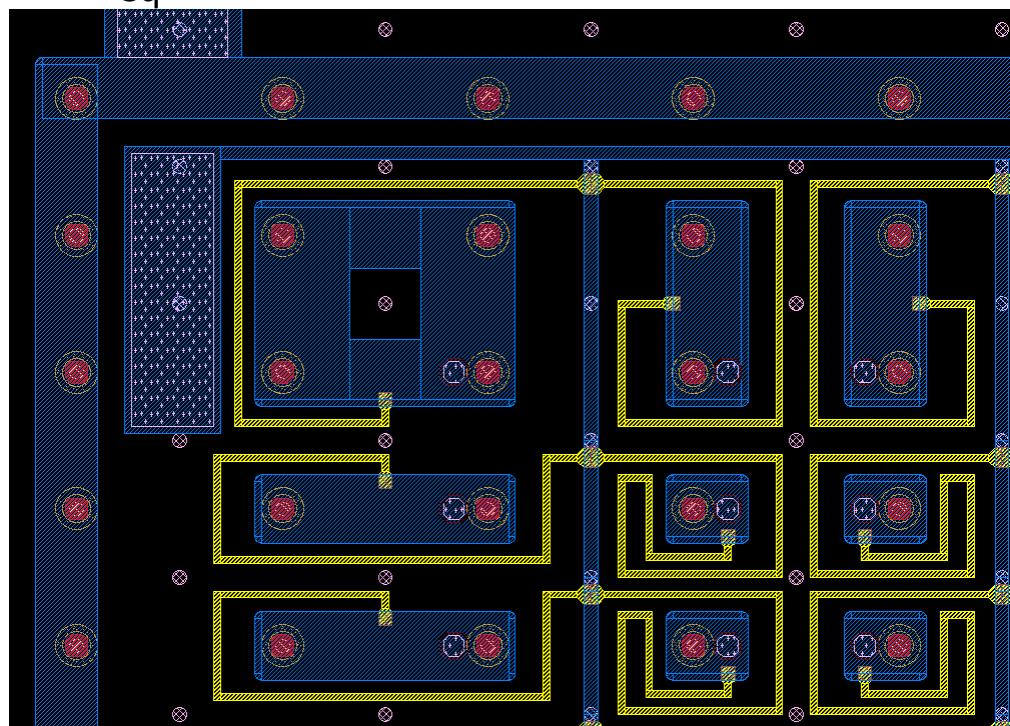


Full module is implemented with sparse pattern of p-type holes and single guard ring



## Polysilicon resistors

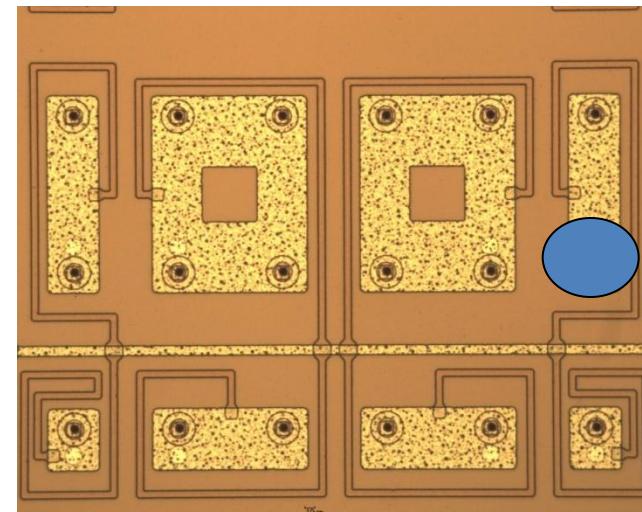
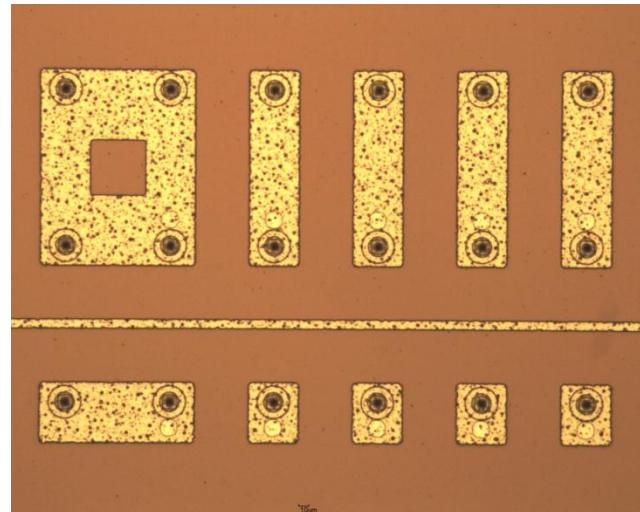
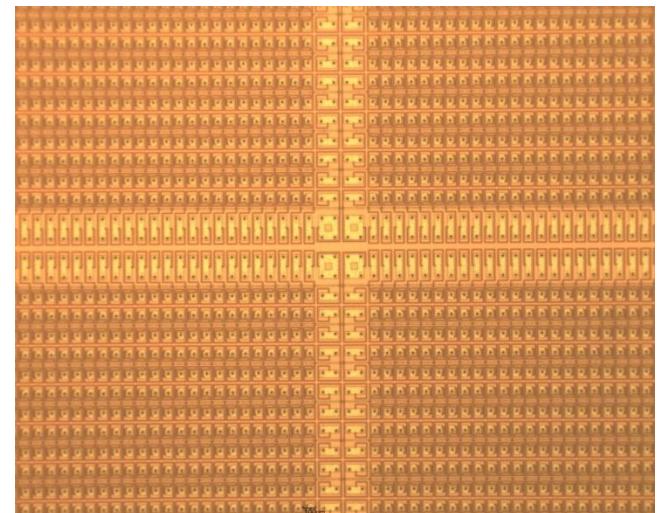
- A grid of polysilicon resistor was implemented for direct testing of pixels before flip-chip
- 2 extra mask level needed
- $R_{sq} \sim 1M\Omega$  (defined by ion implantation)



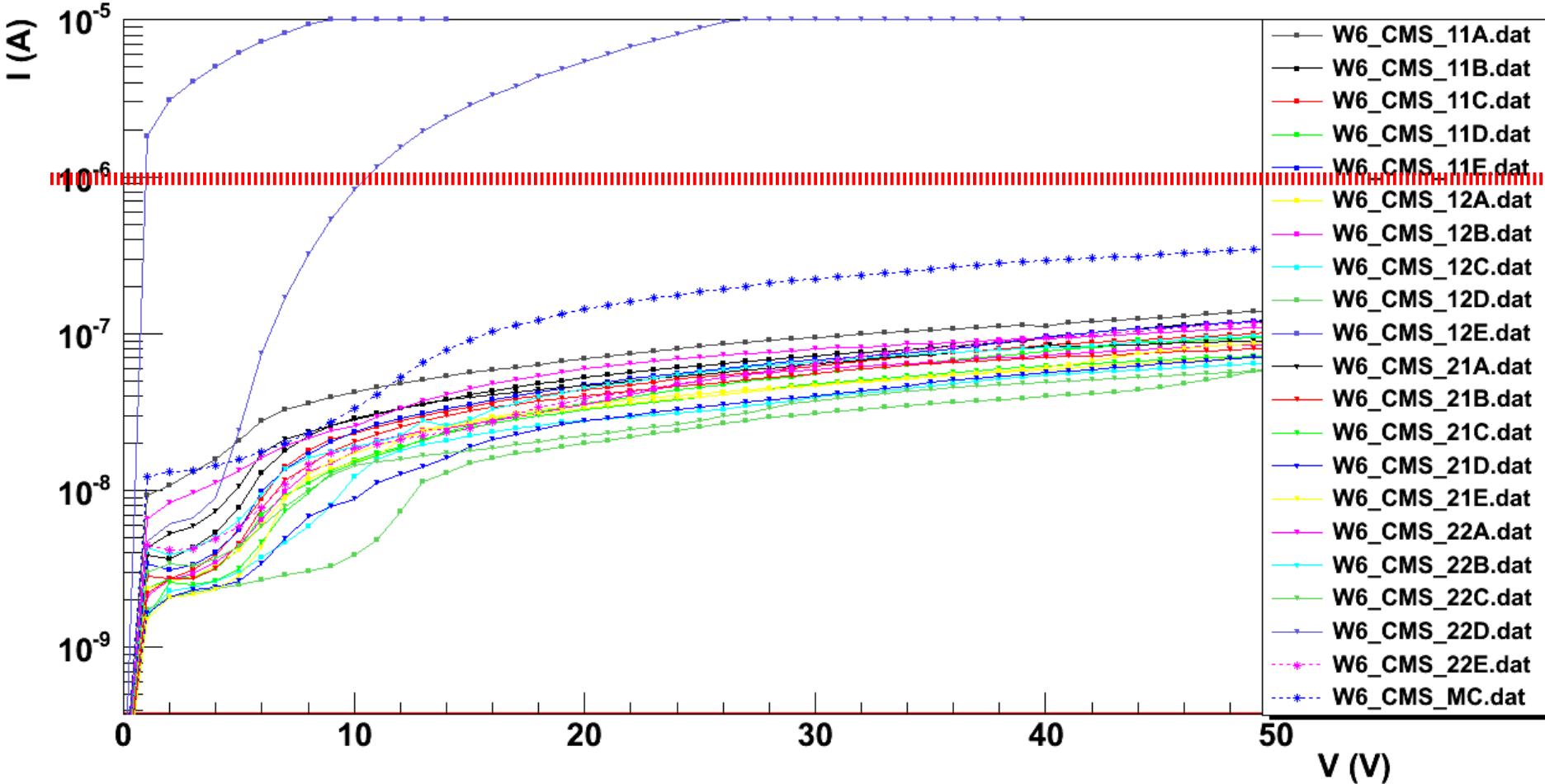
## Fabrication overview

12 wafers started:

- 4 with polysilicon resistors: 1 ended
- 6 standard 285um thick: 4 ended
- 2 thin 230um thick: 1 ended

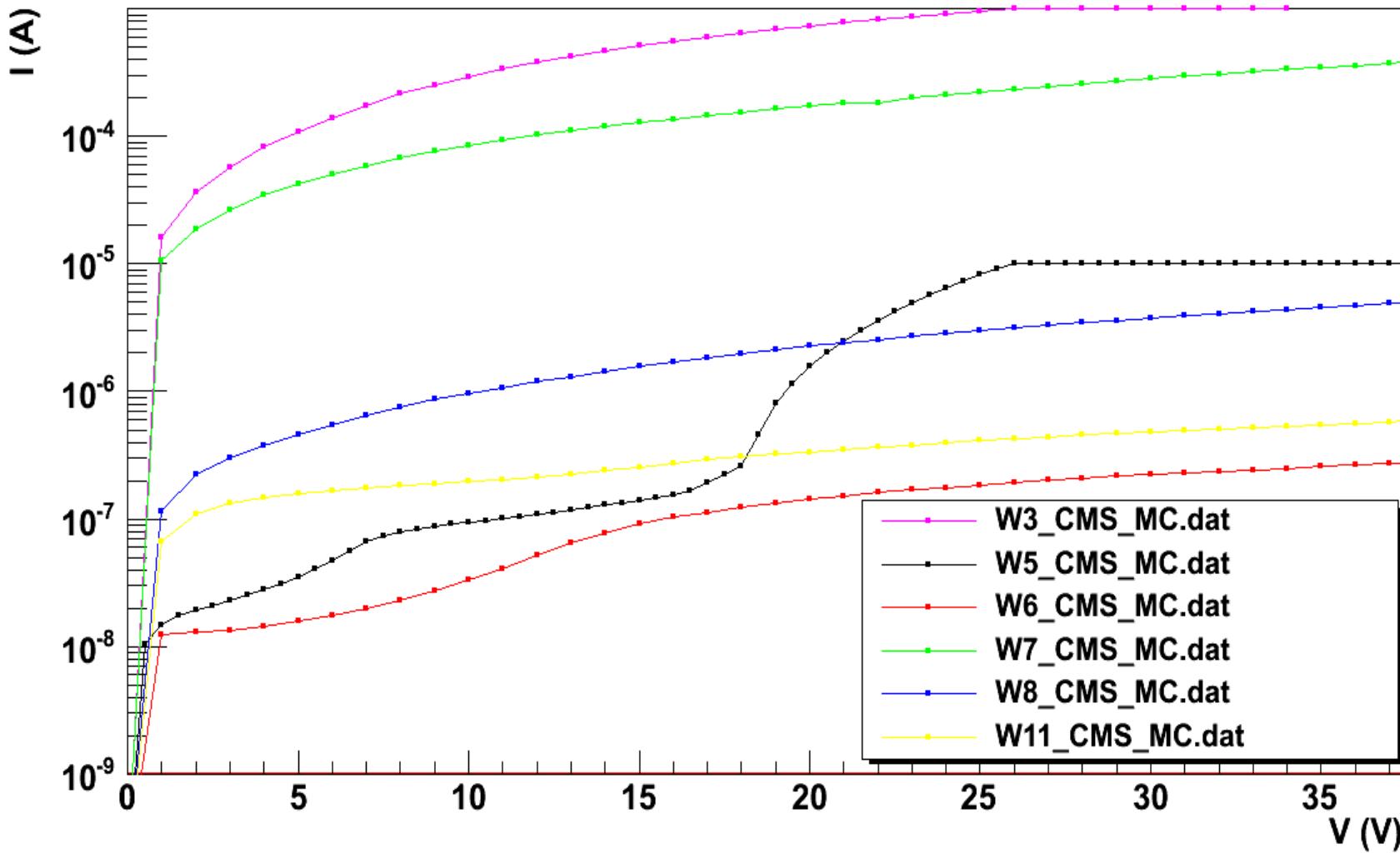


# WAFER 6

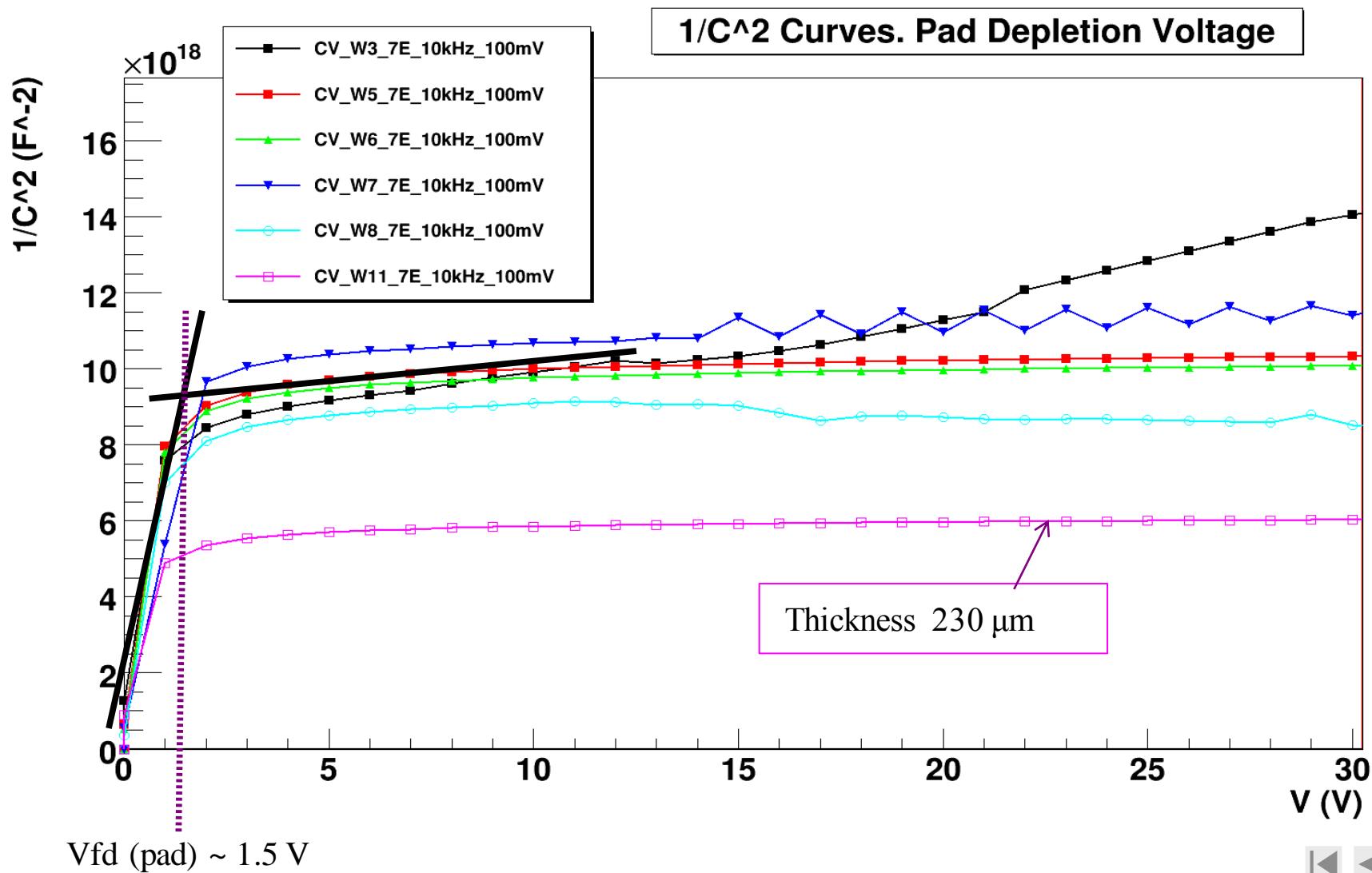
**Wafer 6**

# MC Devices (8x2 detectors)

MC (8x2 detectors)



# CV Curves. Pad Measurements

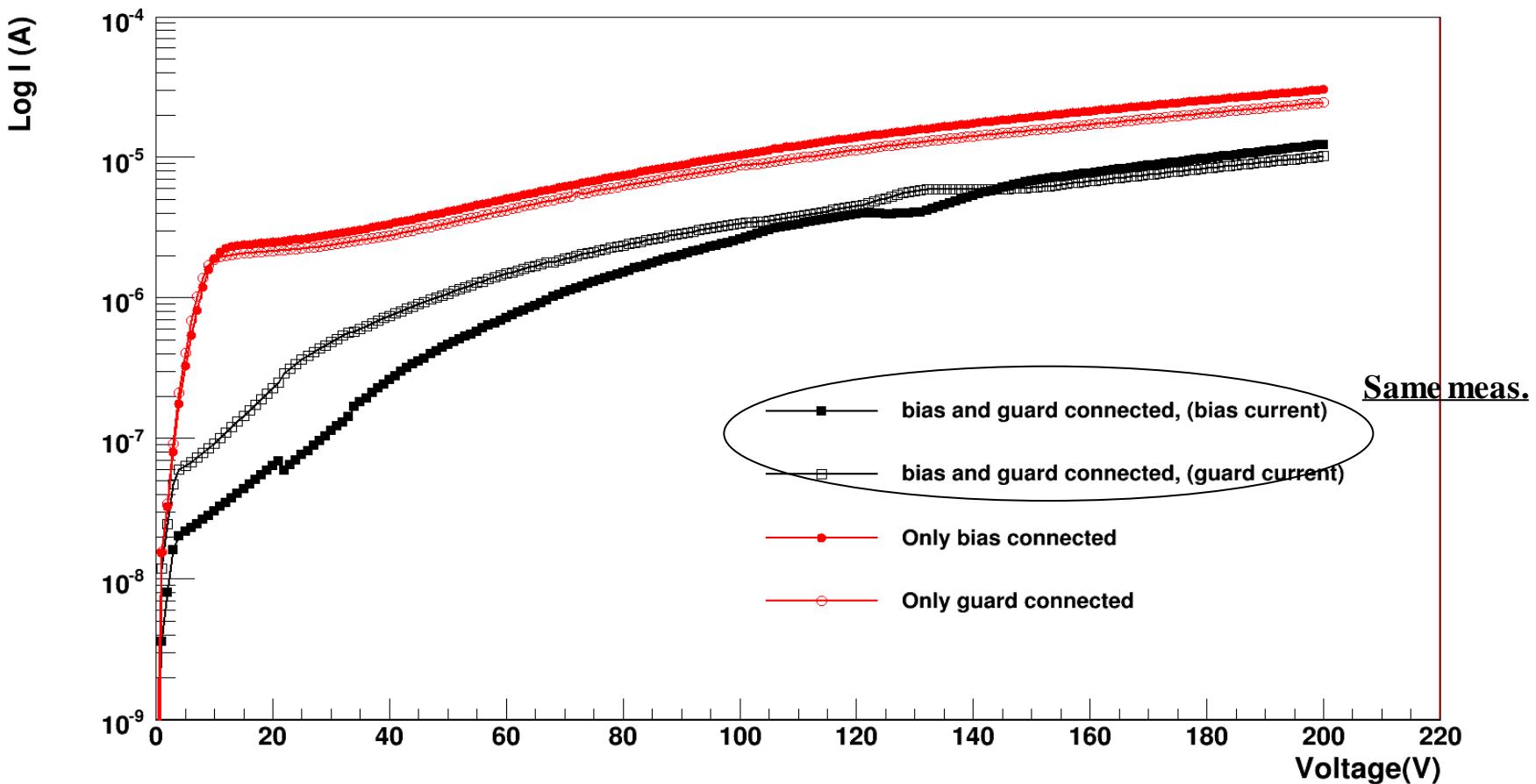


# Biasing studies. Wafer 3

Only guard connected → “punch through” polarization

Only bias connected → pixel by pixel polarization

**biasing studies. Detector 12B**



# Planned measurements (T. Rohe)

- Schedule for pixels:
  - · (now-week 28) Bump deposition/dicing/capacitance measurement(2 Single Chips)/flip-chip
    - =>  $2+4+8 = 14$  SC modules to be assembled (see irradiation details below).
  - · (week 28-29) first irradiation at KIT (1.2 E15 & 5 E15)
  - · (week 29-30-31) Source testing at PSI
  - · (week 31-32) Test beam at PS
  - · (week ?) Second irradiation at KIT ( 1.E16?)
  - · (week 48) Test beam at SPS ?
- - Irradiation campaign:
  - - 2 reference sensors per layout => 4 Reference sensors.
    - to be funded by the AIDA project (PSI will apply).
  - - 2 SC modules to be irradiated per fluence and per layout (dense/spare) => 8 SC modules (about 4 cm<sup>2</sup>) to be irradiated in total.
  - - Interest from Pordue in testing the devices.