# Progress on Scribe-Cleave-Passivate (SCP) Slim Edge Technology

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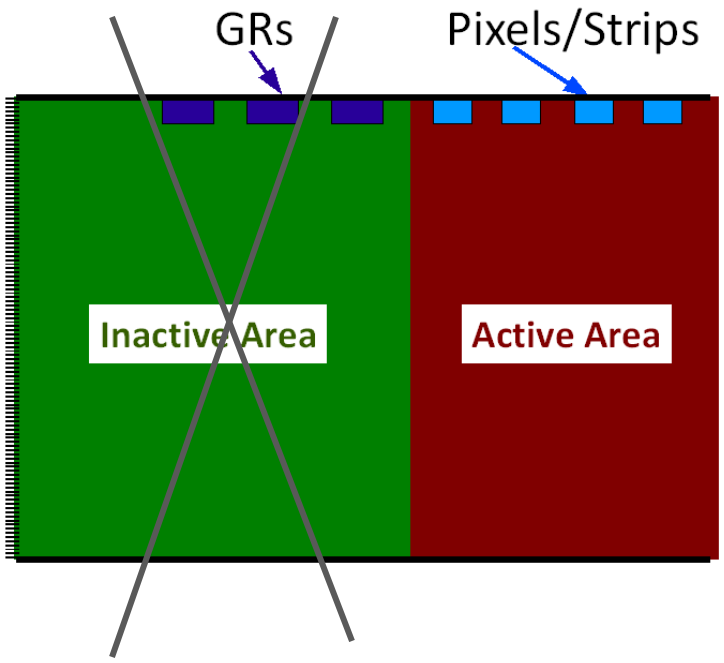
# Outline

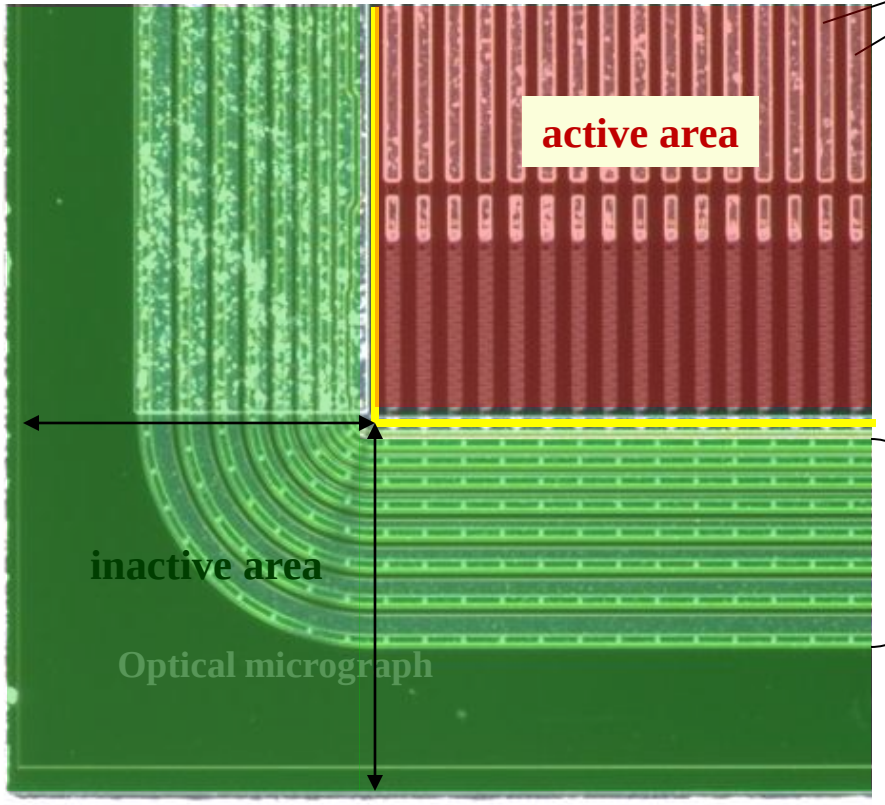
- Slim Edges – Motivation
- SCP Method
- Recent Progress:
  - Passivation for N-type devices
  - Scribing
  - Industrialization
  - Radiation Hardness
- RD50 and Matrix of Requests
- Conclusions and Outlook

# Motivation – Slim Edges

## Side View




## Top View




**Slim edges offer:**

- **reduced inactive area =>**
- **more hermetic coverage**

**(better tiling of sensors)**

**This is especially important for pixels and large-area systems**

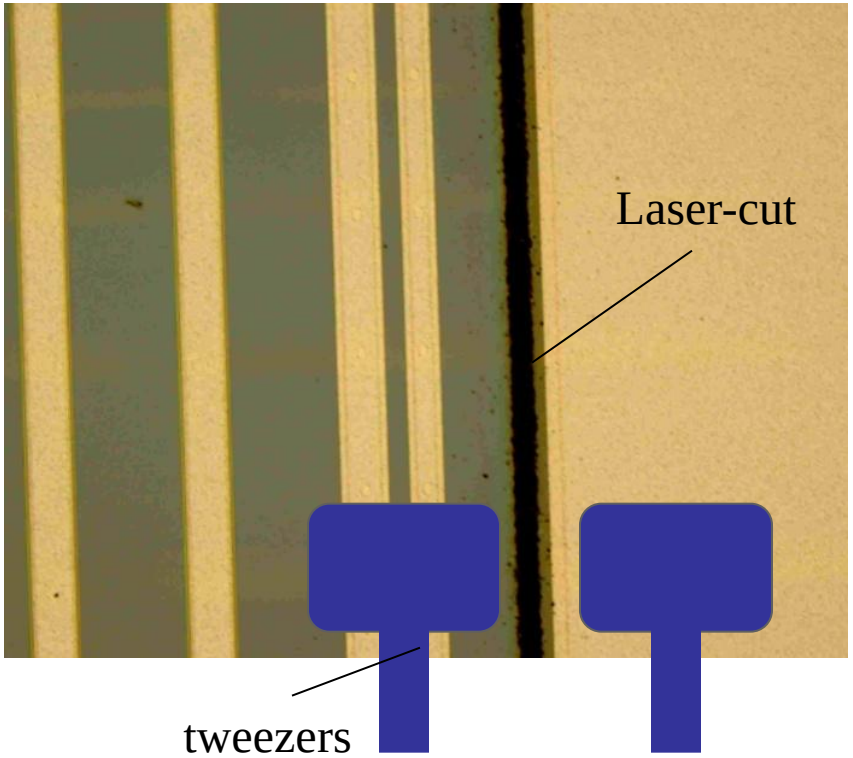
## Our Approach:

- **treat finished devices on the single die level**
- **treat p- and n-type devices**
- **minimize leakage current**
- **achieve uniform bias dependence of charge collection**

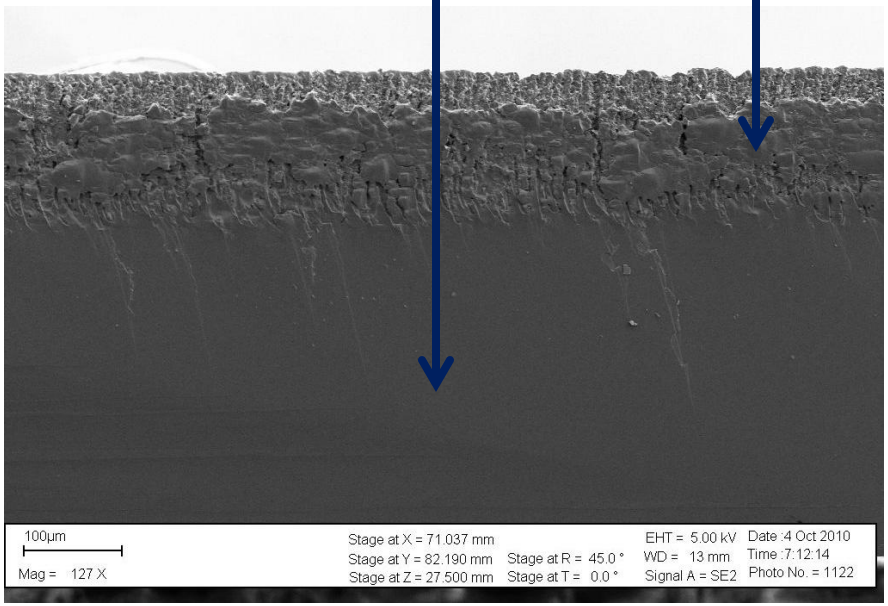
# SCP Method

**There are three key steps of the process:**
**1) Scribing on front-side (initially done by laser)**
**2) Cleaving, which leaves the surface with low defect density (initially done by tweezers)**
**3) Surface passivation to make the sidewall resistive.**

**Optical micrograph, top-view**

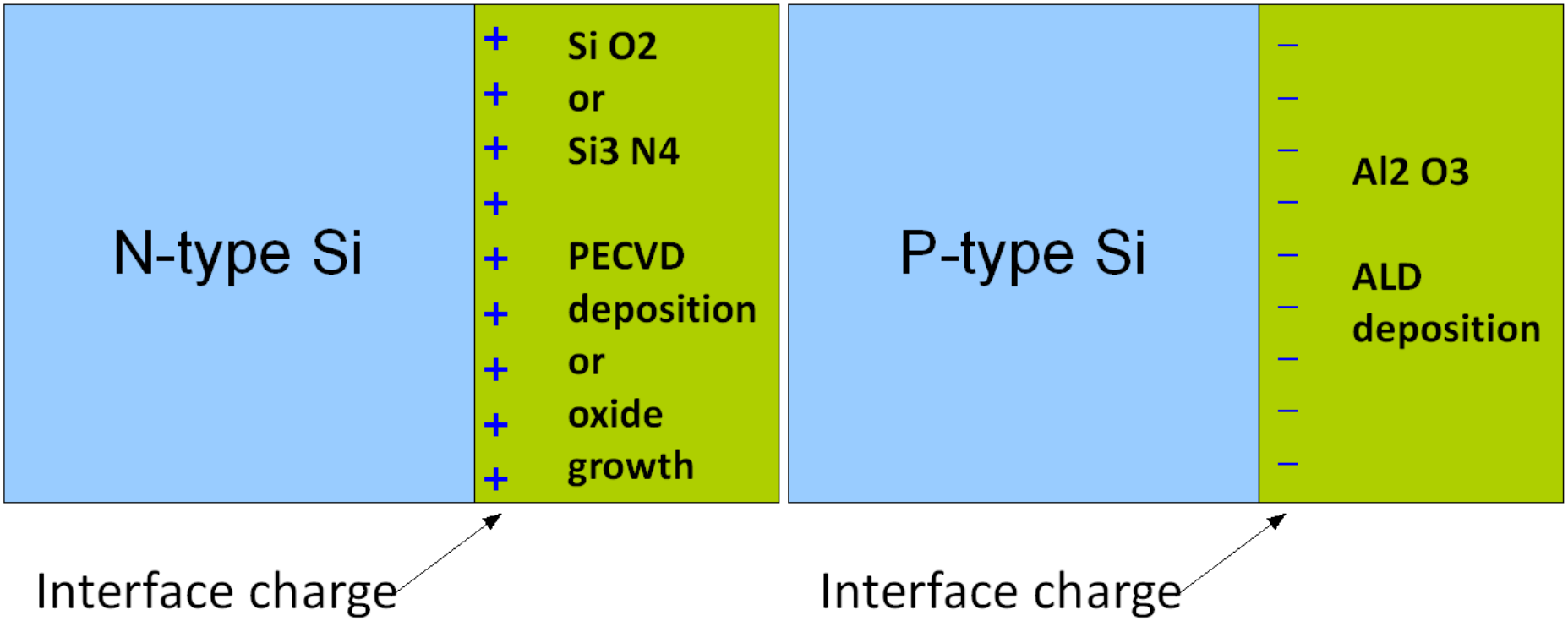



**SEM micrograph, cross-section**




Laser-scribing done at U.S. Naval Research Laboratory using an Oxford Laser Instruments E-Series tool. Breaking was initially done by hand using tweezers, but can be done fully automatic.

# Passivation Options

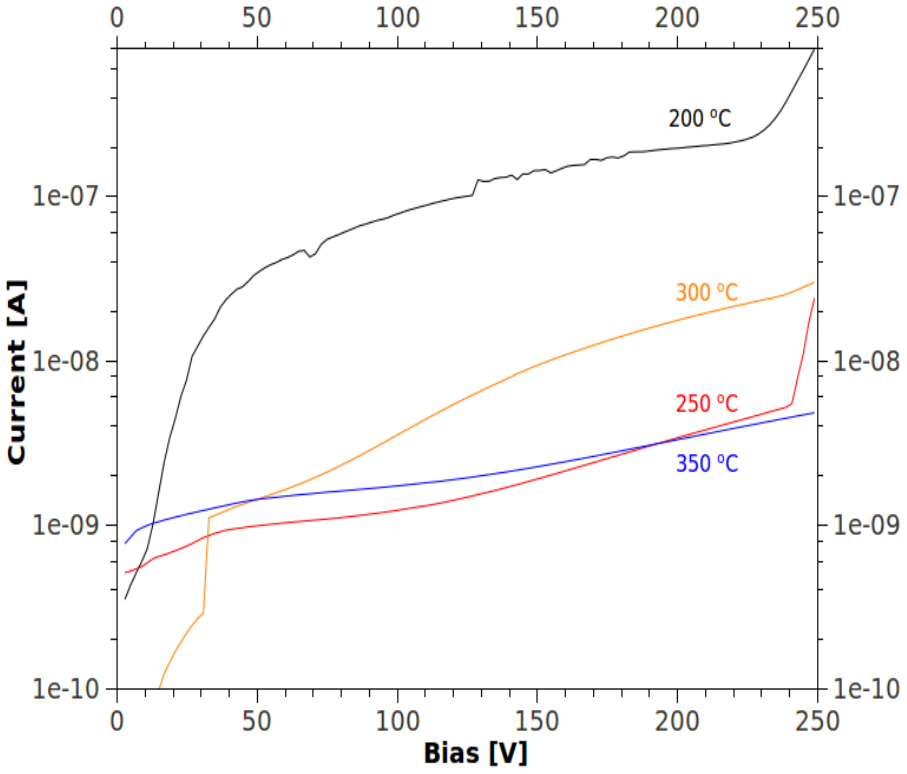



**Surface passivation makes the sidewall resistive. N- and p-type devices require different technologies.**

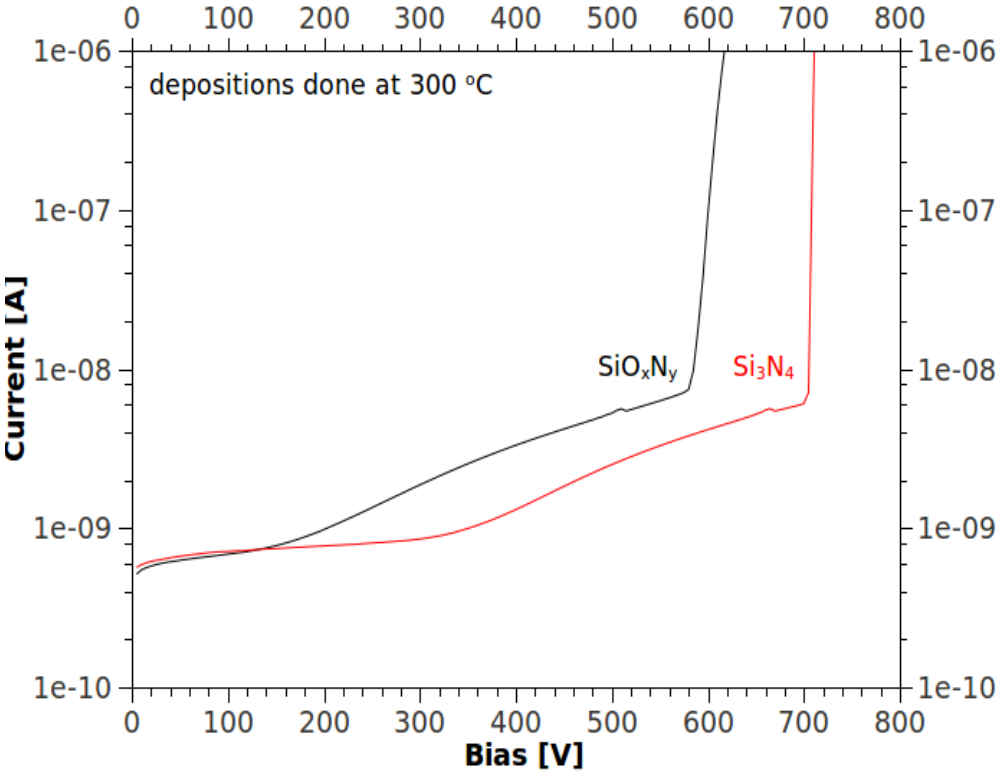
- **For n-type devices one needs a passivation with *positive* interface charge. $SiO_2$ and $Si_3N_4$ layers works well.**
- **For p-type material a passivation with negative interface charge is necessary. We found that $Al_2O_3$ works in this case.**

# Progress with Passivation (N-type Diodes)

## Si Oxide PECVD




## Si Nitride PECVD

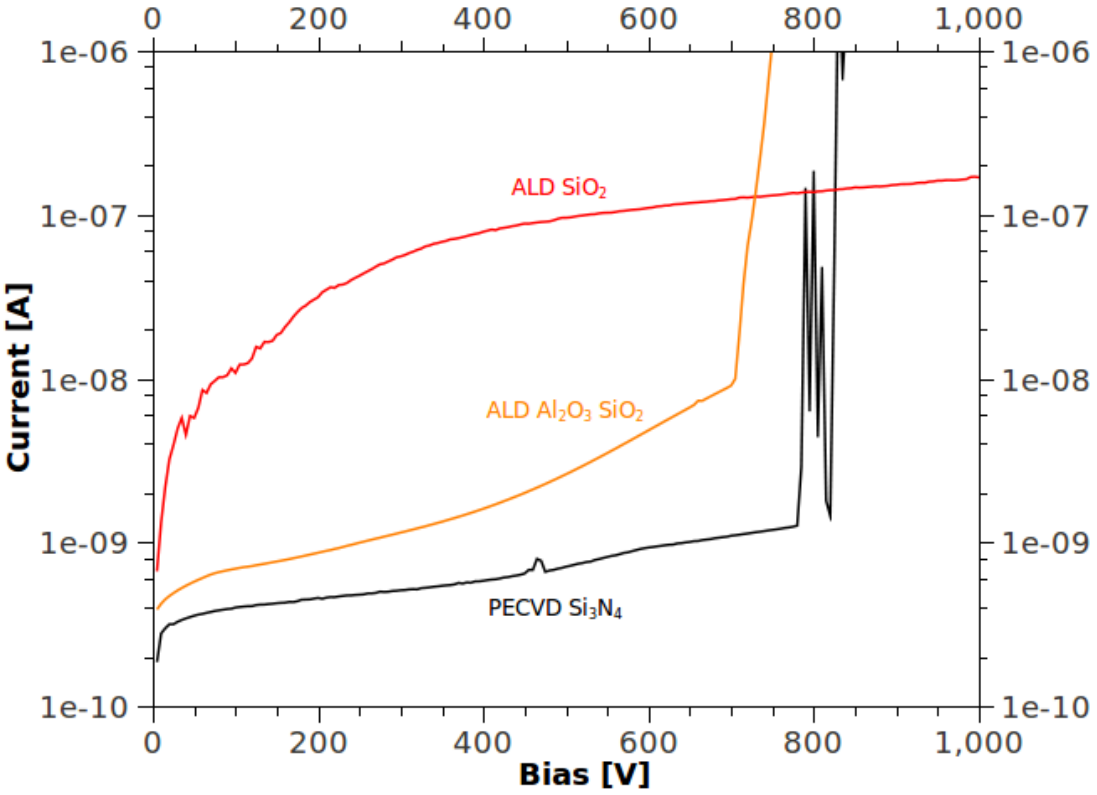



Performance dependence on the deposition temperature:
Can work in the T range that is safe for the finished devices!

Much improved leakage current and breakdown voltage with Si Nitride.

# Progress with Passivation (N-type Diodes), Cont

PECVD process has been developed by industry as a wafer process => Small height of the chamber in a typical machine. This worked well for small size samples, that could be positioned vertically, or slanted. For large sensors this is not quite applicable => replace by ALD method.

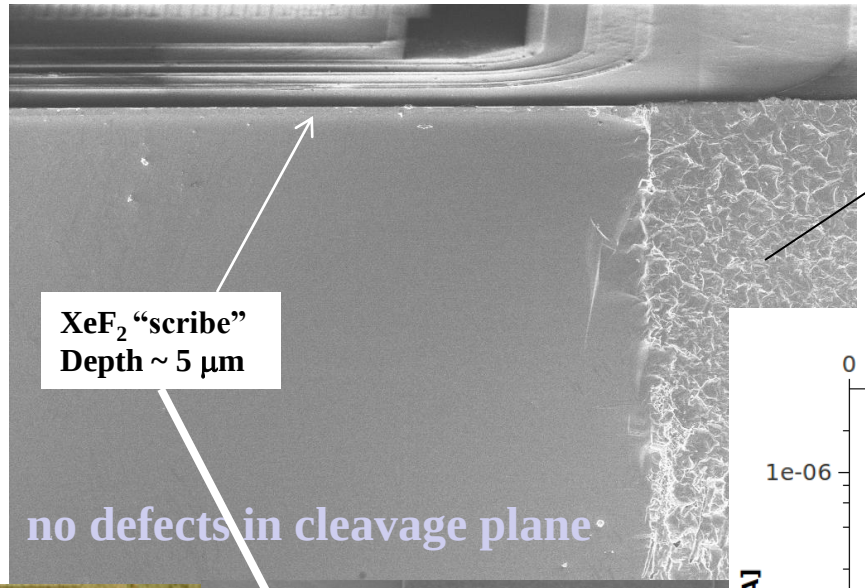


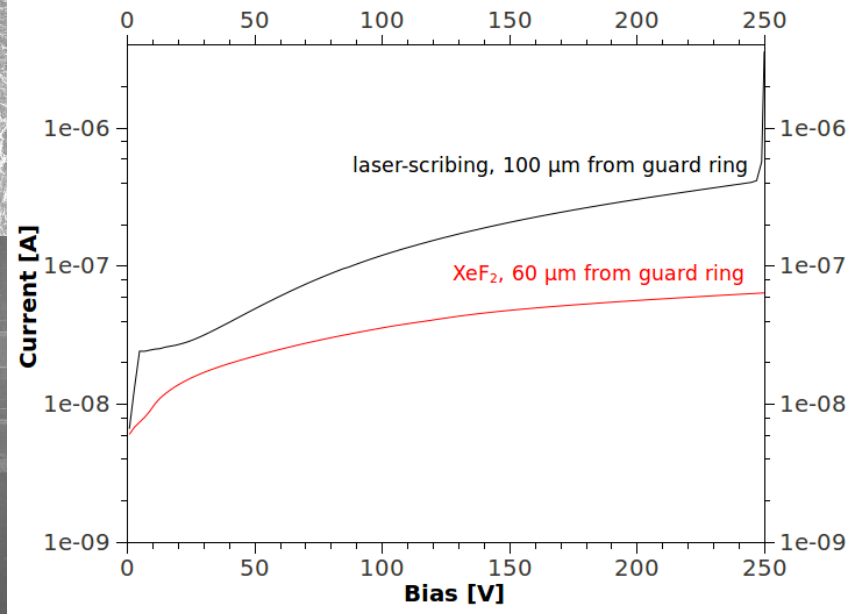

Study with HPK Fermi/GLAST diodes. The plain ALD SiO2 is worse than the best case of PECVD Si3N4.

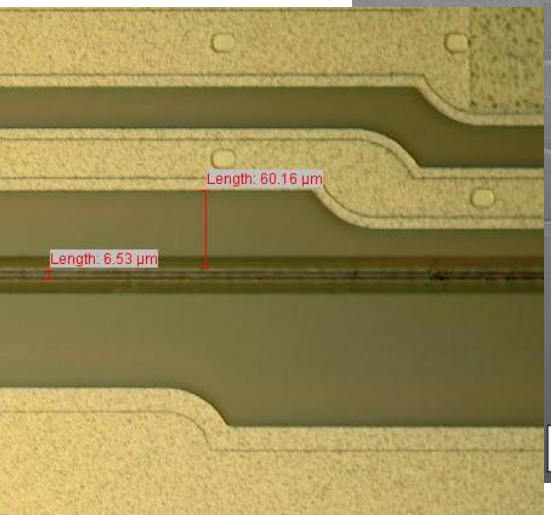
But a "nanostack" of ALD SiO2 (10 nm) and Al2O3 (50 nm) works well. Parameters are from G. Dingemans et al, J. Appl. Phys. 110, 093715 (2011); doi: 10.1063/1.3658246

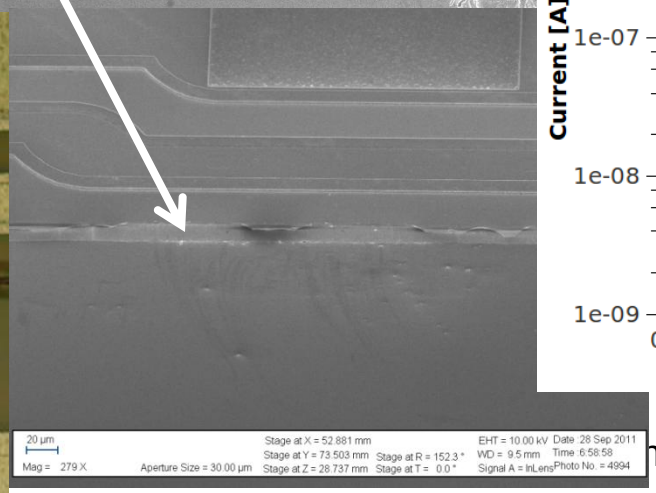
# Progress in Scribing

Laser Scribing → $XeF_2$ Etch:
reduction of the amount of sidewall damage, more control, reliability



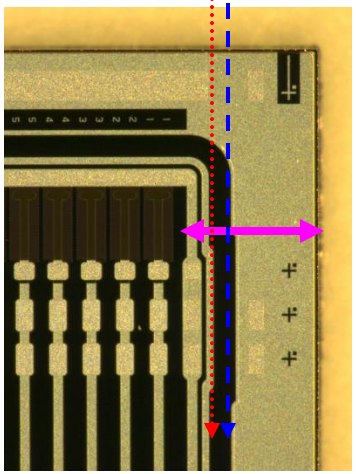



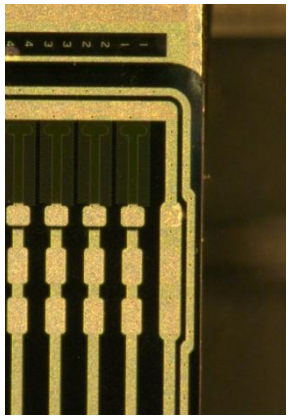
# Progress with N-type Sensors

**XeF2 scribing + Nitride PECVD**

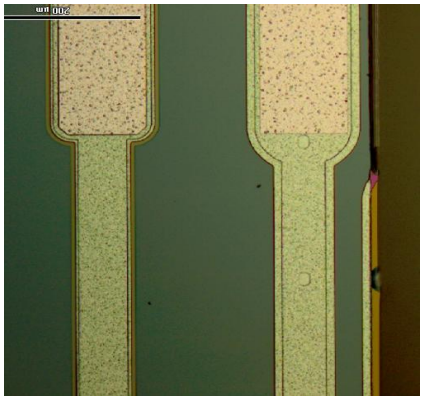
Si SSD with
900µm dead edge

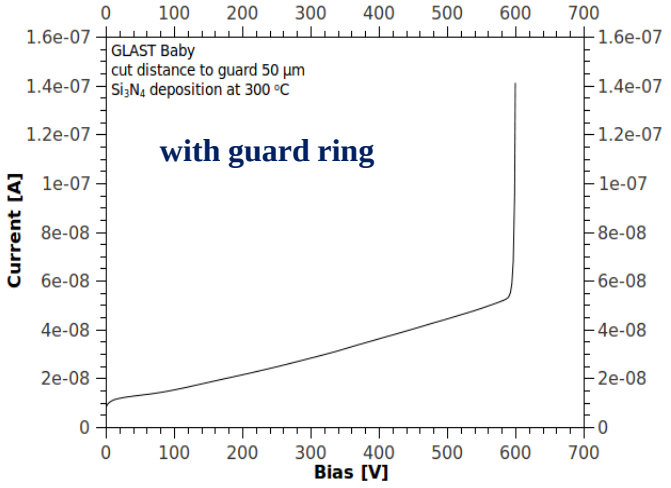


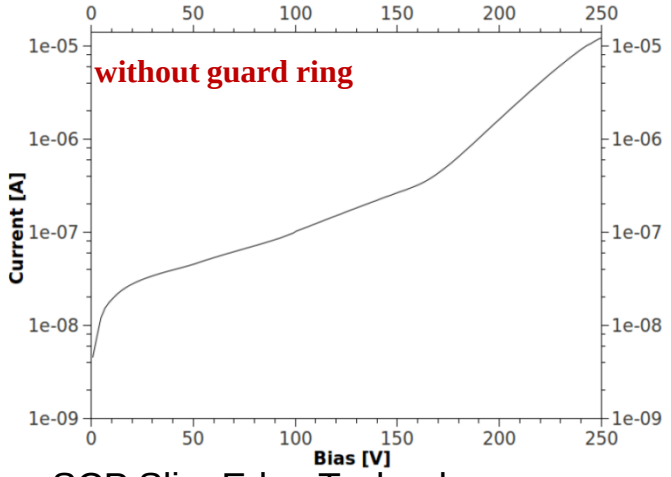
Cut within 50 µm
of Guard Ring



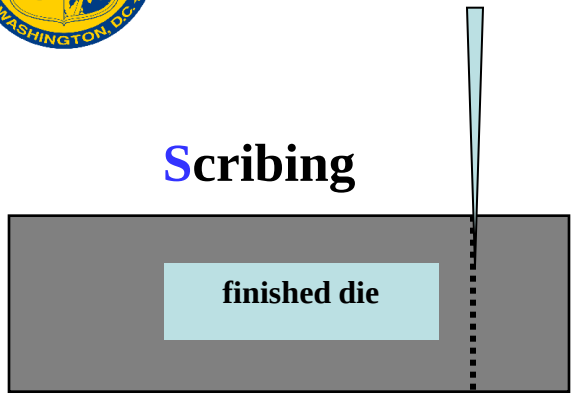
Guard Ring Cut (!)
0 µm to Guard Ring

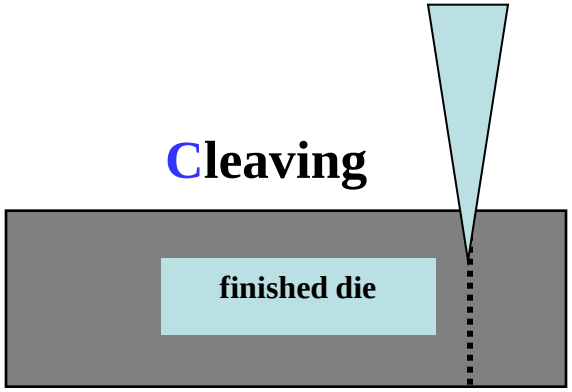


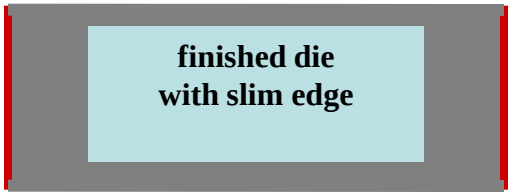


# Evolution of Slim Edge SCP Treatment




**Laser**

**$XeF_2$ Etch**

**Tweezers**

**Present Focus: Automated Cleaving**

**Native Oxide + Radiation**

**N-type** **P-type**

**PECVD Oxide**

**PECVD Nitride *or* ALD Oxide, nanostack**

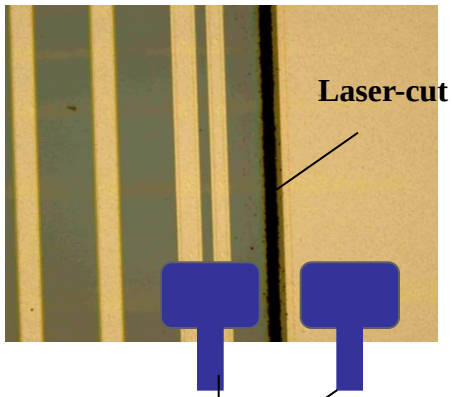
**ALD Alumina**

**CCE, Rad. Hardness**

**All Treatment is post-processing & low-temp (Etch-scribing can be done during fabrication)**

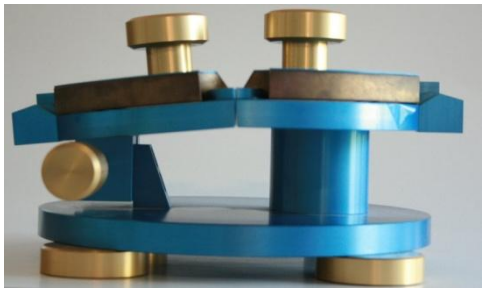
# R&D for Large-Scale Application of SCP

**Key issues in making further progress: replacement of tweezer-based cleaving!**




**Build**

Wafer Brech Maschine
Courtesy PSI and Uni Bonn



**Contract**

Industrial-scale cleaving machines:
- Dynatex (manufacturer)
- Loomis Industries (manufacturer)
- Kavli Nanosciences Institute @ CIT (facility)

LOOMIS
Patented Scribe and Break Dicing Technology
LSD-150
Scriber-dicing machine

dynatex INTERNATIONAL
semiconductor dicing equipment and materials
GST-150
ScriberBreaker

# Industrialization: Automated Scribing

Production-ready device singulation is different from initial trials:

1) Automated scribing
2) Automated cleaving
3) Done on all four sides

Automated scribing depends on the method:

- For laser scribing, it's built-in in the programmable laser + motion stages operation
- For etch-scribing, there is a need for an extra mask, but the process in inherently wafer-scale

We are in process of making wafer-level singulation tests:

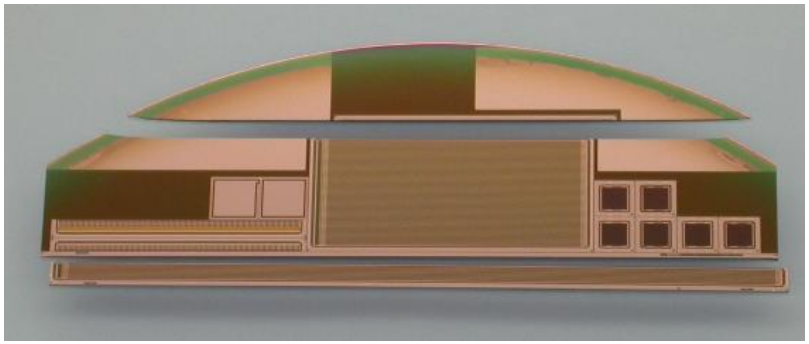
- Post-production scribing with CIS wafers courtesy Anna Macchiolo, as well as wafer pieces from recent "charge multiplication" production at Micron (Gianluigi Casse).
- Planning on doing slim edge tests fabrication with low-strip-resistance run at CNM (Miguel Ullan et al)

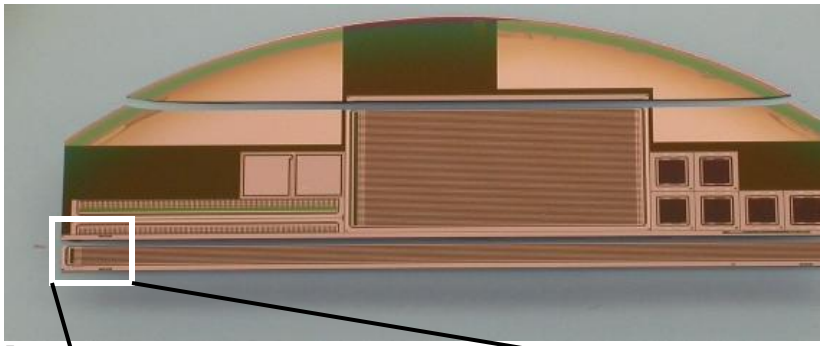
Besides XeF2 etch, there is an idea of using plasma etching for scribing (Giulio Pellegrini).

# Industrialization: Automated Processing

Production-ready device singulation is different from initial trials:

1) Automated scribing
2) Automated cleaving
3) Done on all four sides

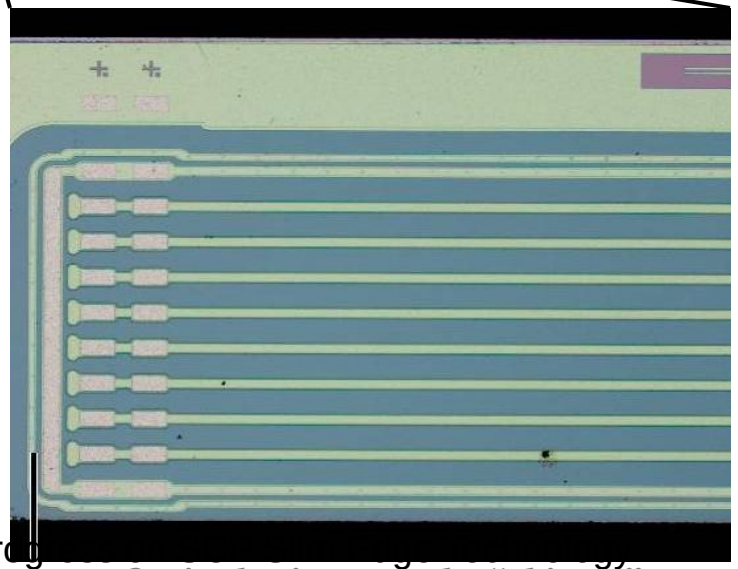




*overview photos*

Cleaving tests done at **Loomis Industries**, makers of cleaving machines and at KNI (Caltech) with Dynatex machine.

In both cases we saw that:
-- Cleaving of laser-scribed samples was successful
-- Cleaving of diamond-scribed samples was successful
-- Cleaving of etch-scribed sampled did not work



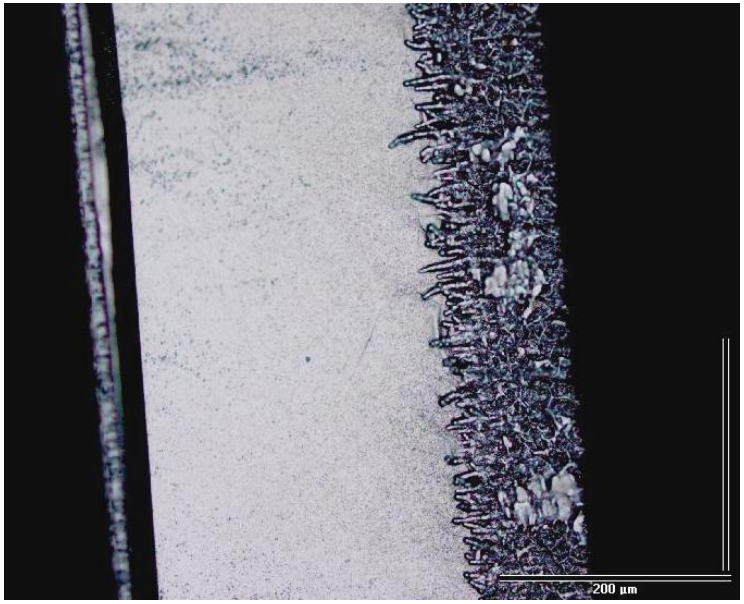
*Optical micrograph, "skinny"*

# Industrialization: Automated Processing

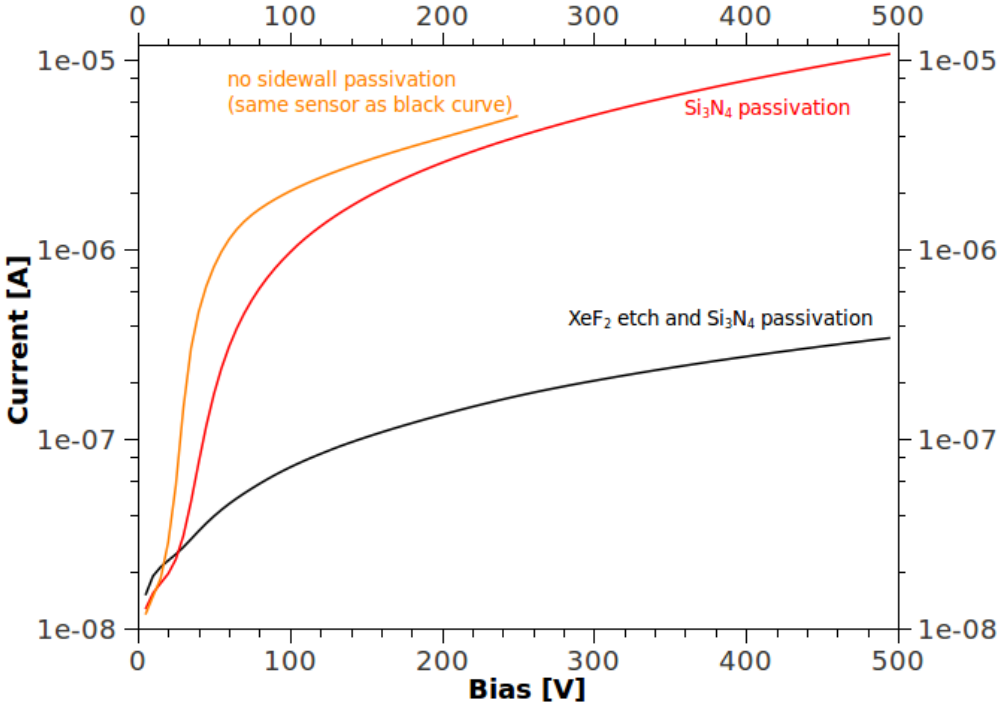
Production-ready device singulation is different from initial trials:

1) Automated scribing
2) Automated cleaving
3) Done on all four sides

Initially had high current after cleaving, even with passivation.
A key improvement was XeF2 etching of the sidewall, that removed the surface damage.




Sidewall surface after etching step.



# Industrialization: Realistic Singulation

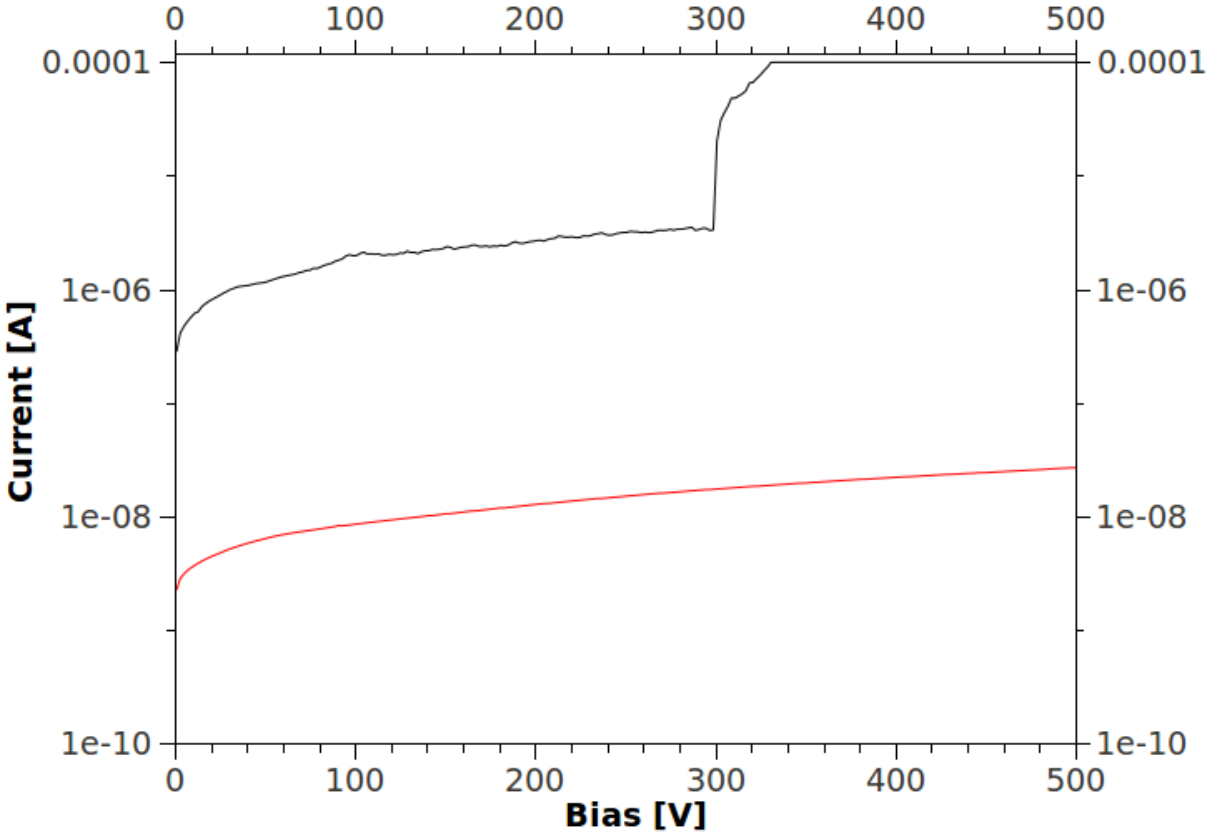
Production-ready device singulation is different from initial trials:

1) Automated scribing
2) Automated cleaving
3) Done on all four sides

4-side cleaving means intersecting cleaved wall with ‘sharp corner”.

This leads to high current.

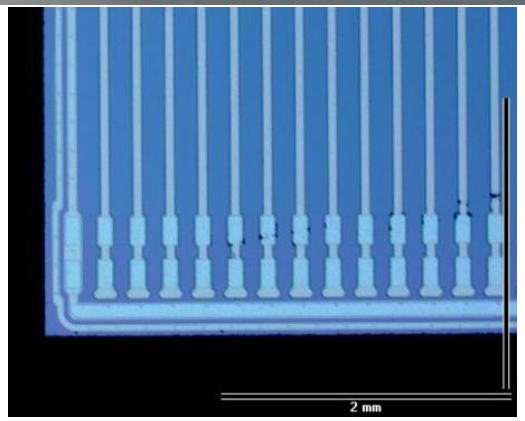
XeF2 etching of the sidewall drastically reduces the current – by two orders of magnitude!



# Four-side Cleaving

An example of a device cleaved on all four sides.

*This is what we'd like to make!*



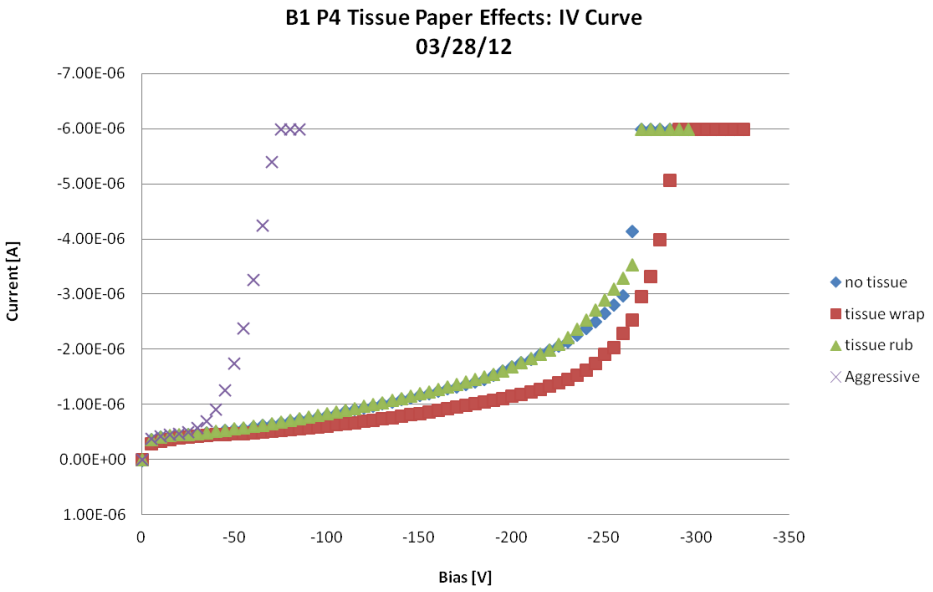

# Irradiation Studies : LANL

**One of the key questions is a performance of the new sidewall technology under irradiation. Work is on-going:**

- **We have irradiated 12 processed strip devices (CIS courtesy A. Macchiolo) at LANL in Dec.**
- **The summary is shown in the table below. Most sensors have breakdown at the pre-rad level or better, but some deteriorated.**
- **A parallel investigation of the robustness of the passivation layer revealed a possible susceptibility to rough handling. It is unclear if this has affected the irradiation results.**
- **In the future we will add ~1 um parylene coating on top of sidewall passivation. This should allow better handling and mounting options.**

| | **Before Irradiation** | **After Irradiation** | | |
|---|---|---|---|---|
| Sensor | V(break) at ~10 uA | V(break) at ~100 uA | Fluence | No Guard Rings |
| B1 P5 | 30 | 460 | 10^13 | 1 |
| B1 P6 | 290 | 165 | 10^13 | 1 |
| B2 P1 | 410 | 80 | 10^13 | 3 |
| B1 P8 | 15 | 90 | 10^14 | 5 |
| B2 P10 | 310 | 80 | 10^14 | 5 |
| B2 P6 | 390 | 100 | 10^14 | 1 |
| B2 P8 | 300 | >800 | 10^15 | 4 |
| B2 P9 | 310 | 335 | 10^15 | 5 |
| B2 P11 | 250 | >800 | 10^15 | 2 |
| B2 P2 | 305 | 390 | 10^16 | 1 |
| B2 P3 | 340 | 330 | 10^16 | 3 |
| B2 P4 | 380 | 425 | 10^16 | 3 |

**Characterization of CIS sensors before and after irradiation.**
**Sensors with breakdown deterioration are marked by reddish color.**

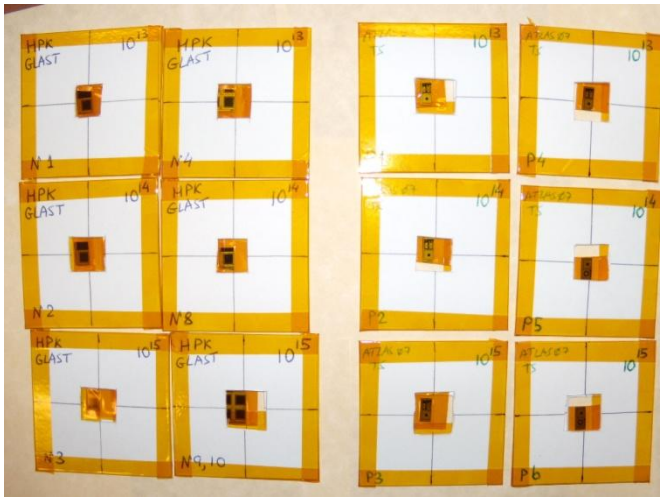


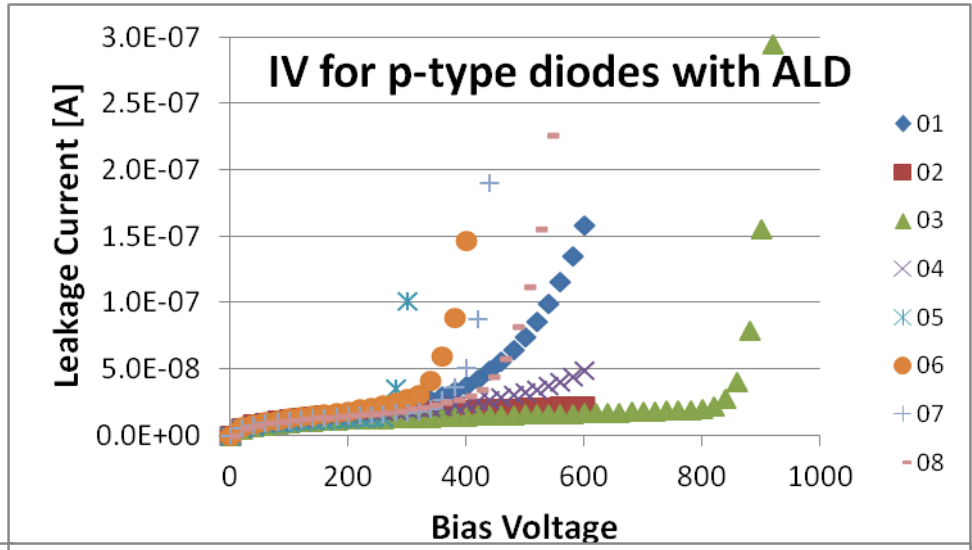

**Exercise with sidewall passivation handling.**

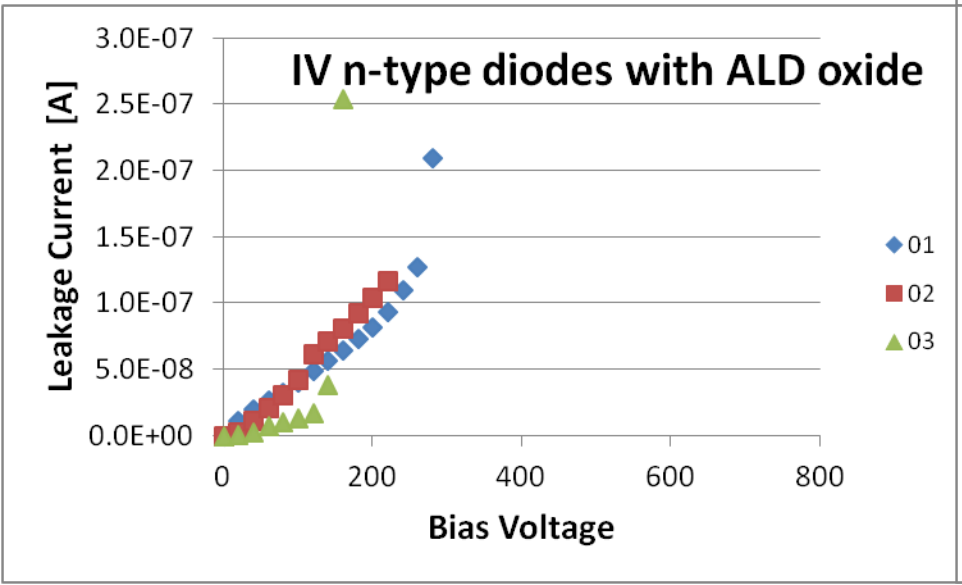
# Irradiation Studies: CERN

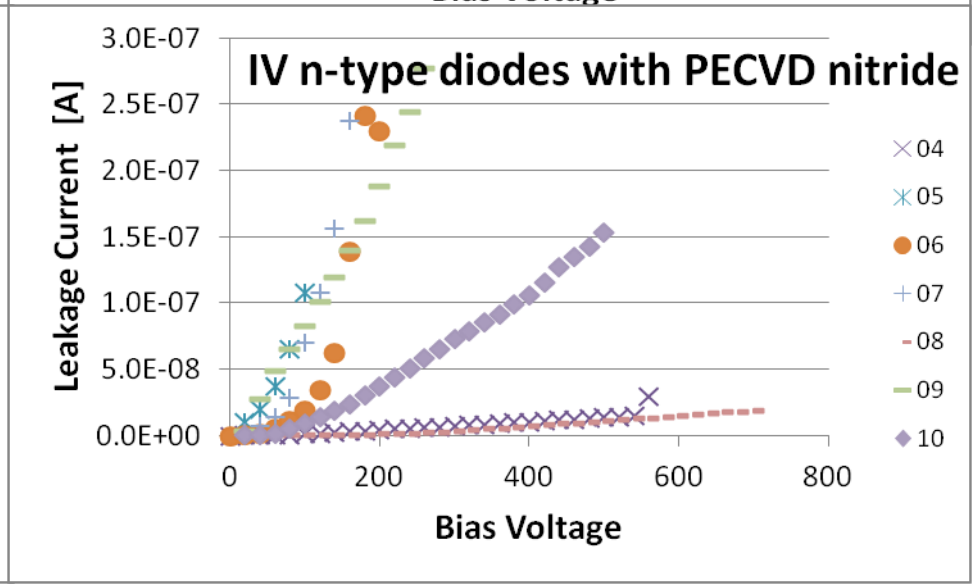
**A new round of irradiations at SPS (help from G. Casse alongside his program):**

- **p-type diodes from ATLAS07 Test Structures**
- **n-type diodes from Fermi/GLAST Test Strucutres, with both PECVD nitride and ALD oxide**



# SCP: RD 50 Common Project

**The initial trials started within the framework of ATLAS Planar Pixel Collaboration.**

**Last summer, the scribe-cleave-passivate (SCP) technology of fabricating slim edge sensors has been approved as RD50 project.**

**The participating institutions are interested in p- and n-type and 3D sensors.**

**We are currently actively working with CNM Barcelona, FBK Trento, MPI Muenchen, UNFN Bari, Ljubljana U., Glasgow U., and TU Dortmund on SCP application to their devices**

**Note that the methods developed are rather generic, applicable to a wide variety of Si devices.**

## RD50 funding request

- Date: *05-26-2011 (Distributed version)*

Development of "slim edges" using cleaving and ALD processing methods

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1. *US Naval Research Laboratory, Bernard Phlips*
2. *FBK Trento, M. Boscardin*

# SCP: RD 50 Matrix

We are very happy to fulfill “slim edge” requests from the RD50 Collaboration

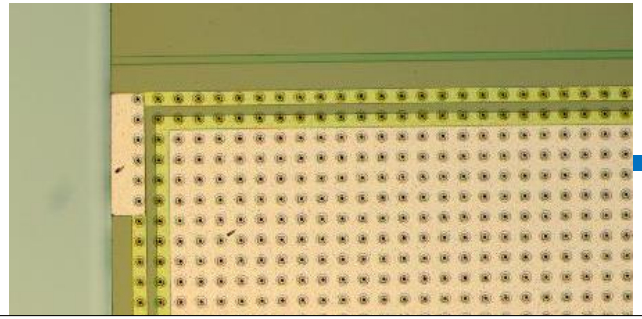
| Institute | Contact Person | Sensors | Status |
|---|---|---|---|
| CNM Barcelona | G. Pellegrini | 3D diodes, strips, pixels | 2nd round of tests ** |
| FBK Trento | G.-F. Dalla Betta | 3D diodes, strips | 2nd round of tests planned |
| MPI Muenchen | A. Macchiolo | P-type planar pixels | In progress** |
| UNFN Bari | D. Creanza | N-type “SMART” detectors | In progress** |
| Ljubljana U. | G. Kramberger | P- and N- type | Devices sent |
| Glasgow U. | R. Bates | P- and N- type | Devices sent, used in precision X-ray scan |
| TU Dortmund | T. Wittig | IBL-style n-on-n sensors | Initial tests done, Iterations with IBL sensors |

**In these instances we are limited by the available margin around the device and performance of the “tweezers” technique. Automated cleaving machines should work better.

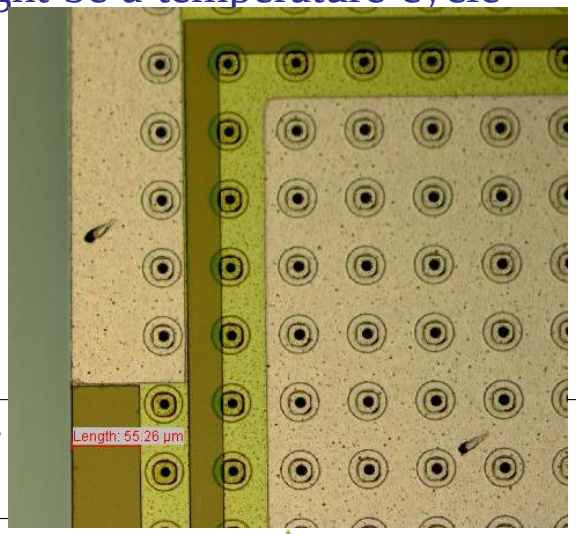
# CNM 3D Sensors: p-type (Alumina Passivation)

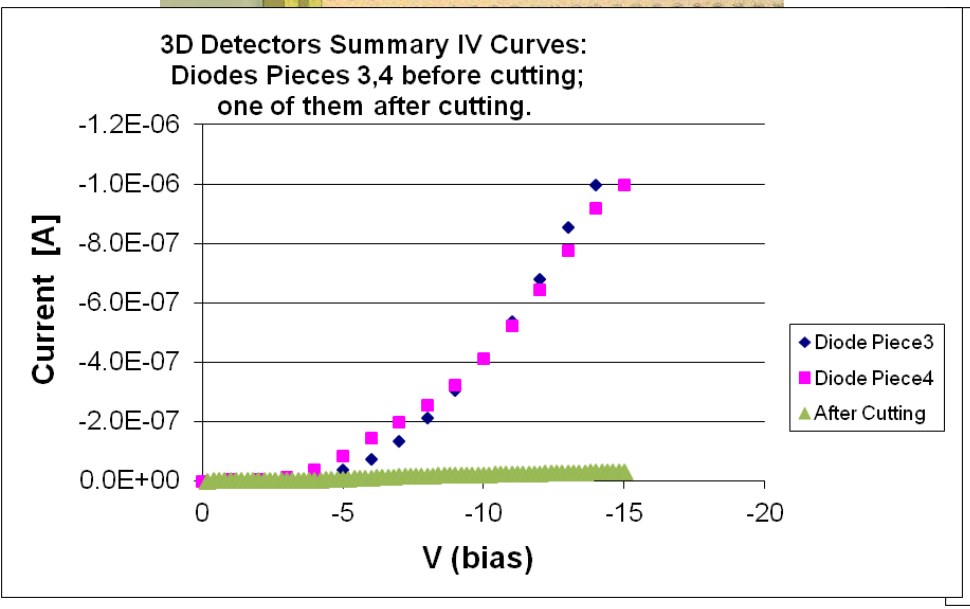
This is 3D diode fabricated by CNM. It was cleaved at 55 um away from GR.

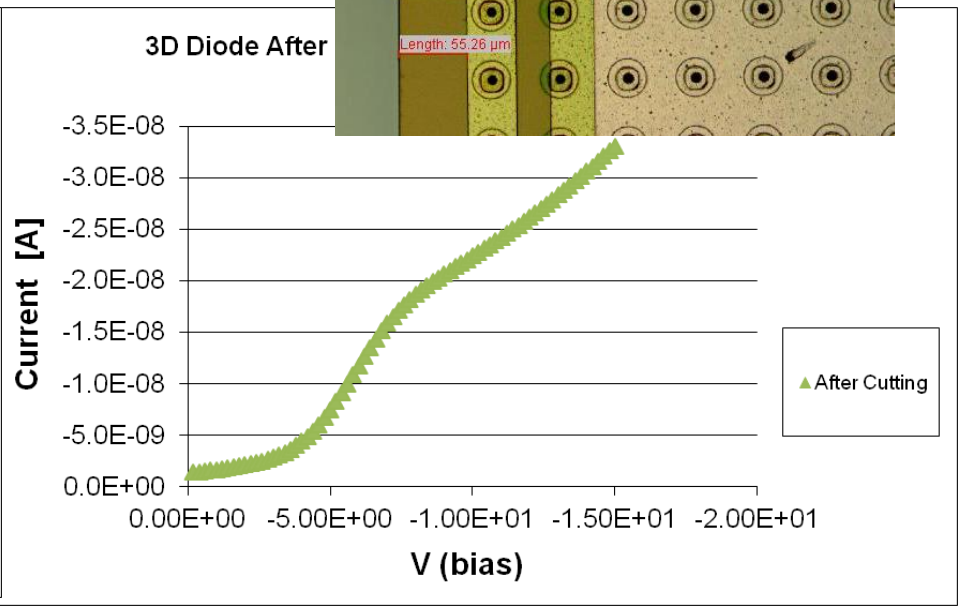
As a result of the scribing, cleaving, and ALD deposition of alumina, the current seems to *improve* a lot. The exact cause is unknown. It might be a temperature cycle post-ALD.



Zoom in



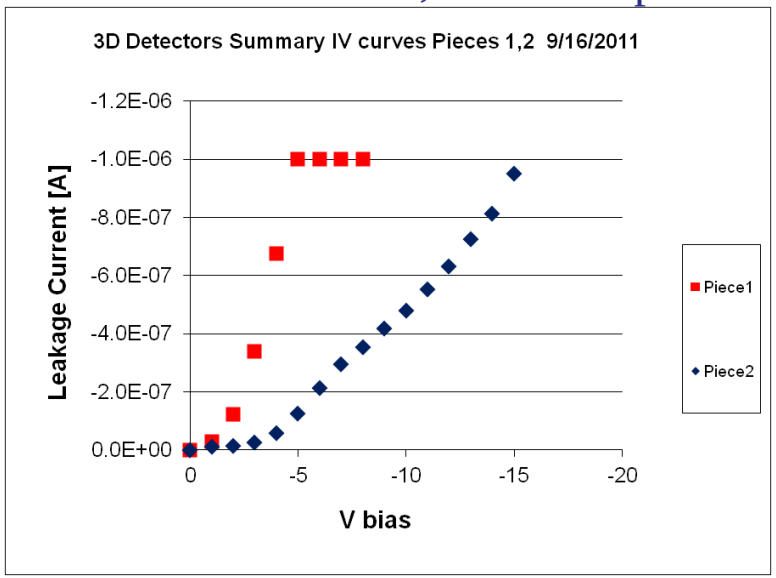



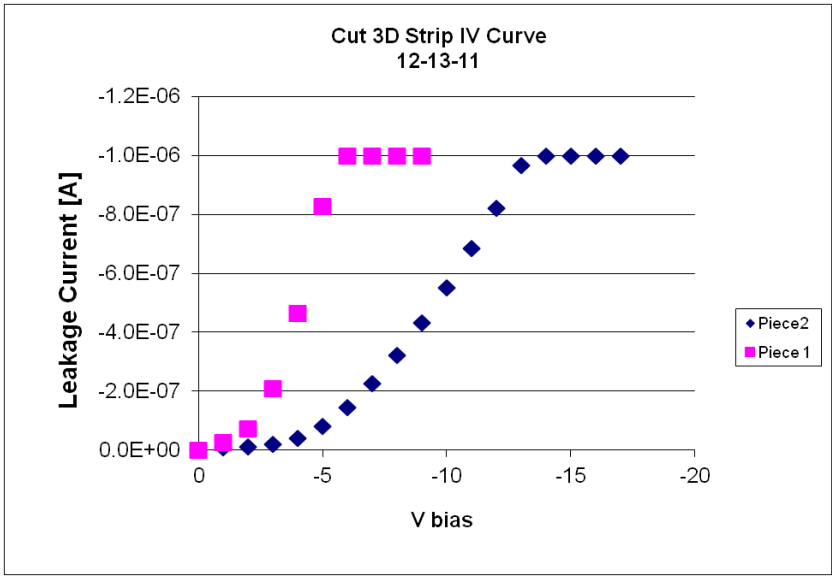

**Comparison of before and after cutting**

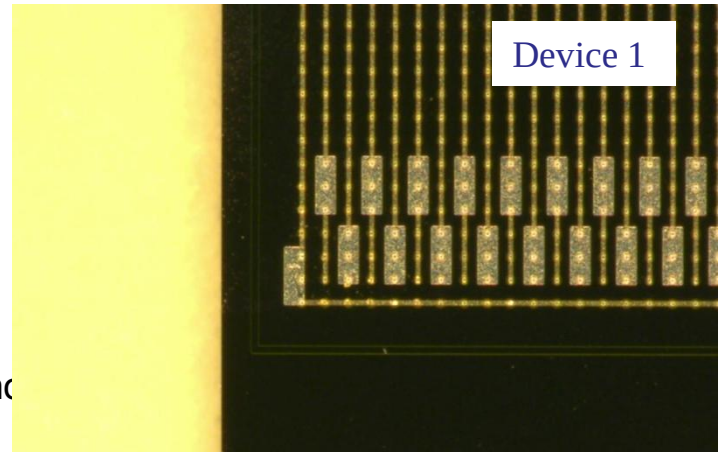
**After cutting alone (note different scale).**

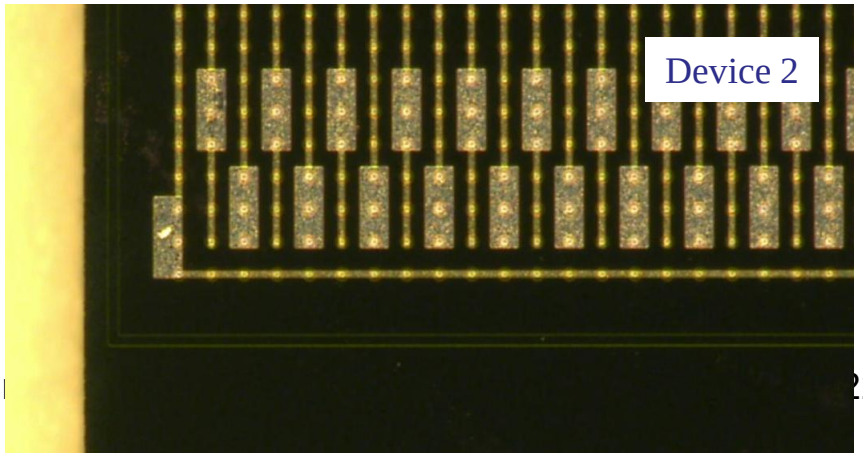
# CNM 3D Sensors: p-type (Alumina Passivation), Cont.

- A more typical scenario is no change after slim edge processing, as shown here for two strip sensors.
- There is a next round of processing in progress, with different devices: FE-I3, FE-I4 for AFP detector, also Medipix devices.



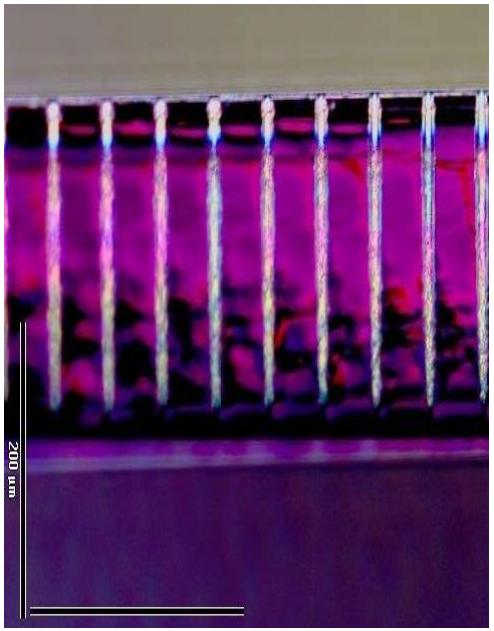



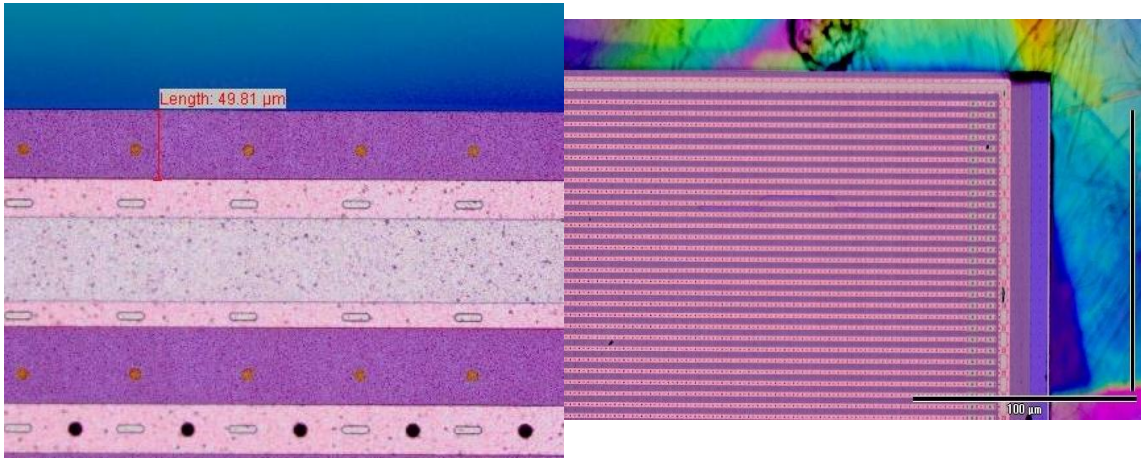



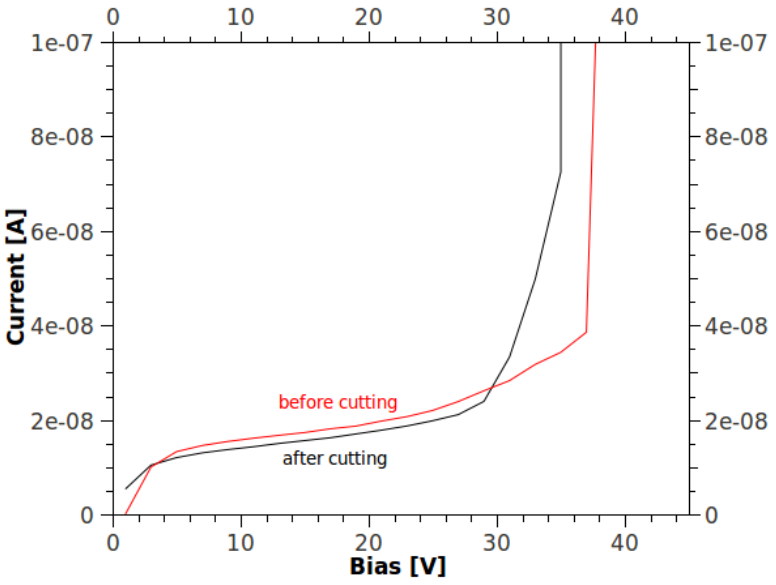
# FBK 3D Strip: p-type (Alumina Passivation)

Cleavage plane "follows" row of "guard fence" holes.

Cleavage plane remains parallel to strip (length of device).



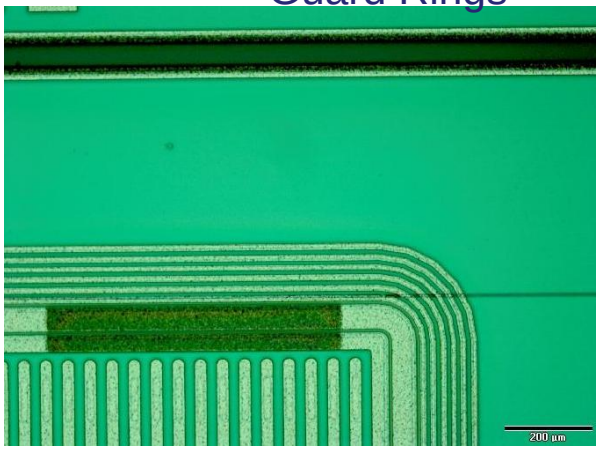



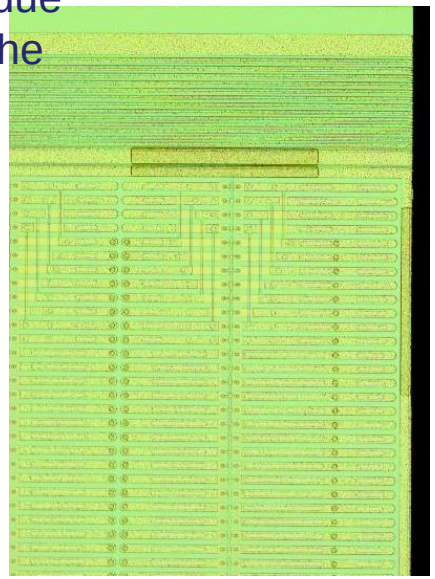




**No change in leakage current due to SCP slim edge (50 µm distance from cut to guard)**

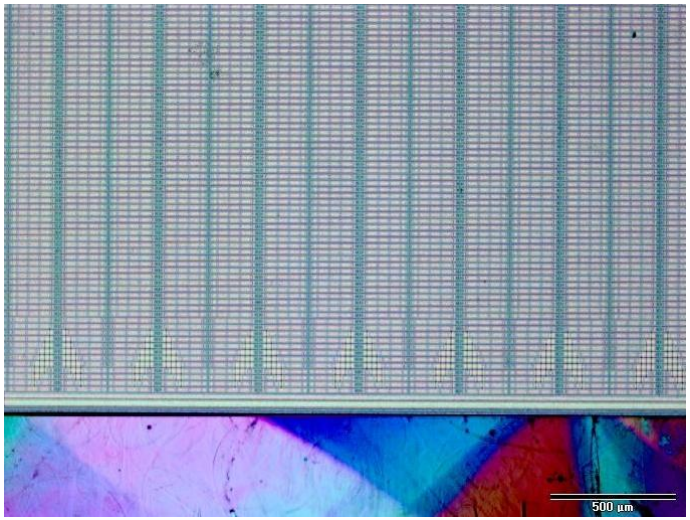
# MPI Devices

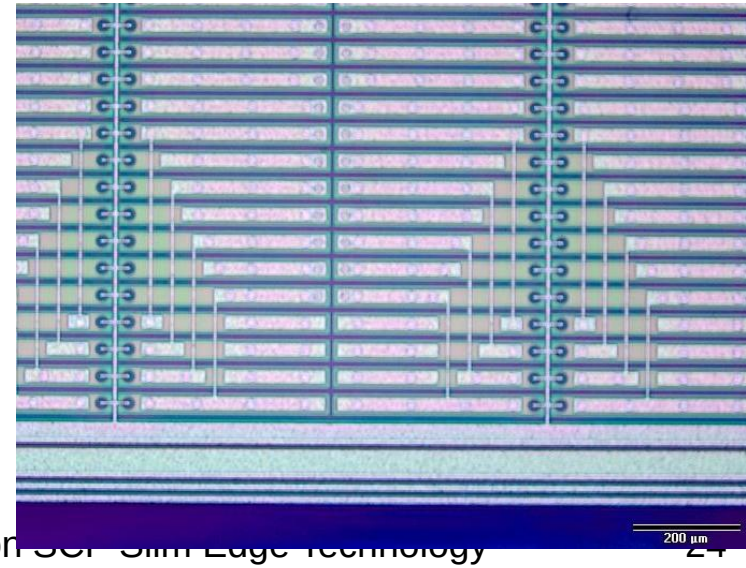
Initially had issues with post-processing etch-scribing, due to presense of metal on the Guard Rings

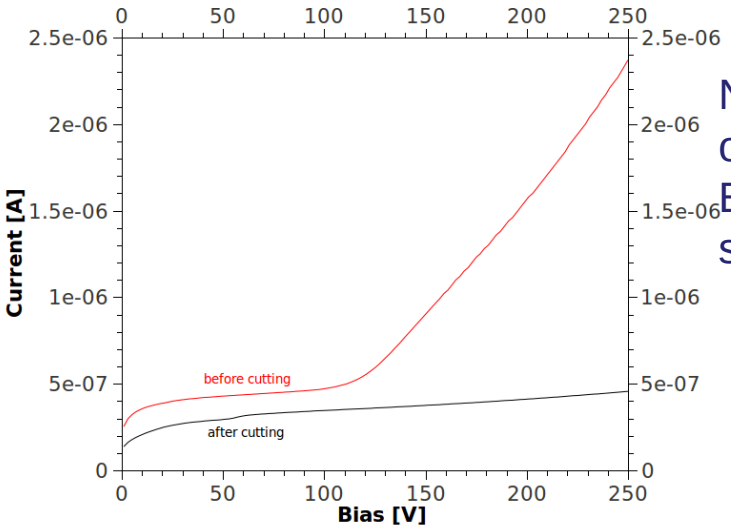


The scribing issue was later solved:



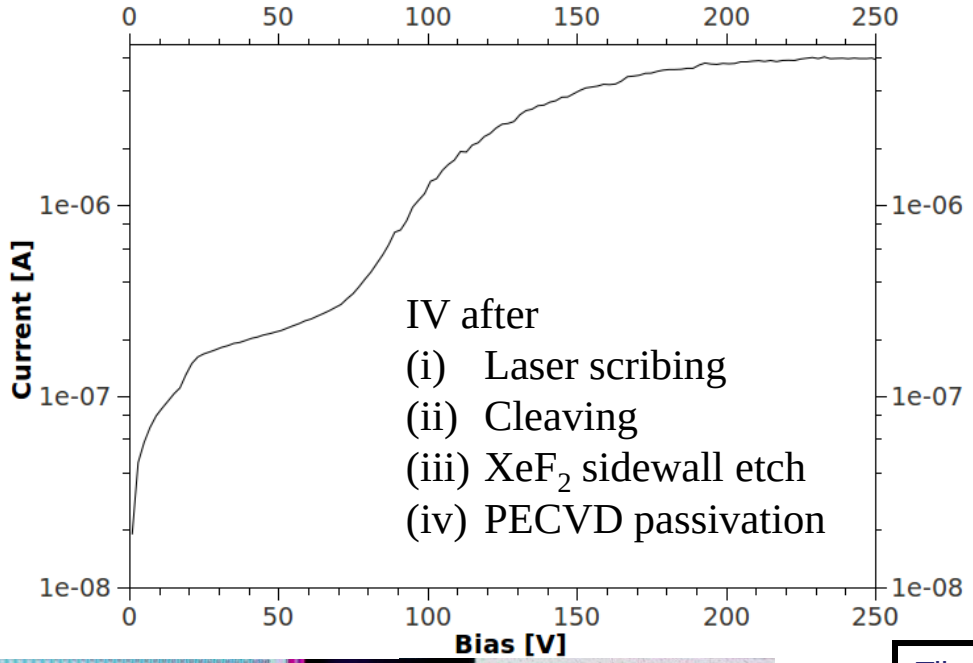




No Guard Ring on one end
But the sensor is still working!

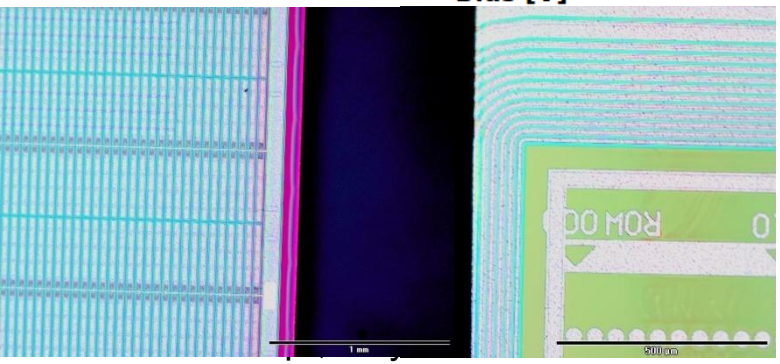
# Dortmund Devices (n-on-n)

Sensors from IBL runs, a special batch with 100 wafers. Would like to find out how SCP would work, and to make samples for irradiations.

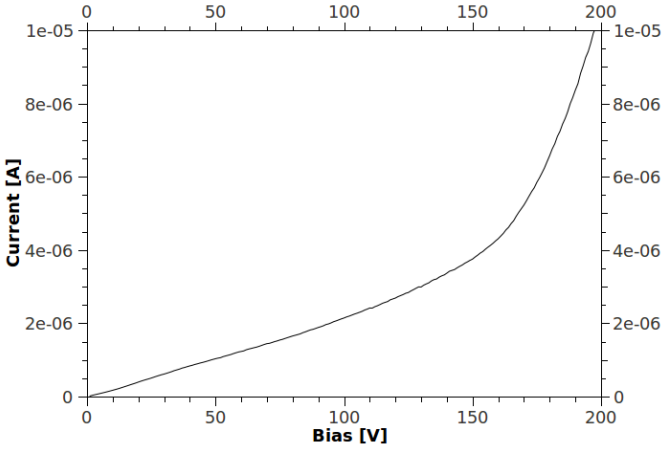
## Laser-scribed device

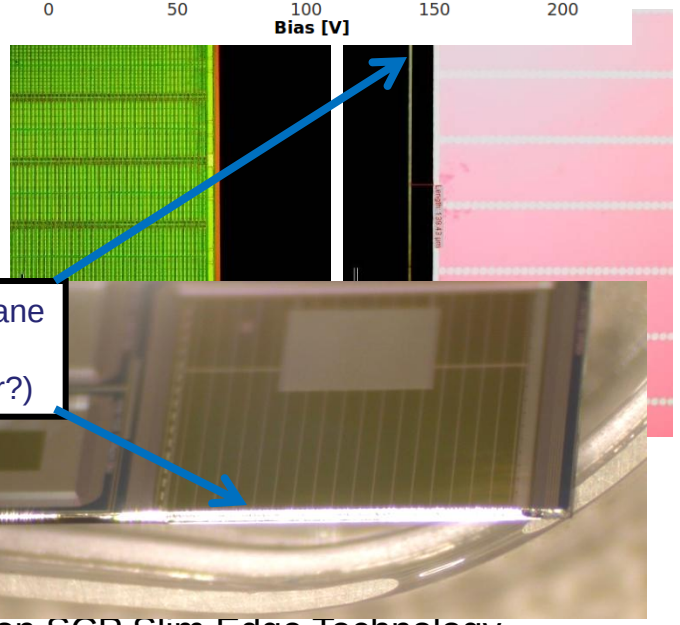



IV after
(i) Laser scribing
(ii) Cleaving
(iii) $XeF_2$ sidewall etch
(iv) PECVD passivation



## Etch-scribed device

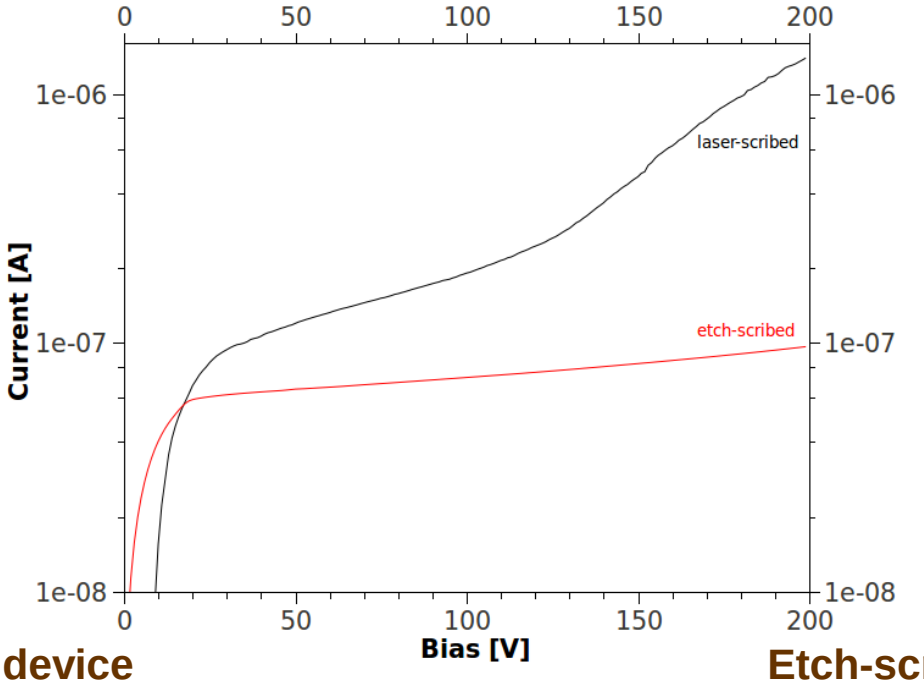


Tilted cleaving plane (Due to stress from nitride layer?)

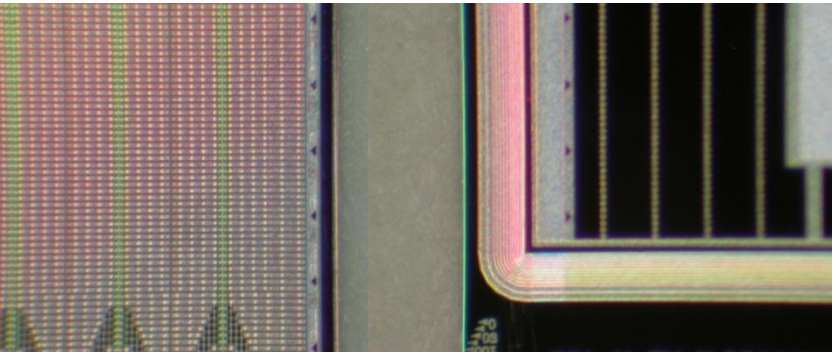
# Dortmund Devices (n-on-n), Cont.

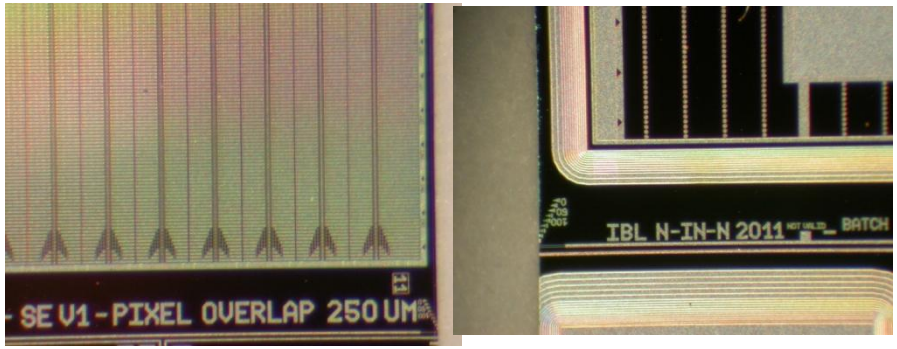
Devices cut outside GR: etch-scribing works better, no issues with cleaving.




**Laser-scribed device**

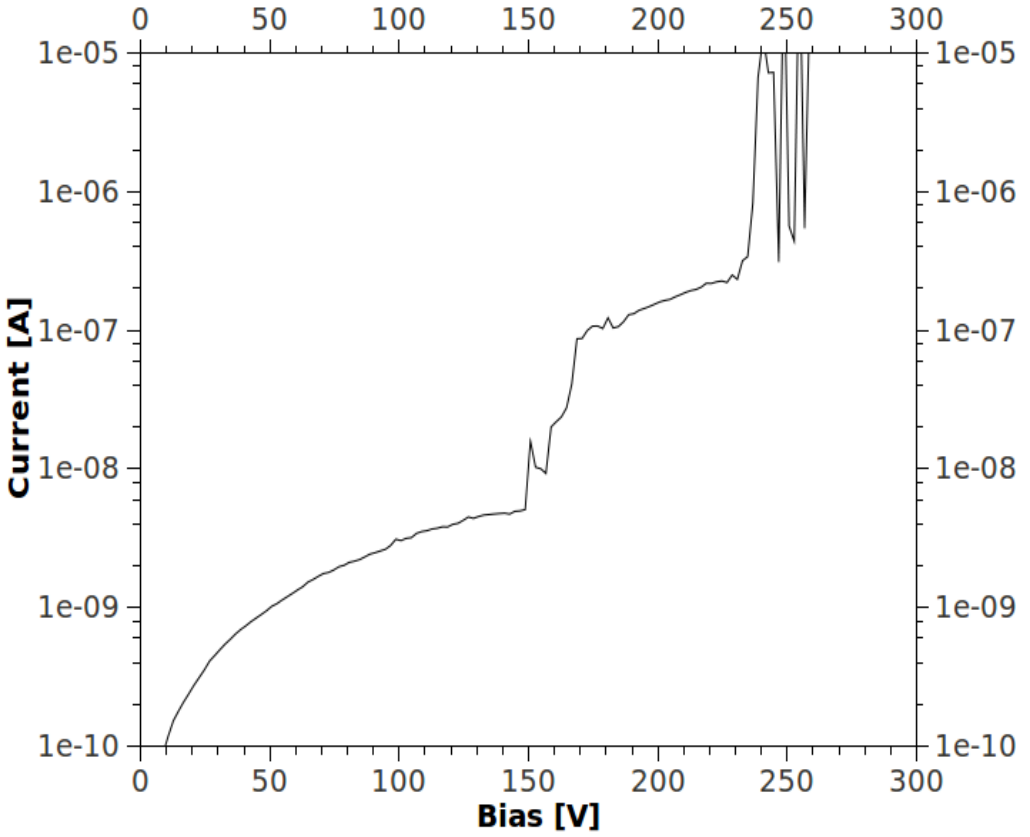
**Etch-scribed device**





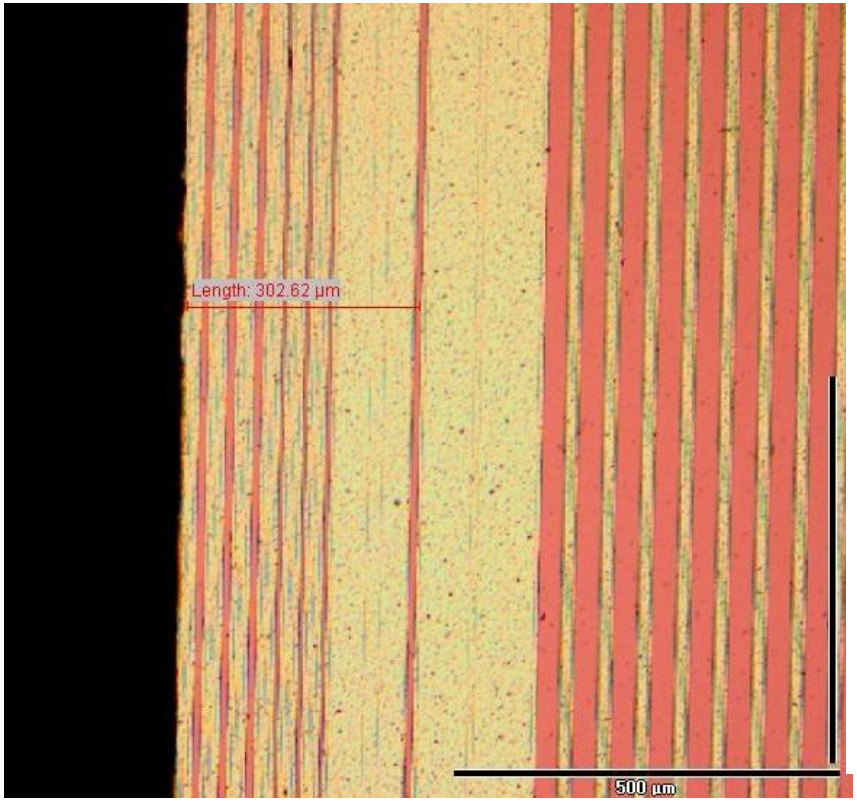
# Narrow Edge Limitation

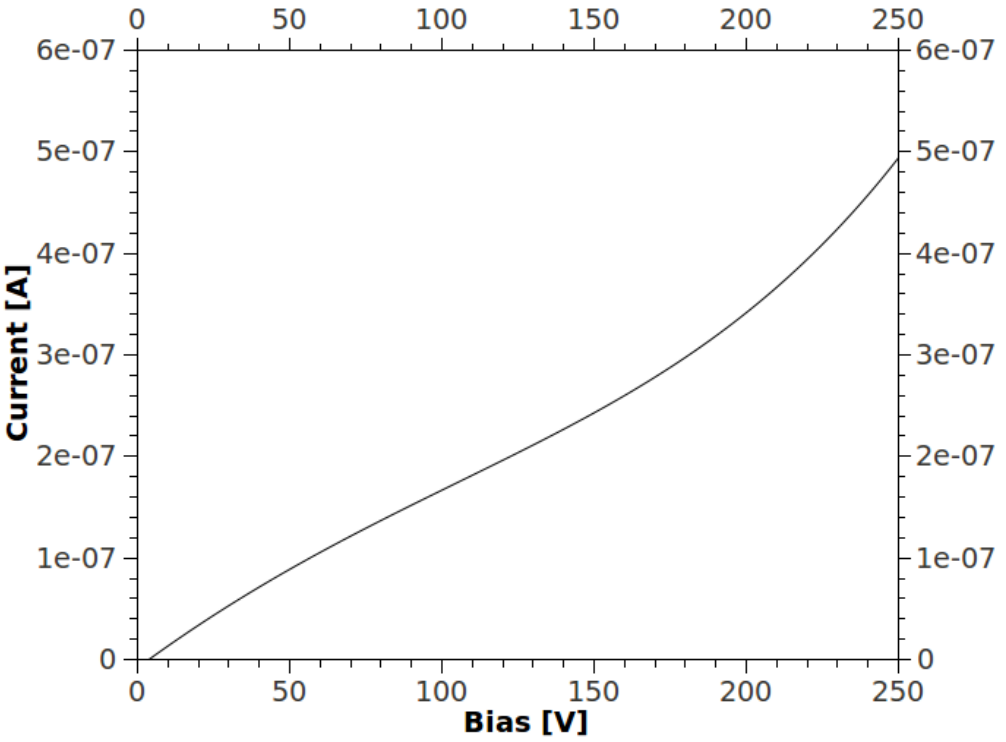
We had difficulty cleaving sensors when the width of removed material is not much larger than the device thickness. This impeded progress on some of RD50 requests.
These issues can be addressed with the existing “building blocks”:
1) (deep) laser scribe, 2) tweezer cleaving, 3) damage removal, 4) passivation.
The laser scribe has to be deep in this case, which is not ideal, but it works, as shown in the example below: 11x6 cm^2 early GLAST prototype sensor without the passivation.

# SMART Sensors from Bari

P-on-n SMART sensors from Bari had the same issue of small width of material to be removed.
The technique of using higher laser power was also used in this case.
No sidewall passivation was applied in this case. However, the sensor is clearly alive.



# Conclusions and Future Work

- Scribe-cleave-passivate (SCP) method of making a slim edge device holds a lot of promise.
- Work goes on in the framework of PPS and RD50 collaboration.
- The method development continues:
  - Etch-based scribing looks promising
  - For N-type devices, PECVD deposition of nitride/oxide works well
  - For N-type devices, ALD deposition of SiO2/Al2O3 nanostack can be a production method
- We have ongoing studies of:
  - Industrialization of the technology – wafer-level automated scribing and cleaving
  - Physics performance: Radiation tolerance, Charge collection
- We are thrilled to perform dedicated studies and service for the community

# Acknowledgements

**We would like to thank the Institute for Nanoscience (NSI) at the Naval Research Laboratory (NRL) and the NSI staff members.**

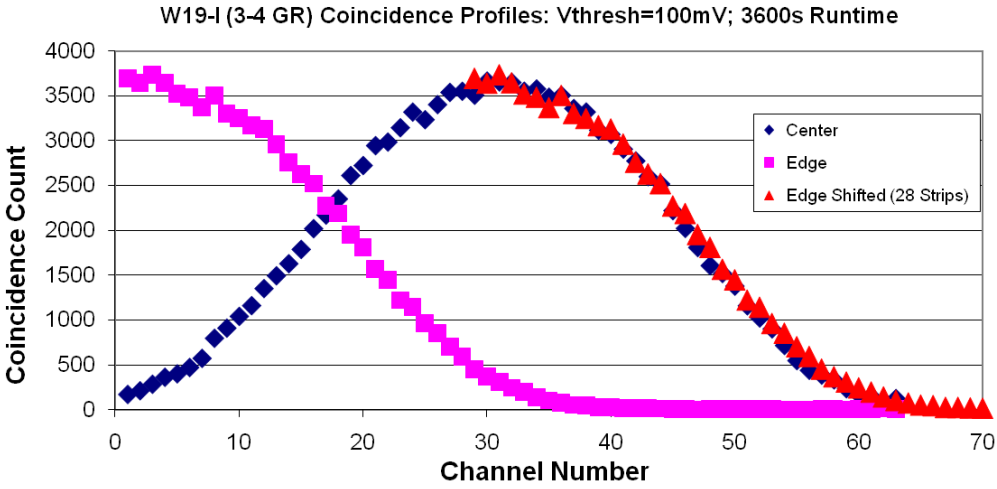
**This work was funded in part by the Office of Navy Research (ONR),
U.S. Department of Energy and National Science Foundation.**

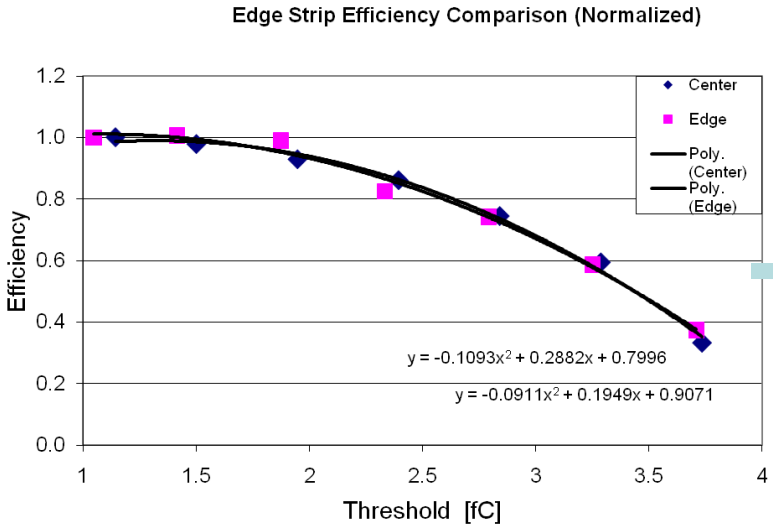
# Back-Up Slides

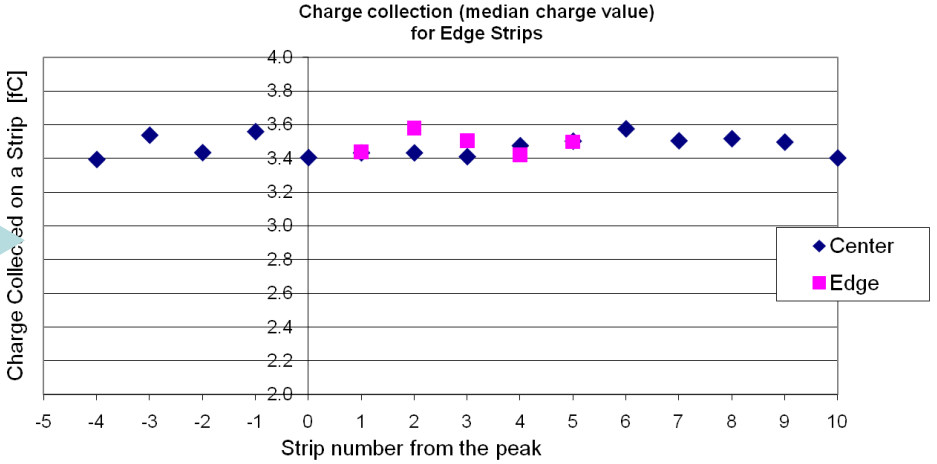
# Charge Collection With Binary Readout System

**We want to make sure that the charge collection near the edge does not suffer because of the slimming.**

- **Consistent beam profiles taken at different positions is an indication of high efficiency at the edge.**
- **By scanning the thresholds we can derive the collected charge on each strip.**
- **We observe the same collected charge at all locations to a few percent on a p-type sensor.**

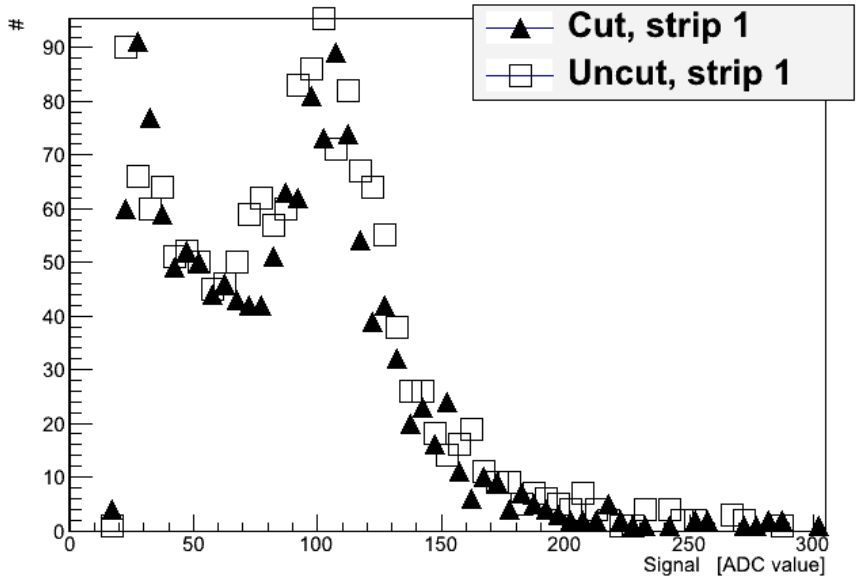


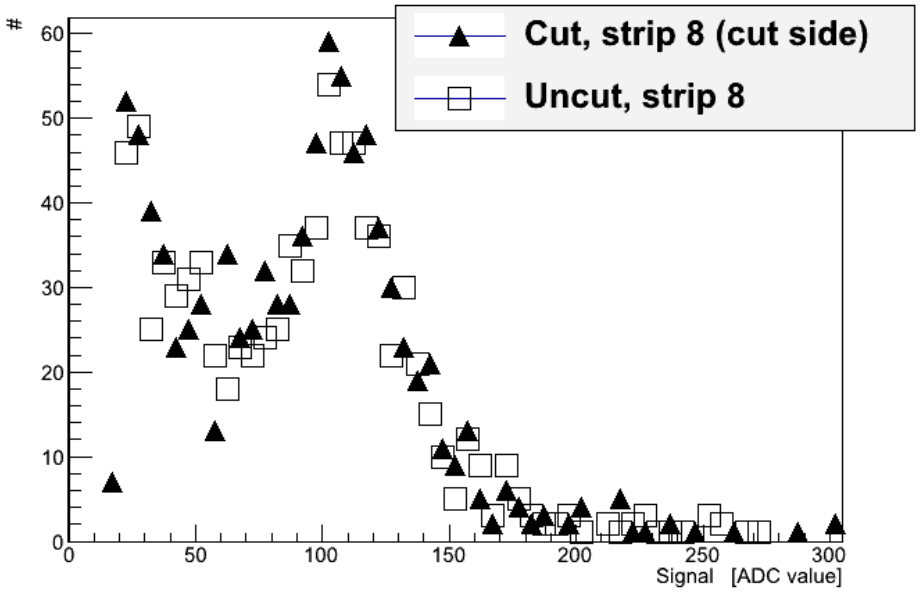



# Charge Collection with AliBaVa

**AliBaVa allows pulse height readout => More direct view of the signal.**
**Data taken and analyzed by R. Mori of Florence.**



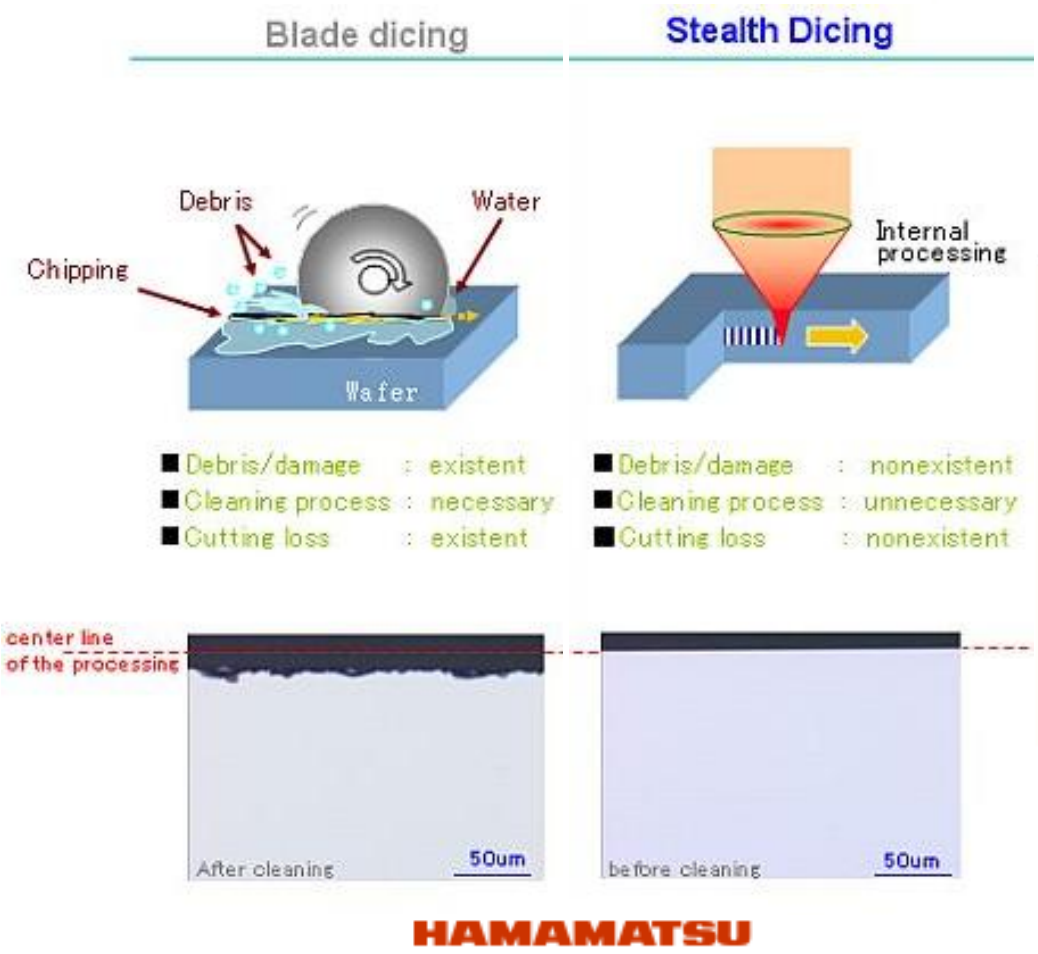

**Edge strips at the normal (wide) edge**

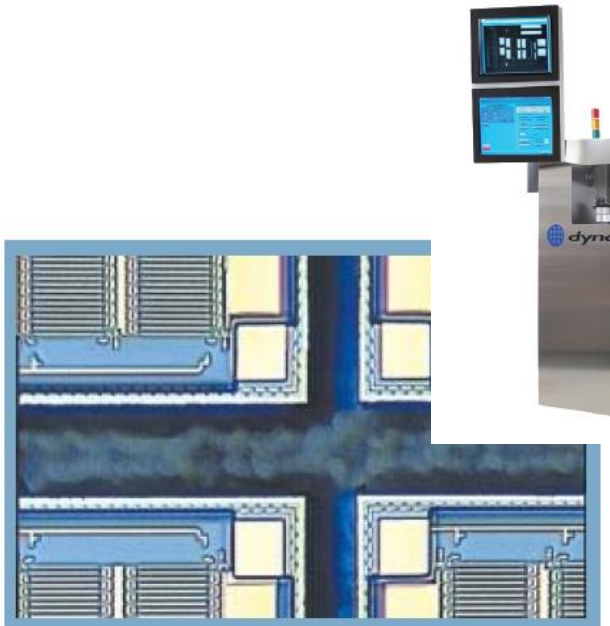



**Edge strips at the slim (cut) edge**

- **A comparison of the data from two n-type Fermi detectors from HPK, one after slim edge processing, another without. The cut is 100 um from the GR.**
- **The pulse height for the "outer" strip (closest to the edge ) might be less by about 4%. The low-side tail is due to absence of neighbor for clustering.**

# Industrial Applications of Laser-Scribing & Cleaving



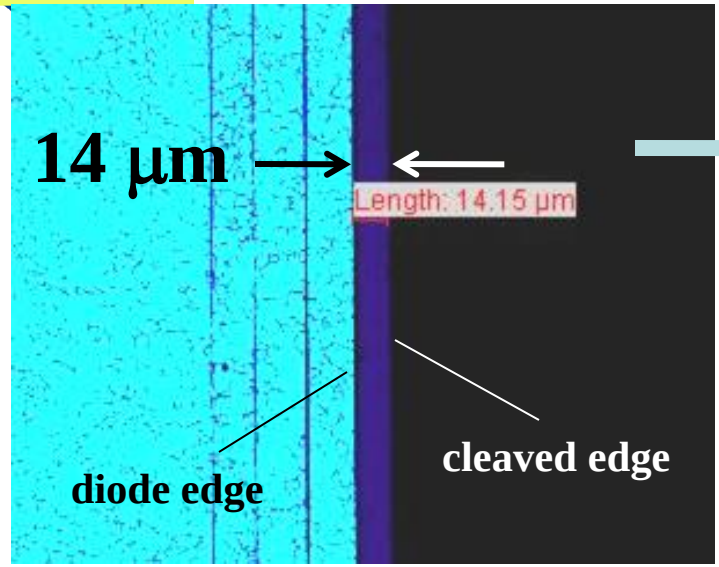



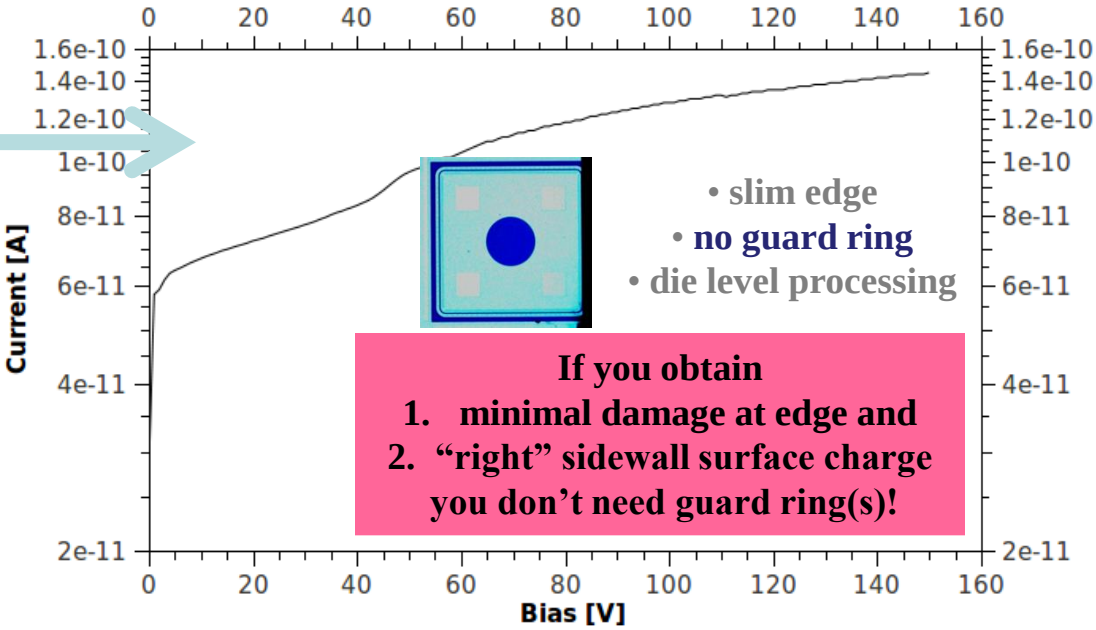

*GaAs wafer, diced and expanded. Wafer dicing is well-suited for UV DPSS lasers with their highly focusable, pinpoint-bright beams*

- laser-scribing and cleaving common in LED industry
- automated tools for scribing and breaking of devices on wafer-scale

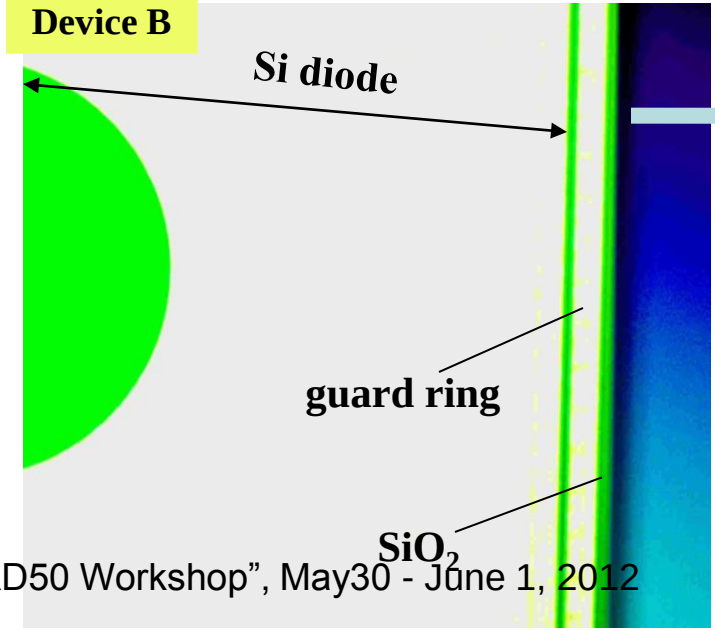
# Examples of Processed Devices

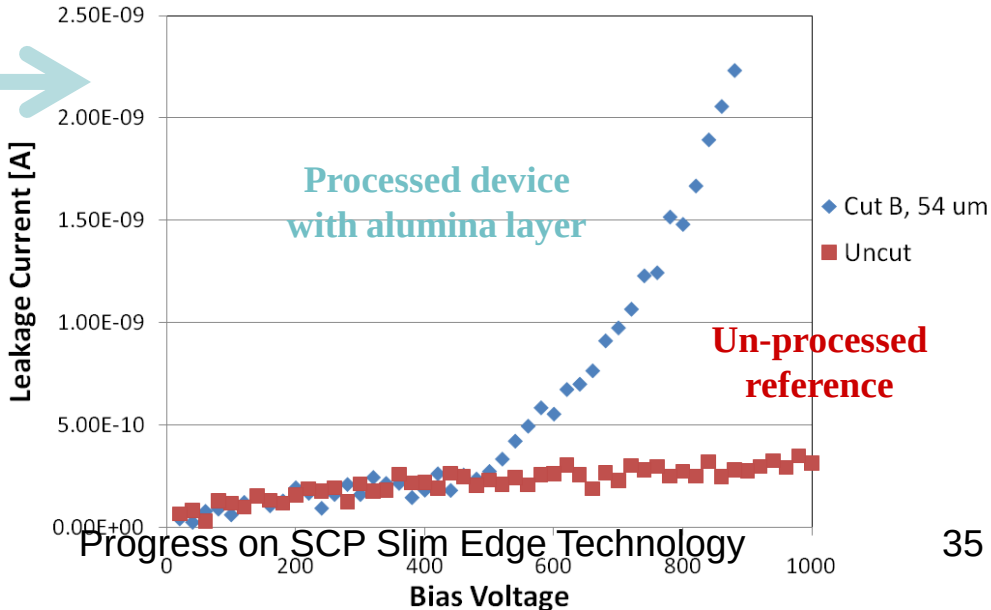
**Device A**



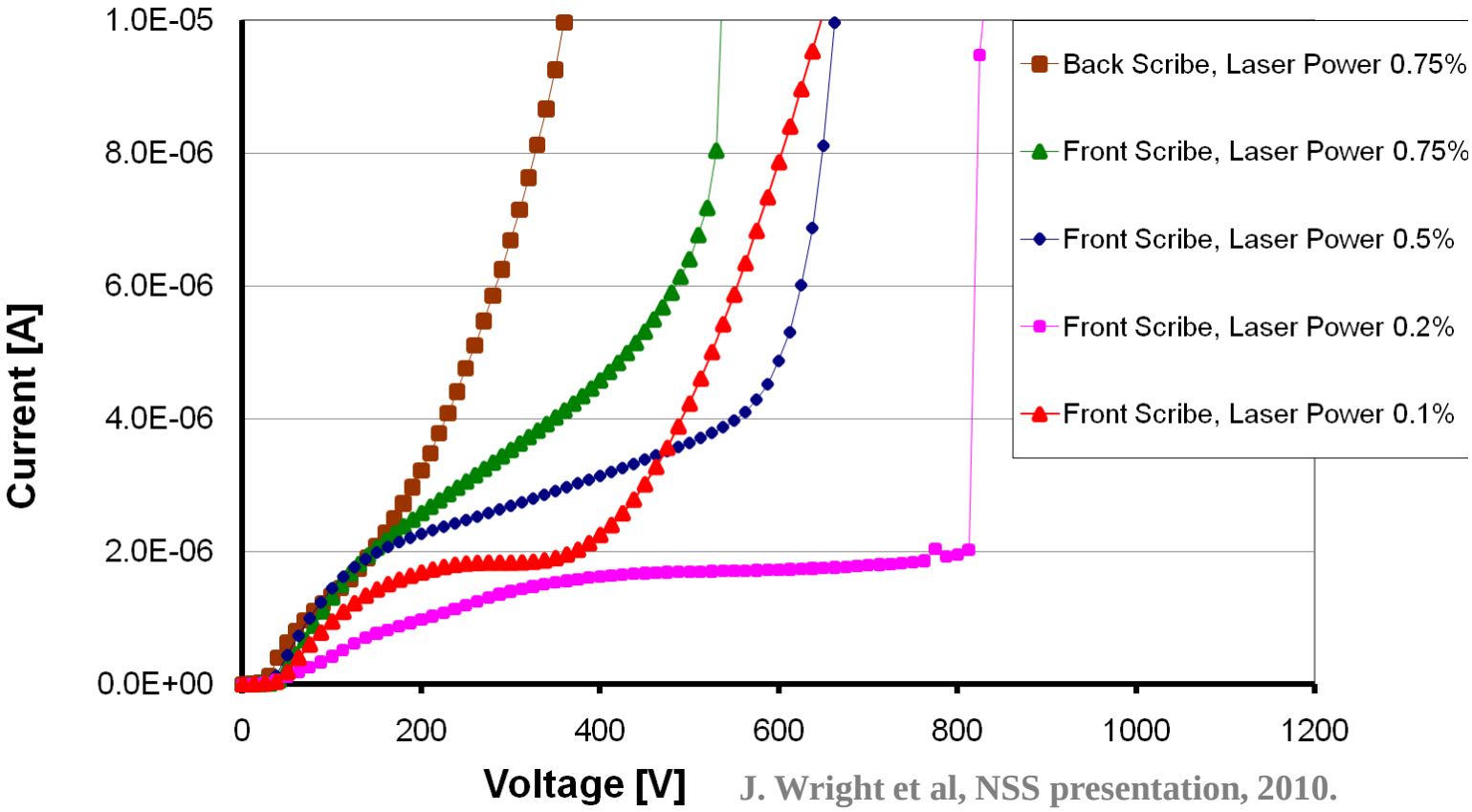




**Device B**



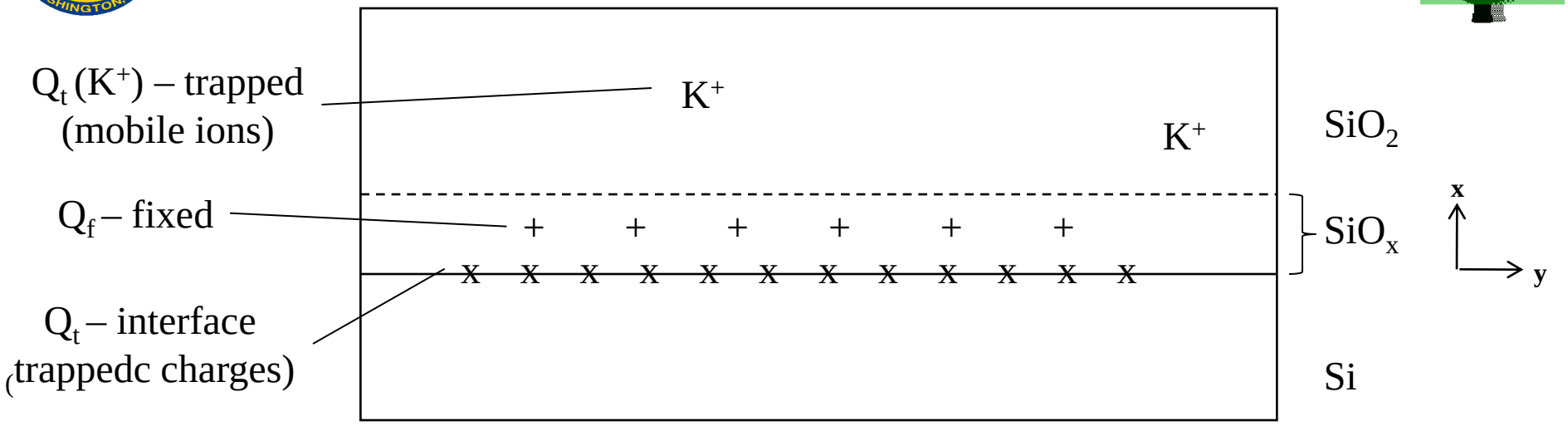
# N-Type Sensor Results – NSS 2010




J. Wright et al, NSS presentation, 2010.

- scribe at 100 um from the guard ring.
- front-side scribe seems to be preferential to back-side one.
- lower laser power is preferential.

# $SiO_2$ – Si Interface Charges




"*Origin*" of excellent passivation for **n-type Si:**

-Thermally grown oxides typically have from ~ $10^{10}$ to 1-2x$10^{11}$ **positive** charges per $cm^2$, localized within about 35 Å of the $Si/SiO_2$ interface [Silicon Processing for the VLSI Era (Vol I), S. Wolf and R. Tauber, Lattice Press 1986, p. 223].

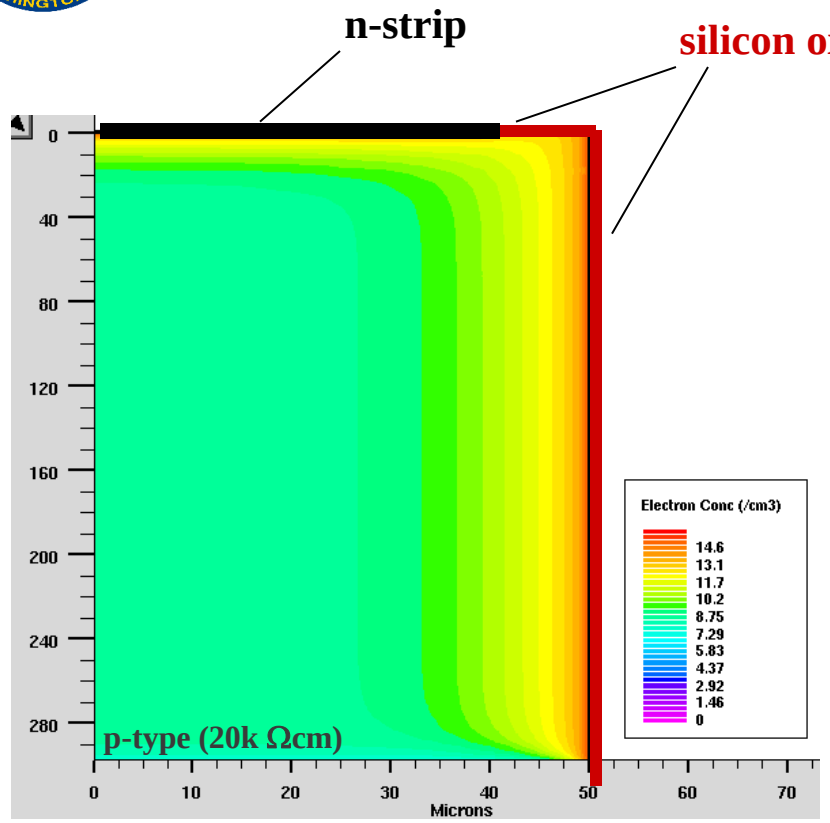
- surface recombination rate: FZ n-type Si (10 Ωcm): ~ 60 cm/s

# Introduction - ALD

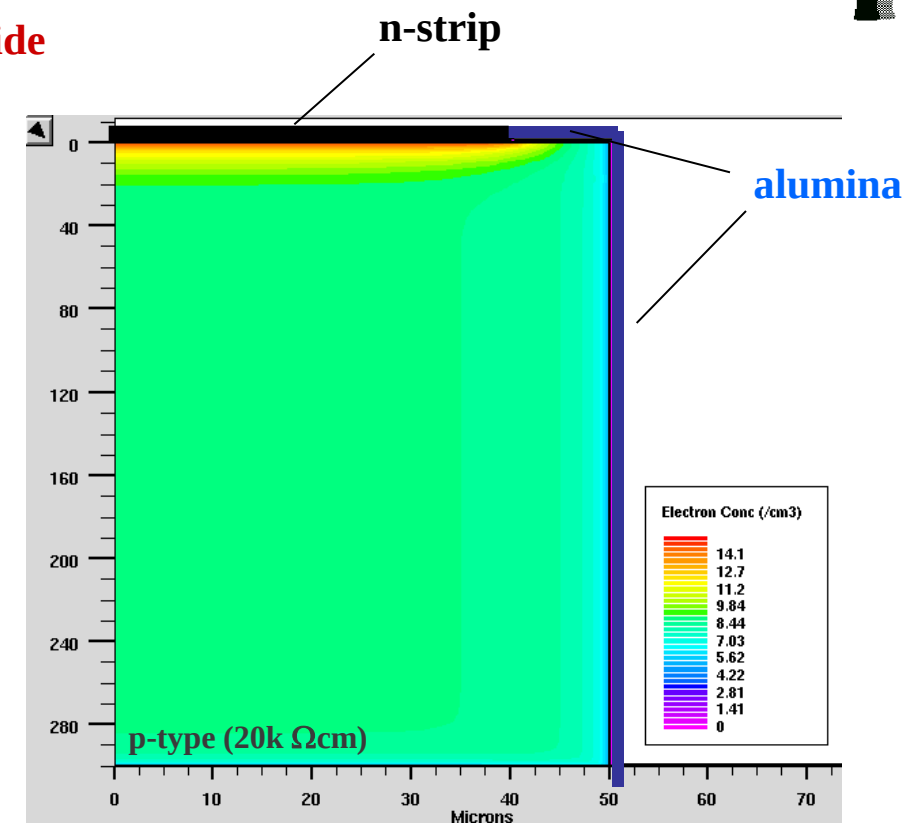
- Similar in chemistry to CVD (chemical vapor deposition), except that the ALD (**atomic layer deposition**) reaction breaks the CVD reaction into two half-reactions, keeping the precursor materials separate during the reaction.
- ALD film growth is **self-limited and based on surface reactions**, which makes achieving atomic scale deposition control possible.
- Perfect 3-D conformality, 100% step coverage: uniform coatings on flat, inside porous and around particle samples.

- **Origin of negative interface charge**: Functional surface groups on the silicon wafer are not optimal for an adsorption of the TMA (trimethylaluminium) precursor molecules, which leads to an incomplete reaction of the TMA and, consequently, an increased relative oxygen concentration at the interface (F. Werner et al., 25th European Photovoltaic Solar Energy Conference, Valencia, Spain, 6-10 September 2010).

# Equilibrium Electron-Concentrations for $SiO_2$ and $Al_2O_3$



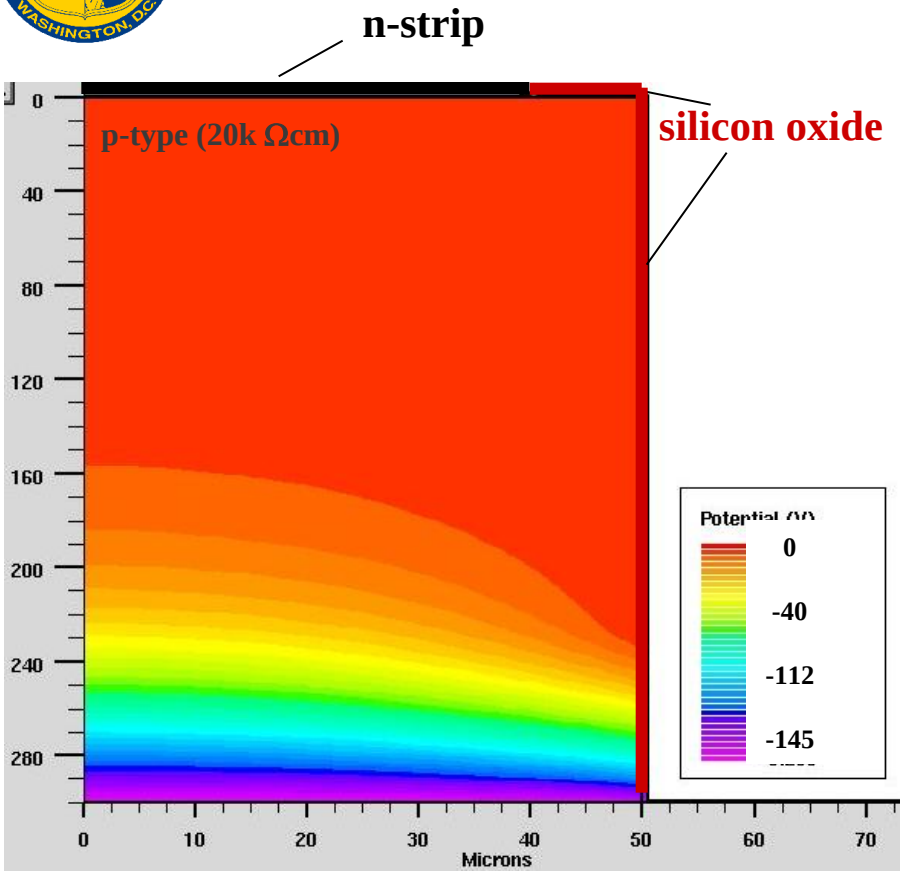

Positive charge (+1E11 $cm^{-2}$), no bias (V=0)



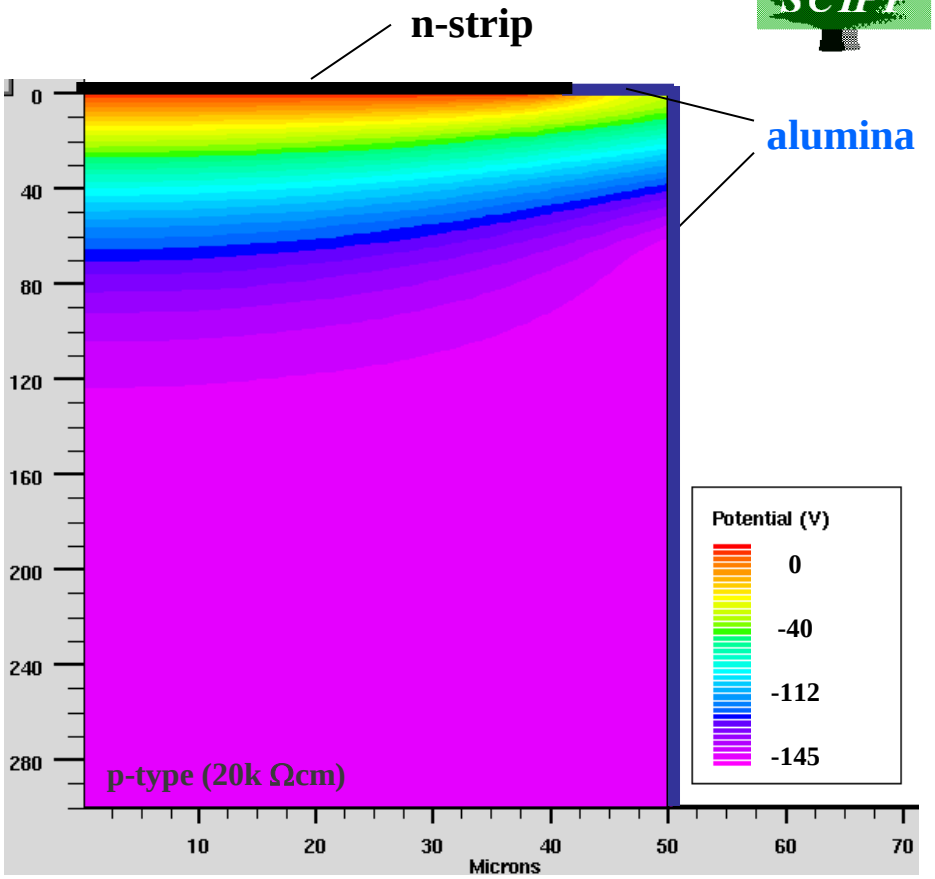

Negative charge (-1E11 $cm^{-2}$), no bias (V=0)

- silicon oxide → electrons path from n-strip to sidewall
- alumina → electrons "pushed away" from sidewall

# Potential Distributions for $SiO_2$ and $Al_2O_3$ Passivation




Positive charge (+1E11 $cm^{-2}$)

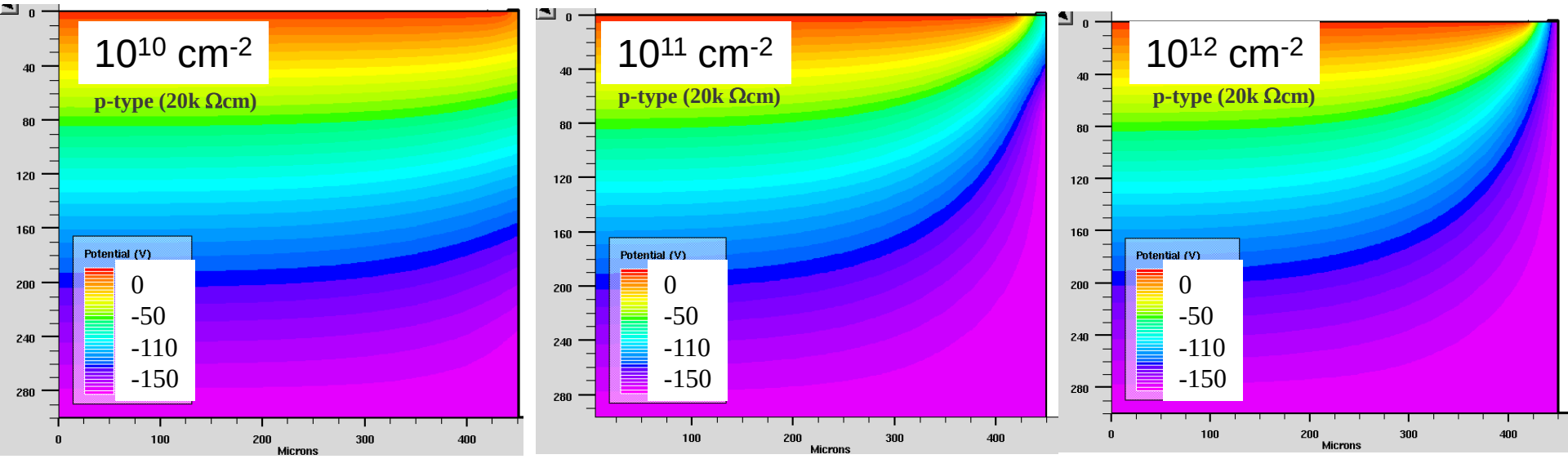



Negative charge (-1E11 $cm^{-2}$)

Oxide passivation leads to:
- high electric field at trench edge,
- no control potential drop towards the cut edge

Alumina passivation leads to:
- high electric field strip edge,
- partially controlled potential drop towards the cut edge.

# Influence of Surface Charge Concentration: P-Si/$Al_2O_3$

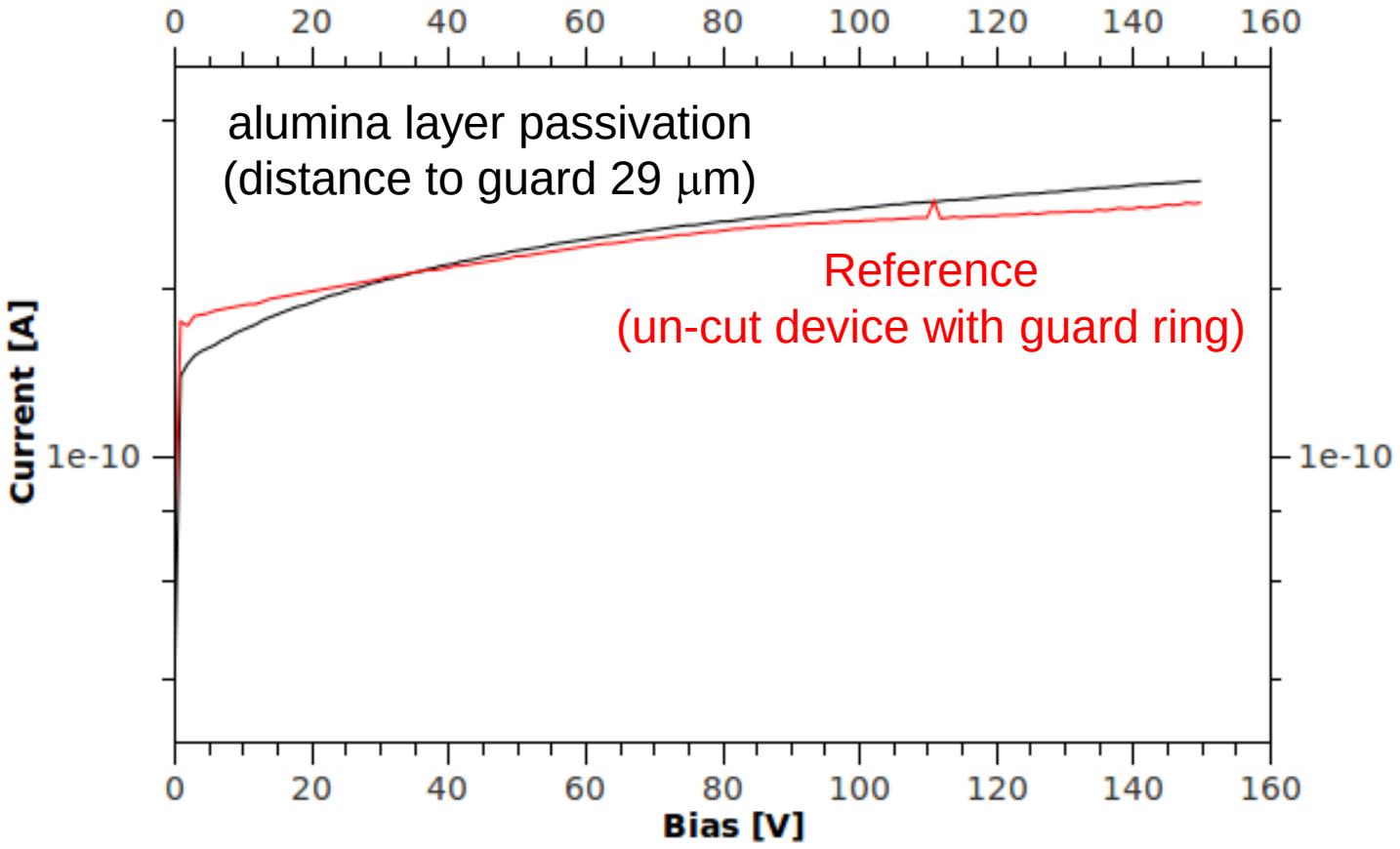



*increasing negative surface charge*

Typical literature values for alumina are ~ $10^{11}$ – $10^{13}$ cm$^{-2}$ depending on deposition conditions. BUT most research is focused on increasing (*not decreasing)* surface charge.

**The potential drop at edge depends strongly on surface charge density.**

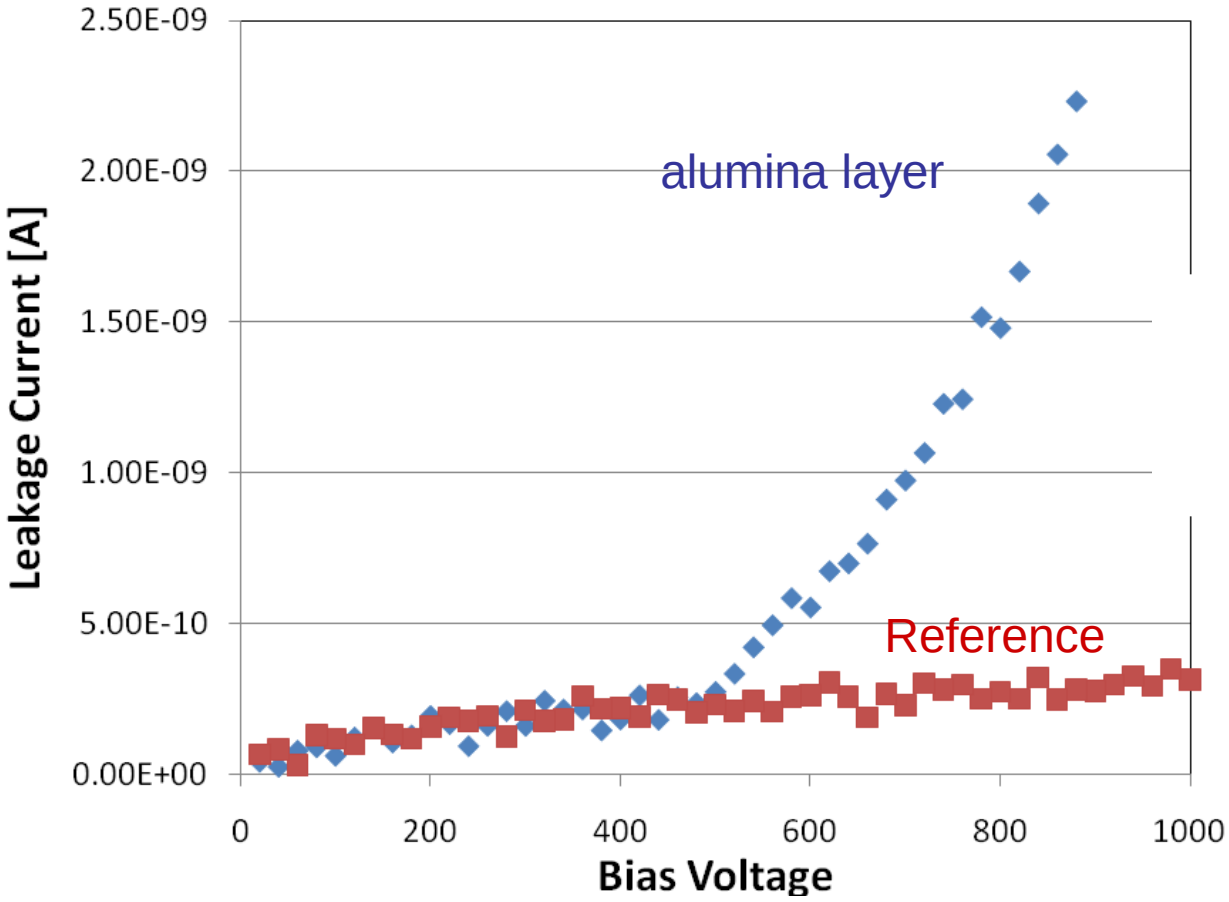
# ALD Alumina Passivation for P-Type Silicon




Leakage for sample with $Al_2O_3$ passivation comparable to un-cut device with full guard ring structure.

**Device I (HPK)**

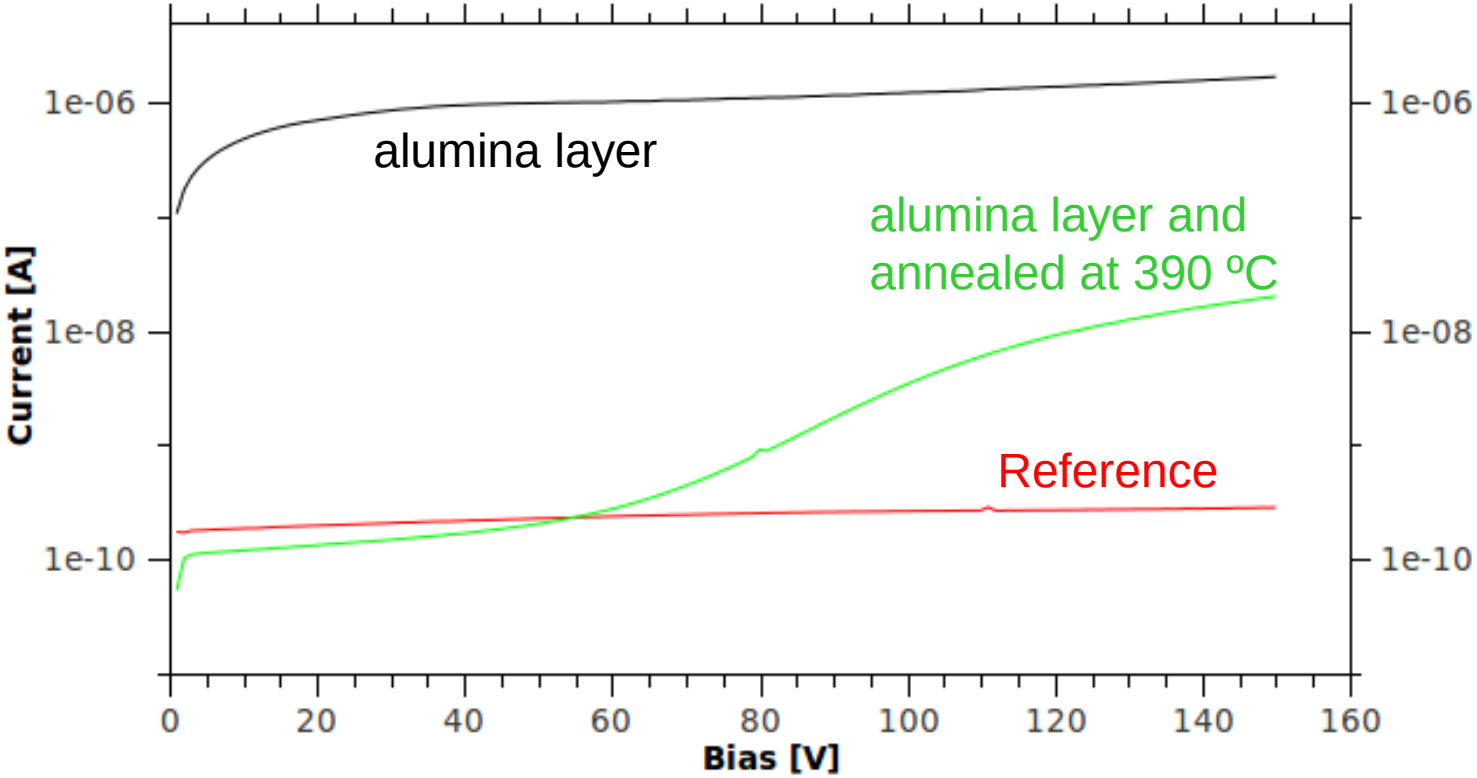
# Low Leakage Currents up to 1,000 V




Leakage is low for voltages up to 1,000 V.

**Device II (HPK)**

# Effect of Annealing and Native Oxide

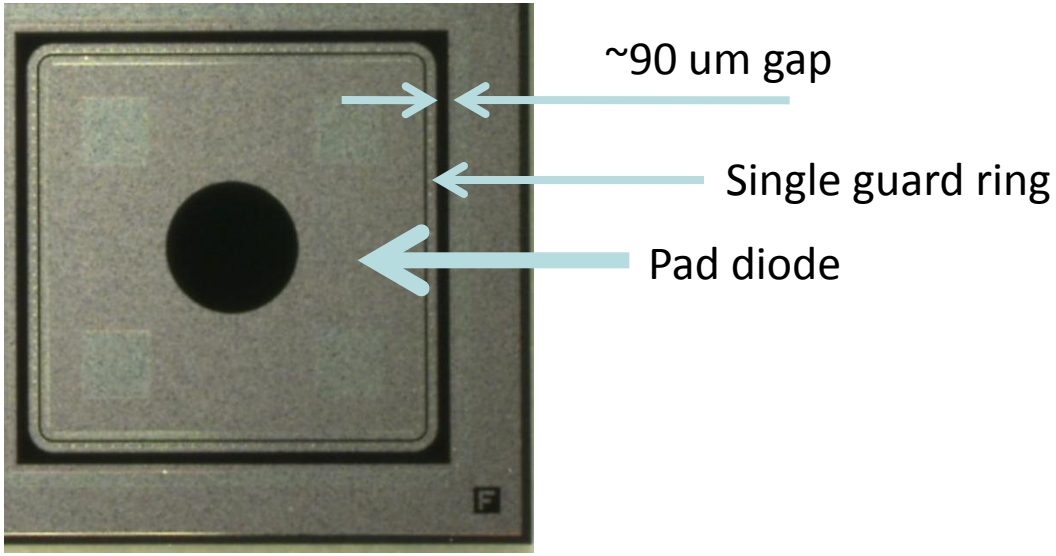



- annealing of alumina layer reduces leakage current (same effect as seen for solar cells, see slide #14 ).
- formation of native oxide (wrong surface charge) ↑ leakage current.
- native oxide forms rapidly (within seconds/minutes) in air.
- native oxide: ~ 2 nm thick, high charge trap density.

**Device III (HPK)**

# Devices I-IV: HPK Samples

- Using a pad diode from HPK test structure meant to provide control over key sensor parameters for ATLAS07 sensors (*).
- It features a classic HPK single-guard ring design.
- Simple DC-coupled n-on-p pad. Vdepl ~ 180 V. Thickness 320 um.




(*) ATLAS07 strip sensors have been developed for ATLAS tracker upgrade for higher luminosity. They served as test vehicle for inter-strip isolation, punch-through protection, and other studies.

References:

Y. Unno et al., “Development of n-on-p silicon sensors for very high radiation environments”, NIM A, doi:10.1016/j.nima.2010.04.080 .

S. Lindgren et al., “Testing of surface properties pre-rad and post-rad of n-in-p silicon sensors for very high radiation environment”, NIM A, doi:10.1016/j.nima.2010.04.094 .

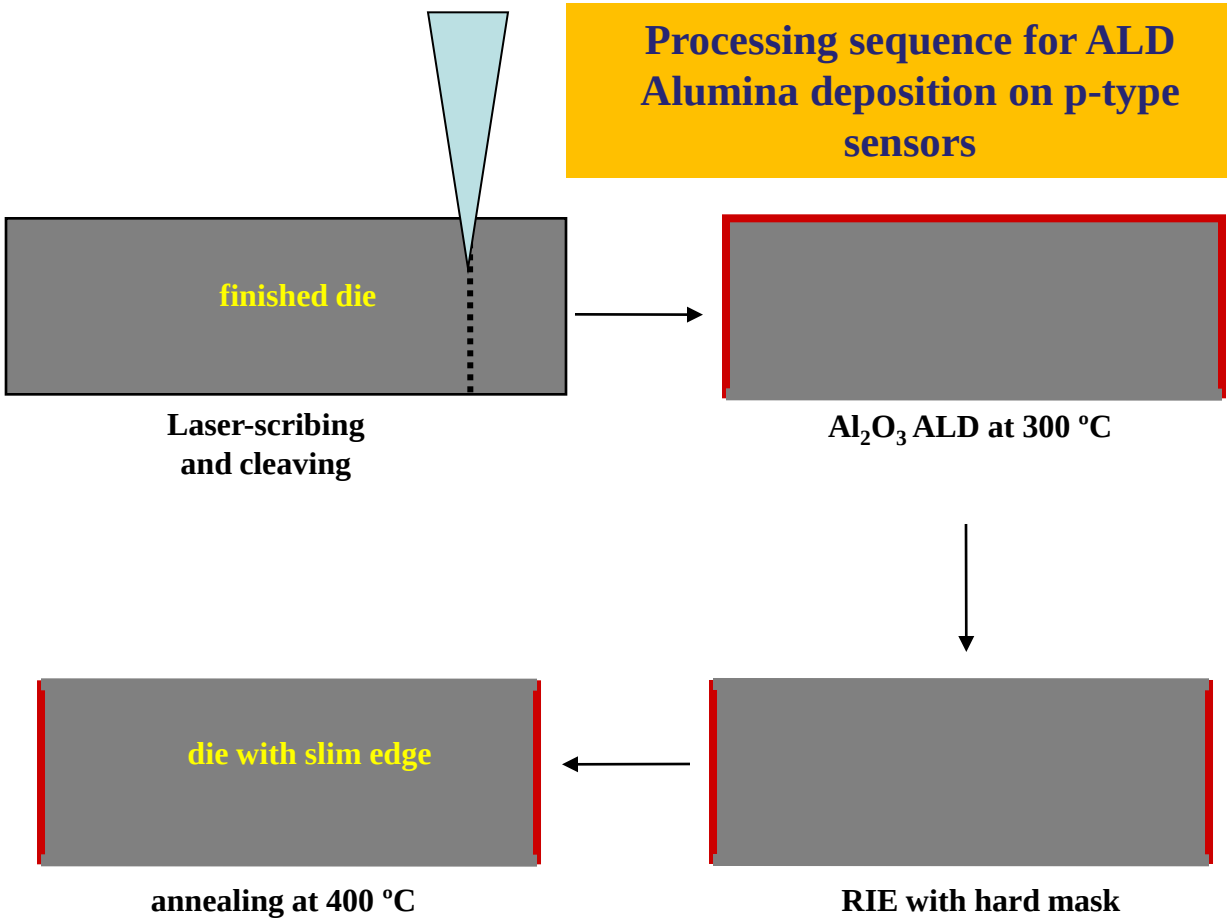
J. Bohm et al., “Evaluation of the bulk and strip characteristics of large area *n*-in-*p* silicon sensors intended for a very high radiation environment “, NIM A, doi:10.1016/j.nima.2010.04.093 .

# Treatment Sequence

**There are three key steps of the process:**
**1) Scribing on front-side**
**2) Cleaving, which leaves the surface with low defect density**
**3) Surface passivation to make the sidewall resistive.**

**N- and p-type devices require different passivation technologies:**
- **For n-type devices one needs a passivation with positive interface charge. Silicon Oxide $SiO_2$ layer works well, Silicon Nitrite $Si_3N_4$ layer works even better.**
- **For p-type material a passivation with negative interface charge is necessary. We found that ALD with Alumina $Al_2O_3$ works in this case.**

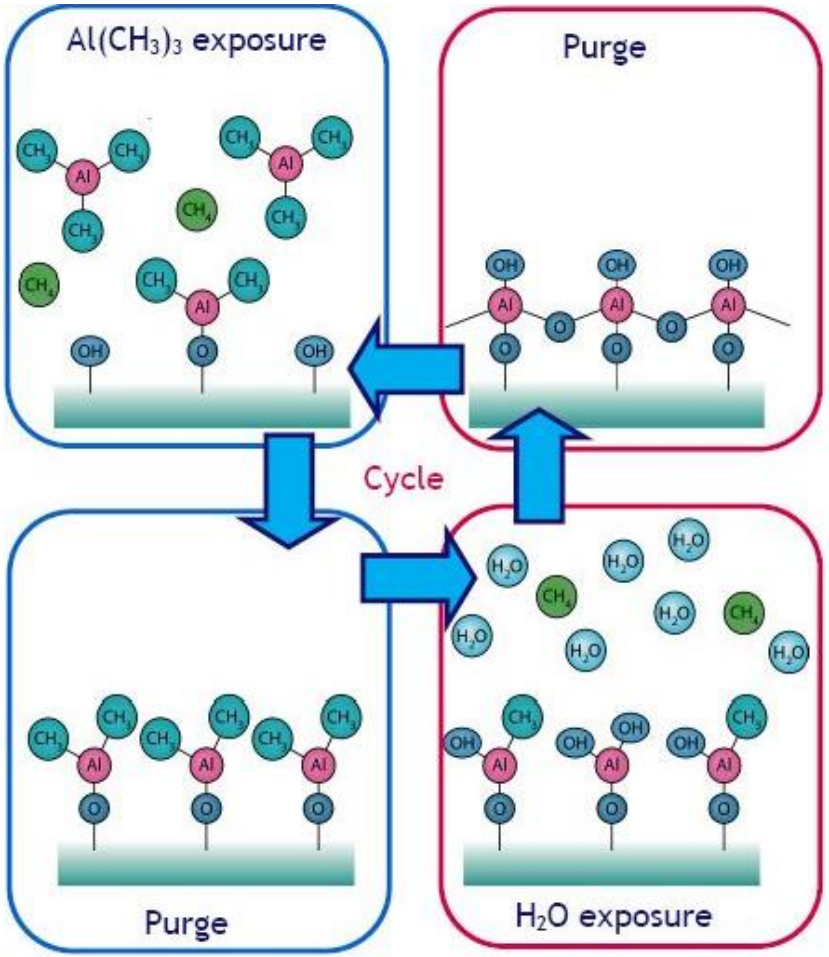
**Processing sequence for ALD Alumina deposition on p-type sensors**



# U.S. Naval Research Laboratory's FlexAL®

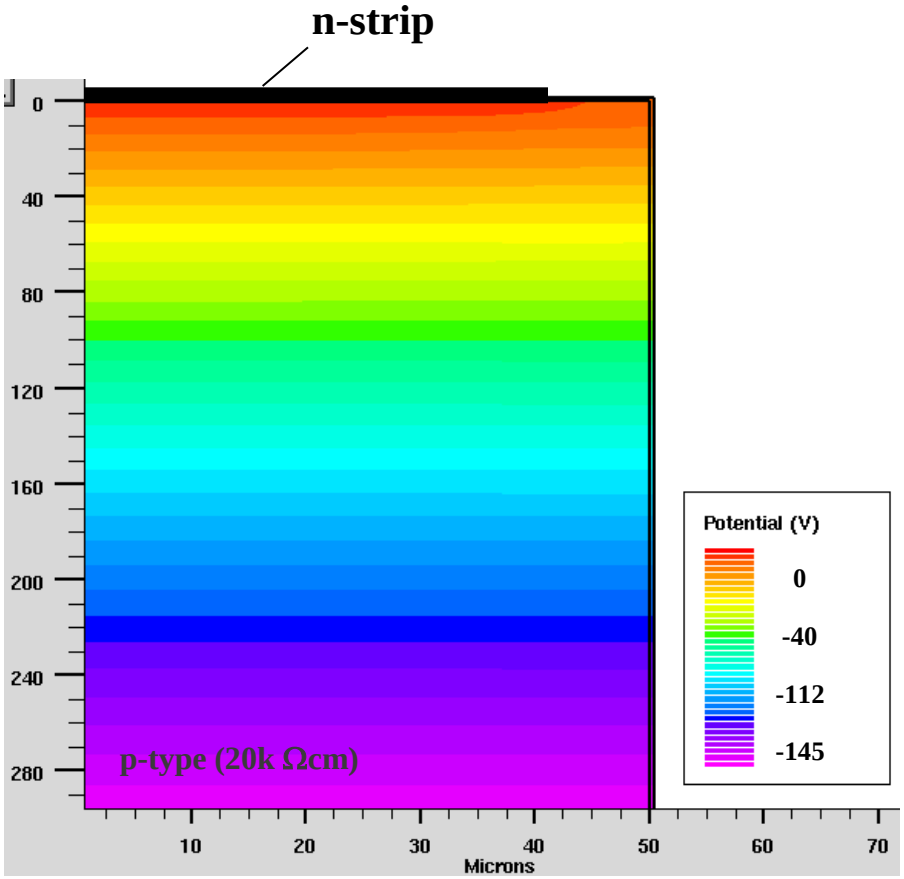

- FlexAL® from Oxford Instruments.
- plasma & thermal ALD in one flexible tool.
- stage temperature: 100 – 400 ºC.
- installed at NRL's Nanoscience Institute.

# Alumina ALD Deposition Cycle



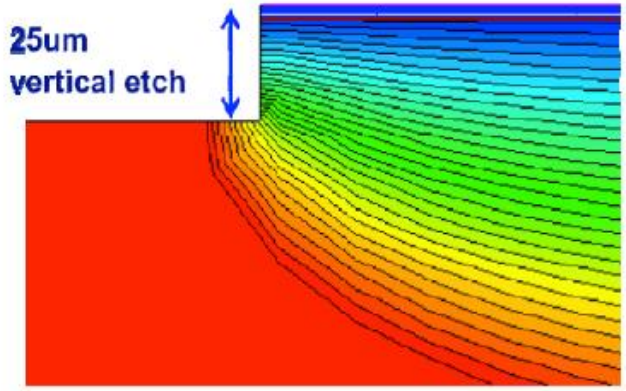

ALD Growth of $Al_2O_3$ from $Al(CH_3)_3$ and $H_2O$

# Potential Distribution Without Surface Charge

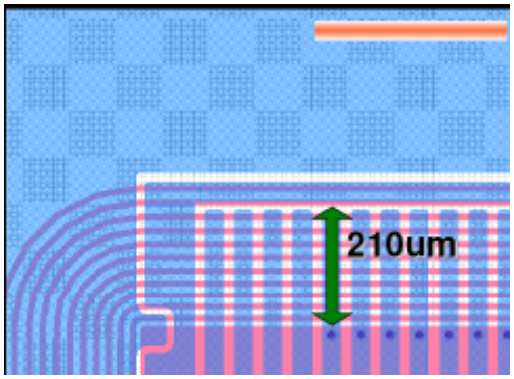



**Not considering surface charges leads to *wrong* potential distribution at sidewall.**

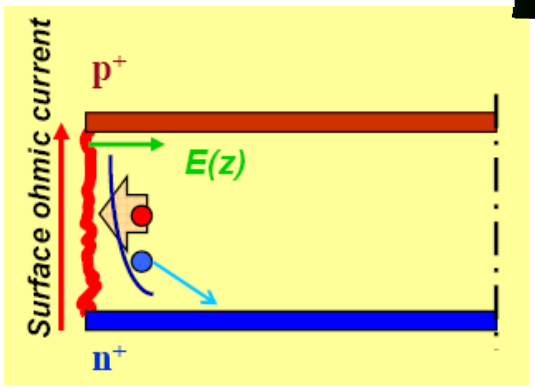
# Slim Edges - Approaches



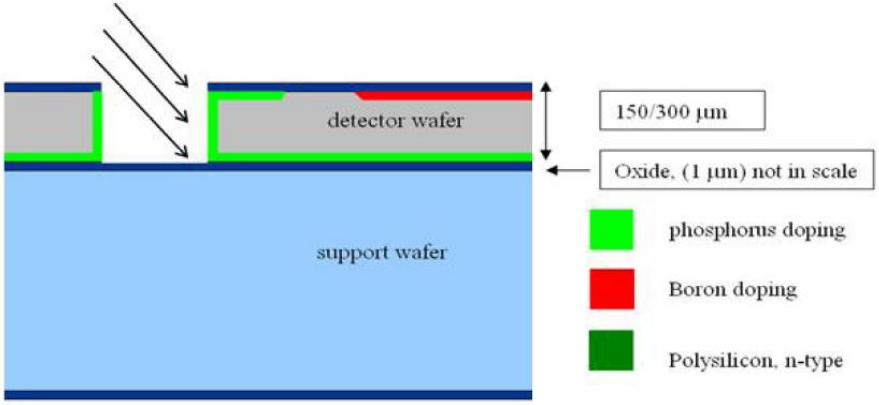

J. D. Segal, et al., NSS 2010



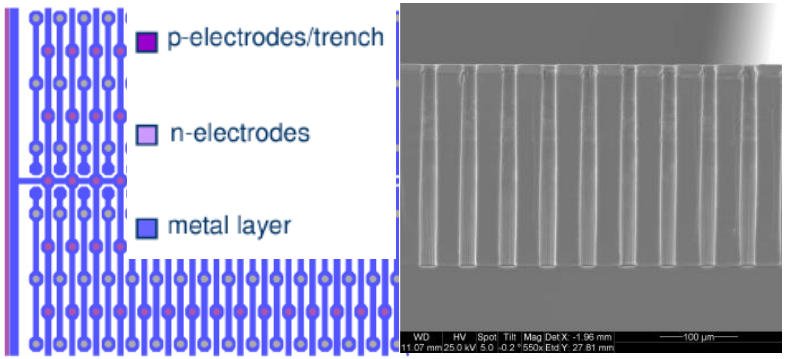

A. Rummler et al., 2010




E. Verbitskaya et al., 13 RD 50 workshop, 2008




J. Kalliopuska, NSS 2010




T.-E. Hansen et al., 2009

**Goal of our research:**
- **slim edges with finished devices on die level**
- **slim edges on p- and n-type devices**