# Interface with I2C @ SCA

- Short summary of discussion with Kostas Kloukinas (this morning)
- GBT-SCA will be the interface for FE ECS
  - GBT-SCA is in IBM 130 nm:
    - 1.2 V core and up to 2.5 V for IO (currently)
    - However IO @ 3.3 V is possible using extra masks (thicker gate oxide for IO MOS)
  - I2C slow signals are connected to fast digital electronics
    - Problems (glitches, etc) observed: pads with hysteresis are required.
- What happens if to be connected to 3.3 V chips?
  - Currently GBT-SCA CAN NOT be directly connected to 3.3 V chips
    - Even for I2C which is in open drain configuration
    - With 3.3V pull-up, logic 1 will turn on protection diodes of 2.5 V IO
  - It is possible to use commercial level shifters but they will have to be qualified to operate in radiation (TID and SEL).
  - Preferred solution would be have 3.3 V IO at SCA
    - No technical problem but some extra cost
    - Calo is interested on that ! Anybody else ???
- Same problem for any other SCA signal: what about reset ? GBT IO?

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- GBT to SCA interface (e-link)
  - 3 differential SLVDS pairs
  - Swing: +-200 mV and CM is 200 mV
    - Limited length and good ground required
- I2C slave implementation, two options
  - Synchronous
    - If a fast and stable clock (not SCL) is available: sample SCA and SCL lines
    - Synchronous state machine (x3 for TMR)
    - More robust but more noisy
  - Asynchronous
    - Asynchronous state machine
    - Trickier implementation: have to deal with delays in protocol transitions
    - But lest noisy (no transitions during data taking)
  - CERN has silicon proofed RTL code for both, could be available. Contact:
    - Asynchronous: Ken
    - Synchronous: Kostas