LHCb Upgrade Electronics

Meetings in 2012 (Thursday, 2pm):

9th August ??? Bring forward to July???
11th October
13th December

http://lhcb-elec.web.cern.ch/lhcb-elec/html/upgrade.htm

News

- **Optoelectronics workshop**

Some interesting info (eg Versatile Link components):
https://indico.cern.ch/conferenceDisplay.py?confId=185504

- **Related study:**

Long distance fibres from detector to surface (rather than D3)
Study underway coordinated by Niko/Laurent – next meeting

- **Maintenance contract in place for ISEG power supplies**

(many thanks to CERN-PH-ESE, valid up to end 2019)

Reminder of FE specifications

LHCb note
http://cdsweb.cern.ch/record/1340939/files/LHCb-PUB-2011-011.pdf
TFC note
http://cdsweb.cern.ch/record/1424363/files/LHCb-PUB-2012-001.pdf

Important points

Zero suppression/ Data compression:

Simulate with data from Monte-Carlo

Upgrade goal is $L = 2 \times 10^{33}$: simulate with this data !!!!!!

Extensive checks of algorithms (eg sensitivity to occupancy)

Can you use an FPGA? (flexibility)

Buffer sizes simulated & safety margin included

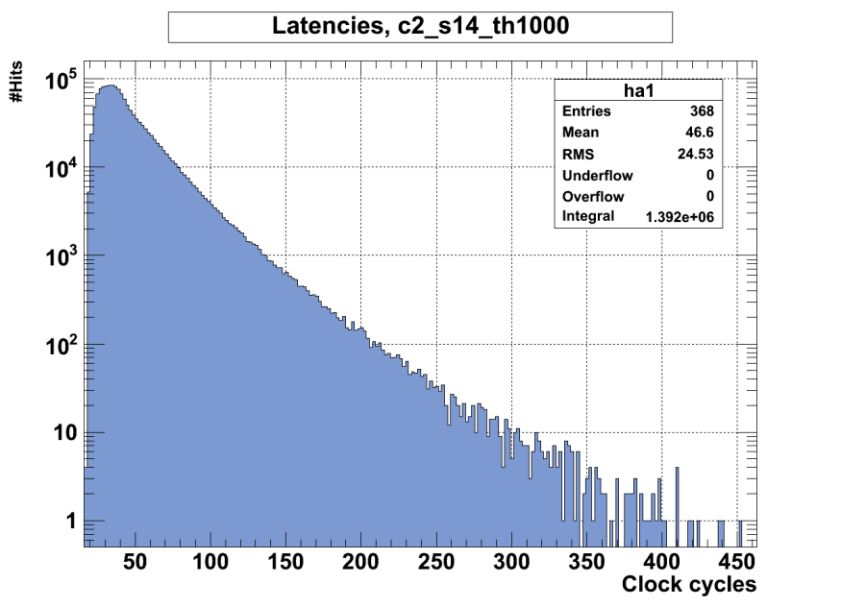
Truncation of data when overflow (still send header)

Latency of data transmission

Simulate & give worst case

Important for TELL40 buffering

Example from Velopix (not final!)



Transmission of non-compressed data

Can you do it?

Do you want to do it?

Can you easily switch between ZS & NZS?

Or will it require changing mode (via ECS)?

Local Bunch counter (12 bits):

Pre-set value to be loaded (writeable via ECS)

Very useful for time alignment

Data framing:

Header & Data

Header always sent:

Mandatory to include BCnt (max 12 bits) & flag for data truncation

Orbit reset:

BCnt and FE resets every orbit (3564 BXs)

These are different resets: make sure these are separated correctly!

Testing & Commissioning

We won't have an L0 trigger to play with!

- Test pulse injection
- Time alignment: within sub-detector (eg pulsed laser)
  between sub-detectors (cosmics, beam)
- Pattern generation: fixed digital patterns to allow (eg) clock phasing

Other diagnostics from running experience.....

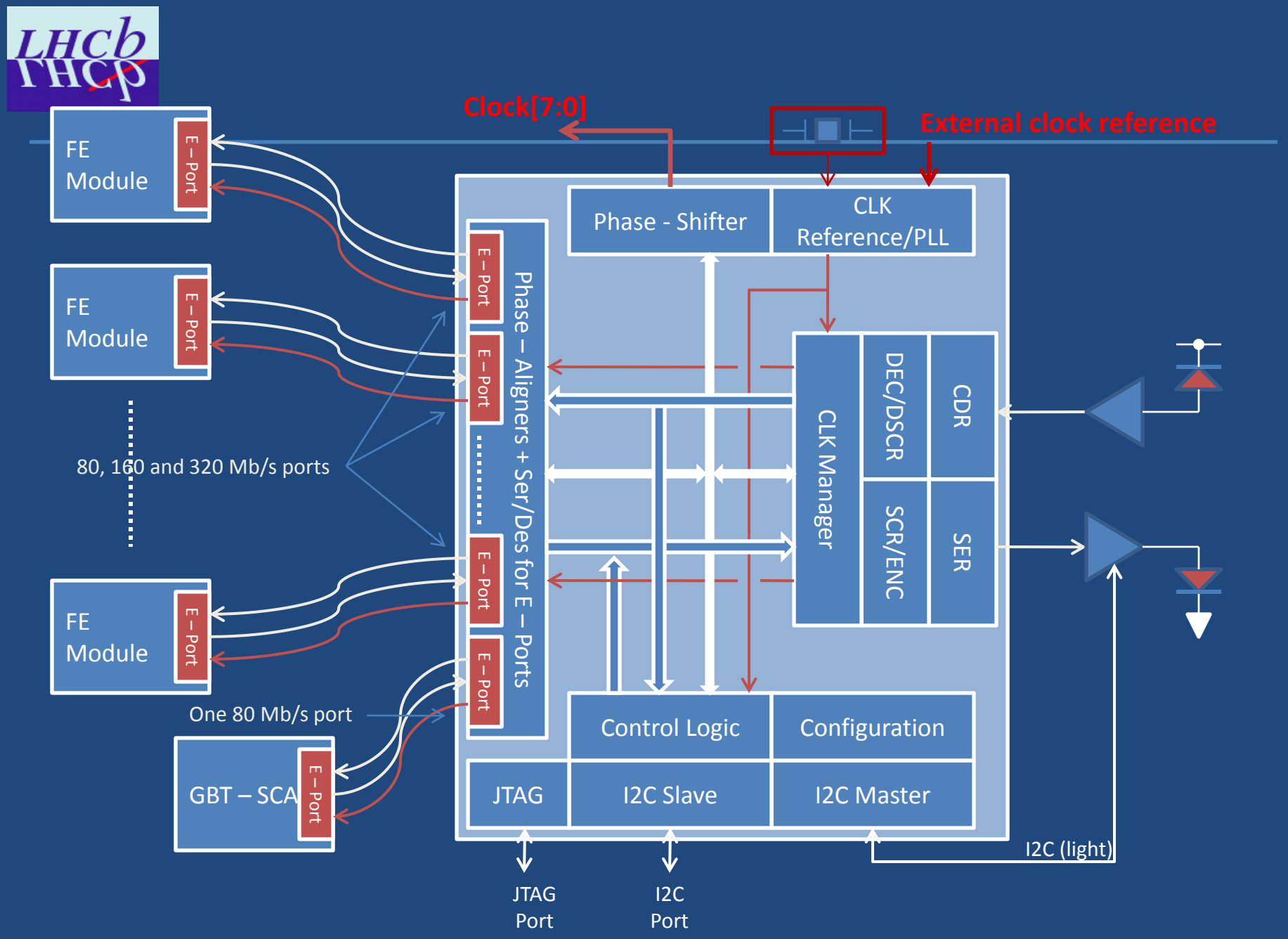
More ideas from brainstorming with Richard & Federico
Any more ideas?
For discussion at next meeting

Interfaces with common components

The GBTX is complex: please read carefully the specs!
In particular:

- Understand how to use the clocks
- Check compatibility with SLVS
- Decide Eport mode & understand implications on FE

Signal voltage swings:
GBT-SCA will be 2.5V – compatible with your FE?


Clock[7:0]
External clock reference
FE Module
E – Port
FE Module
E – Port
80, 160 and 320 Mb/s ports
FE Module
E – Port
One 80 Mb/s port
GBT – SCA
E – Port
Phase - Shifter
CLK Reference/PLL
Phase – Aligners + Ser/Des for E – Ports
E – Port
E – Port
E – Port
E – Port
CLK Manager
DEC/DSCR
CDR
SCR/ENC
SER
Control Logic
Configuration
JTAG
I2C Slave
I2C Master
I2C (light)
JTAG Port
I2C Port