Electronics for SciFi tracker for LHCb upgrade

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LHCb central tracker

The central tracker option

- Upgrade of the T station;
- Central tracker: scintillating fibres;
- Outer tracker: drift tube;
- 3×4 detector frame;
- Installation in 2018.

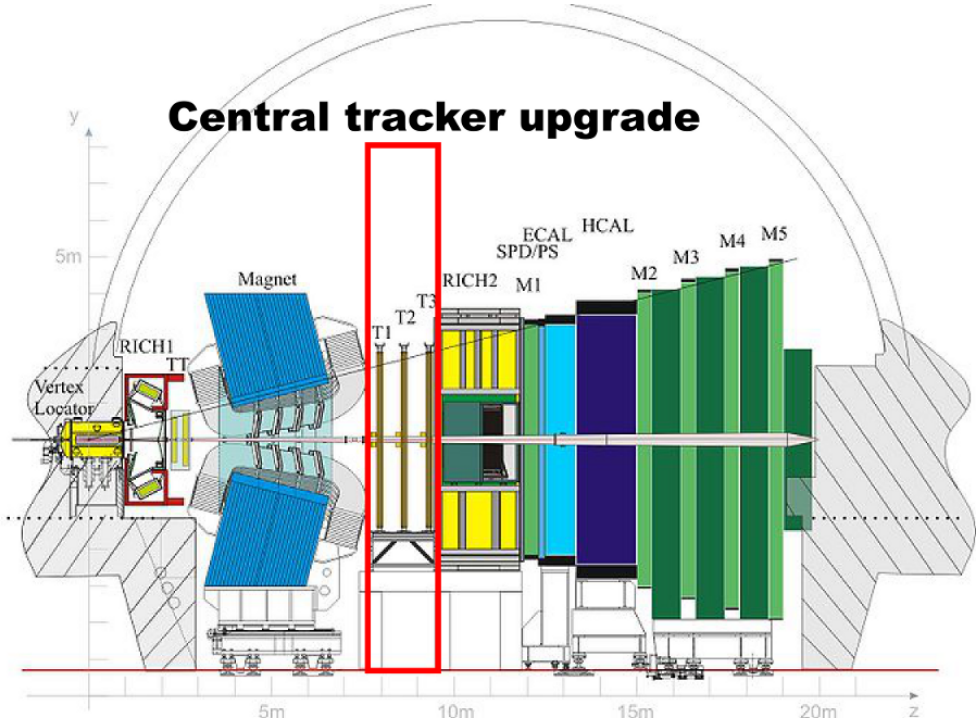


Figure: LHCb upgrade: the T stations

Foreseen electronic from the detector to the PC farm

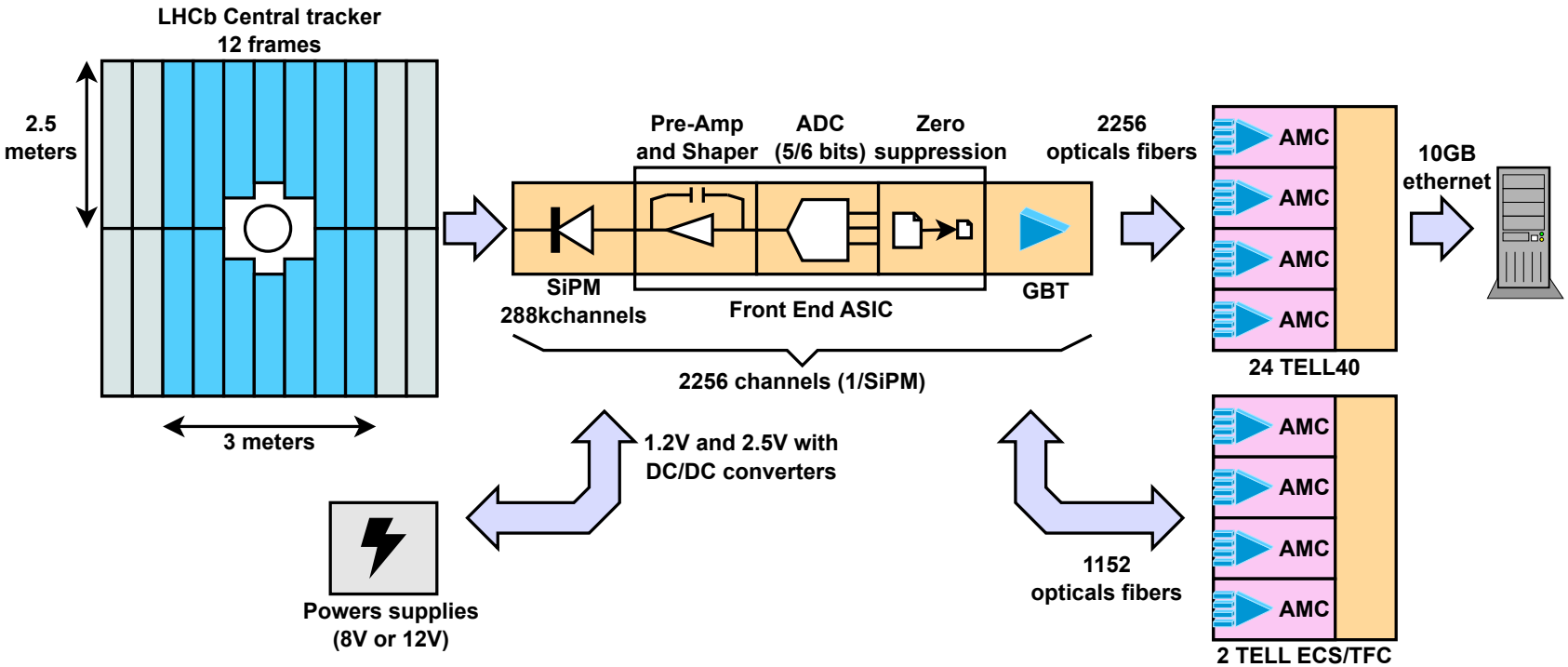
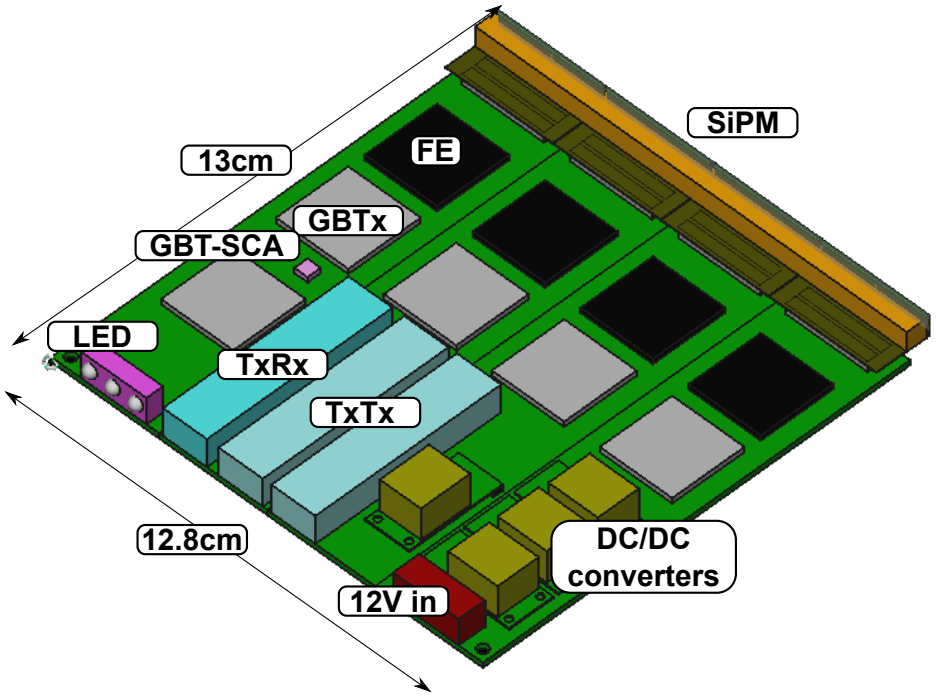


Figure: Foreseen readout scheme with 1 GBT/SiPM and 1 GBT ECS / 4 SiPM

The central tracker option

- 2.5 meters scintillating fibres;
- 250μm fibres;
- 4×3 layers.

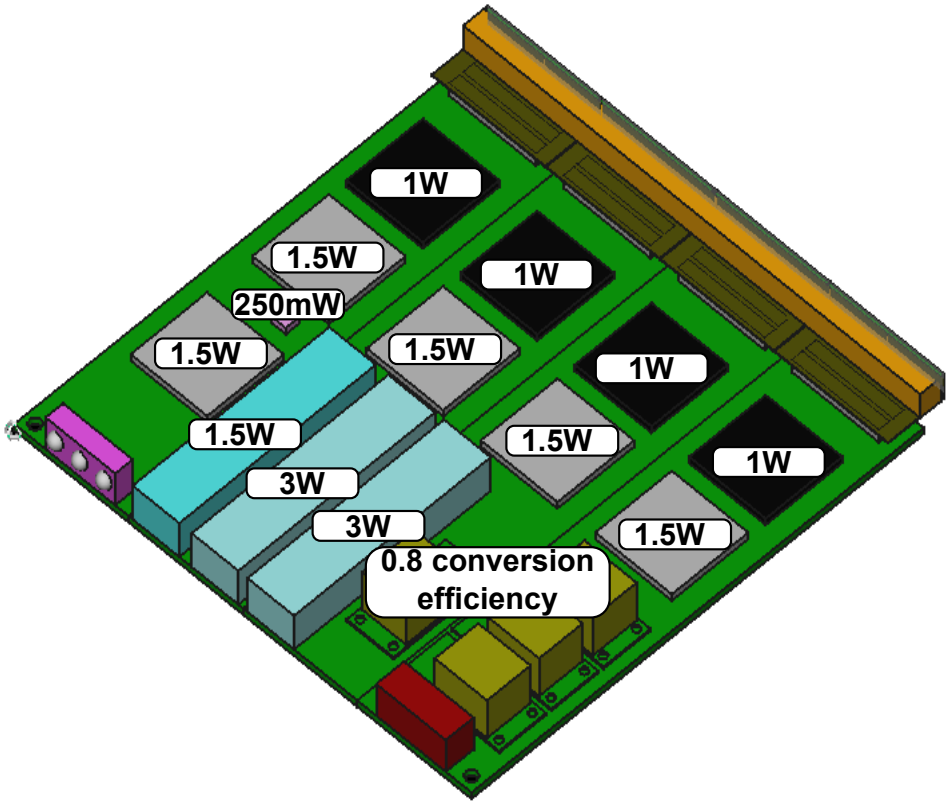
Electronic board



The FE electronic board

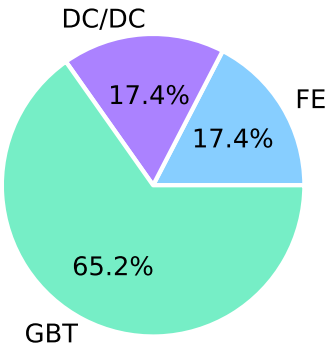
- Use 8V or 12V from remote power supplies converted to 2.5V and 1.2V using DC/DC converters (reuse marathon power supplies);
- Handle at least 4 SiPM;
- FE ASIC: BGA package (flip chip);
- 1 GBT ECS/4 SiPM ?
- Standalone module (easier to test).

Electronic board: Power consumption



For a board:

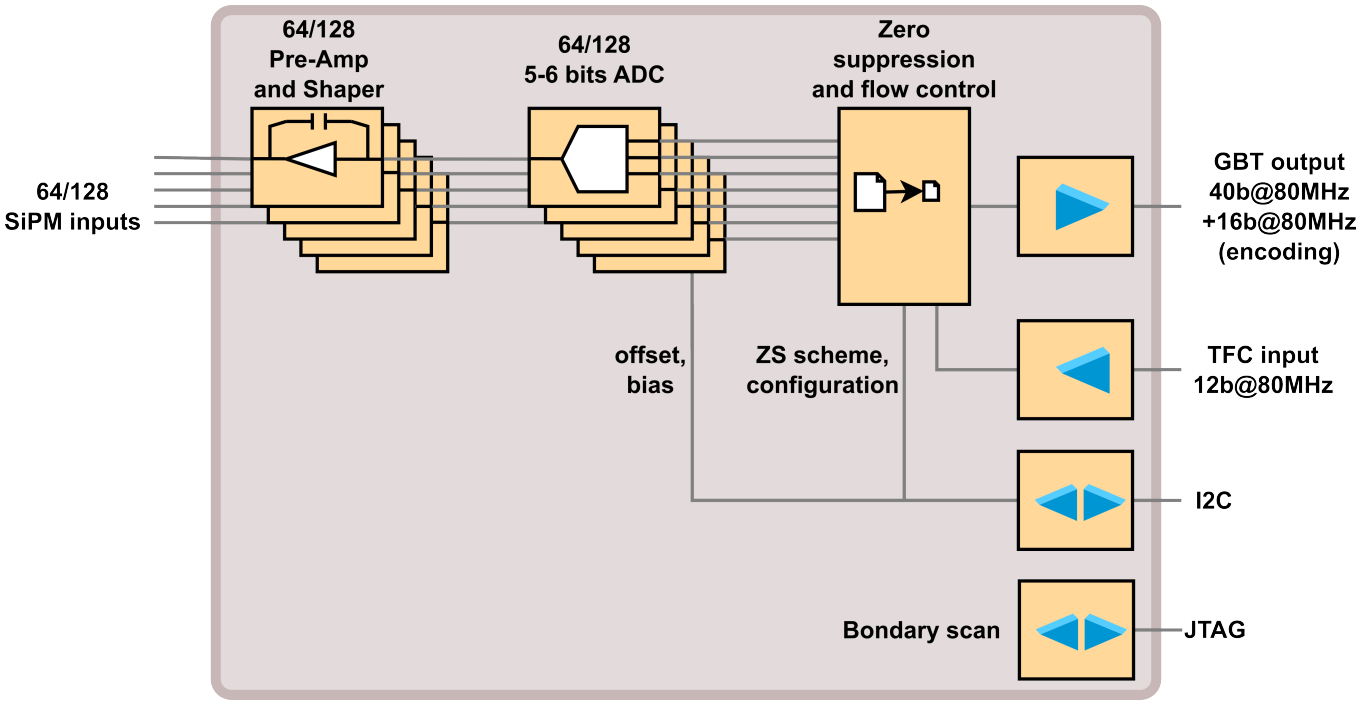
- 4W for the FE chips;
- 15W for the GBT;
- 4W for the DC/DC converters.



Detector power consumption

- Needed boards: $24 \times 2(up/down) \times 12(planes) = 576$;
- For the detector: 14kW.

Chip block diagram



The low-Power ASIC for the sCIntillating FIbres traCker (PACIFIC) is a collaboration between the Universitat de Barcelona and the Laboratoire de Physique Corpusculaire de Clermont-Ferrand. Synergies with the ASIC for the TT and VELO strip option are investigated.

- Low power (8mW/channel);
- With built-in test features.

Silicon Photo-Multipliers readout needs

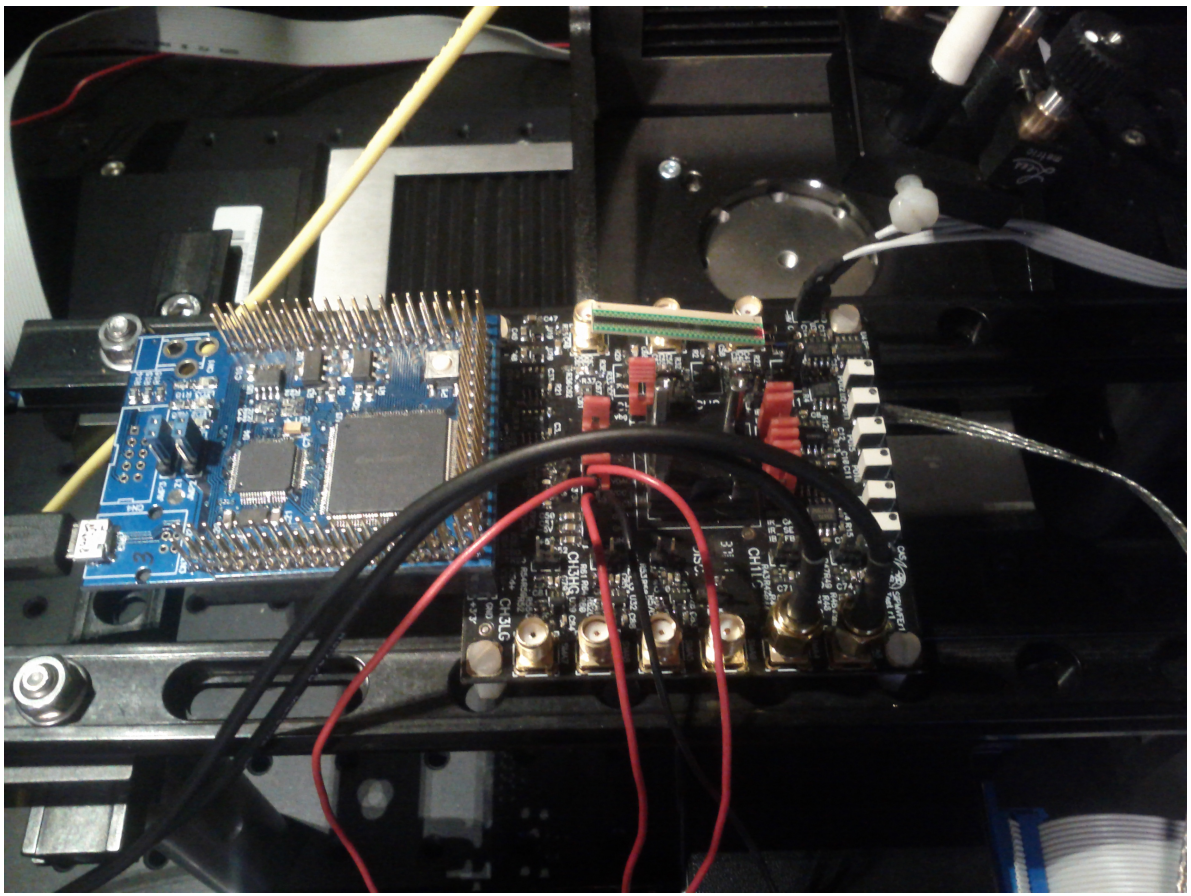
Some simulations and tests with commercial devices suggest an optimal ASIC design with the following characteristics:

- Input stage:
  - Common-Catode arrays, current must "enter" into the preamplifier;
  - Sensor capacitance may vary, now around 35 pF;
  - Low input impedance (around 20Ω);
  - Dynamic range should be around 88cells ($5\mu A$ - 1.3 mA);
  - V_{ANODE} must be configurable by channel in a range of ≈1V;
  - High speed (around 250MHz) preamplifier.
- Signal processing:
  - Shaping time should be around 25ns, double pulse resolution of 25ns.
- TDC or ADC:
  - 40MSps, 4,5 or 6 bits, low power. One per channel? Multiplexed?
- Digital processing:
  - Zero supression;
  - Clusterization;
  - Compression;
  - GBT interface.

Analog front-End: Test

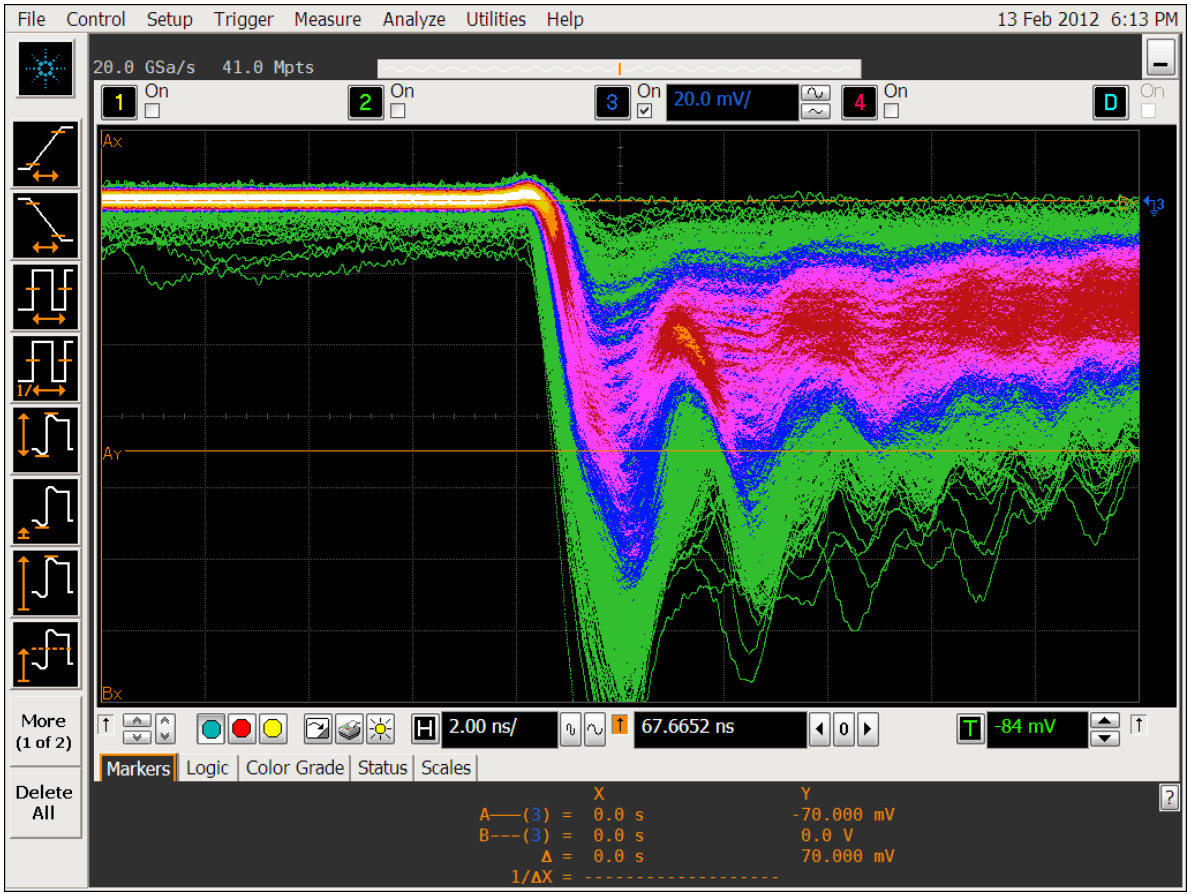
A first analog front end has been developed in 0.35μm with BiCMOS:

- the 0.13μm version design is ongoing;
- allows to test SiPM Array: red laser pointing on first channels of device connected to ASIC test board.



Analog front-End: Result

As an example: Output with 10 SiPM cells fired using the low gain



Clusterization

Needs

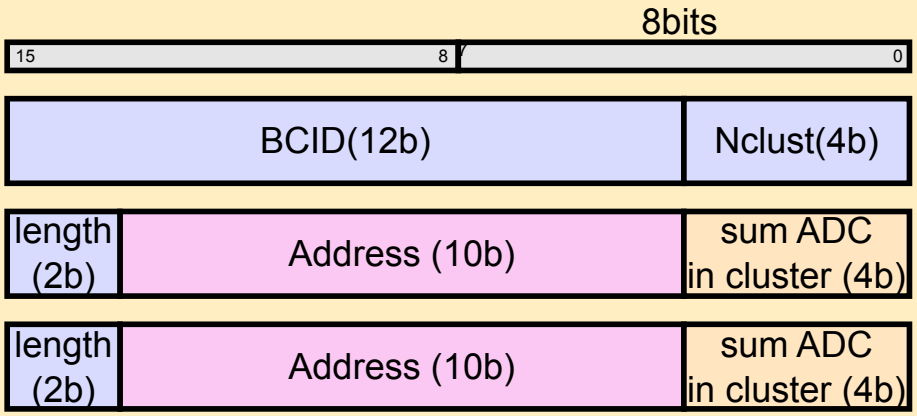
A GBT can not send all the data processed from a SiPM (31Gb/s)

Solution

The cluster barycentre is computed in the chip.
Principle:

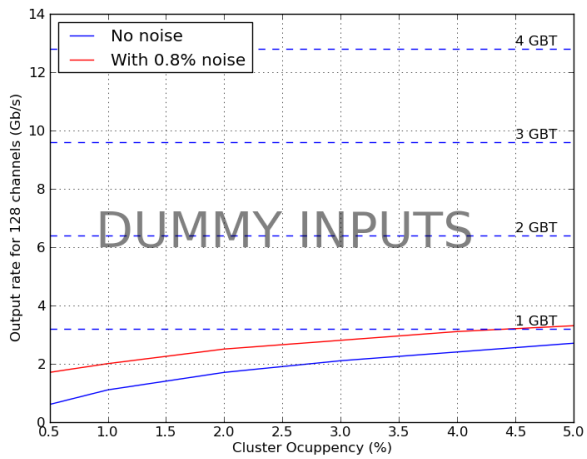
- The ADC values are not sent;
- An extended address (7b+3b) with an 1/8 fibre resolution is sent;
- the ADC sum/cluster size is sent for sanity checks;
- 16 bits/cluster.

Frame:



Results

A systemC model has been developed to check this processing.



- The feasibility has to be tested using full physics simulations.

Frame

Solution

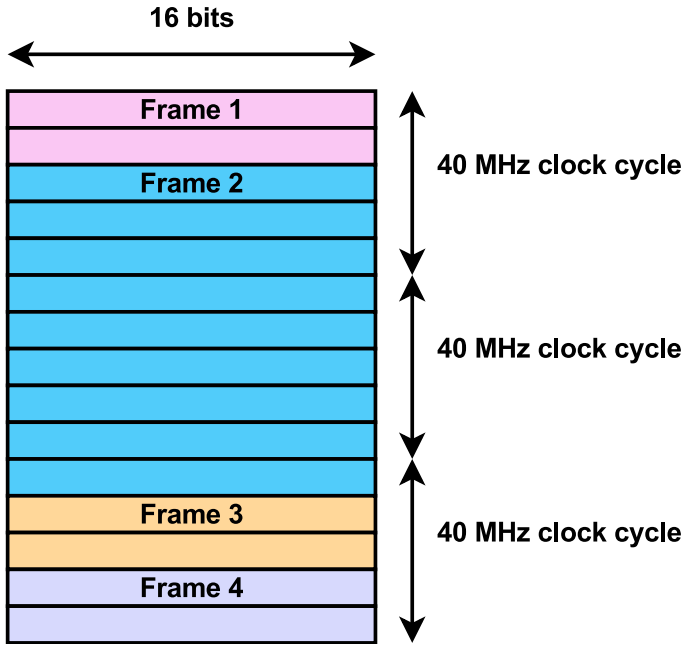
- The GBT is able to send 80 bits/40MHz clock cycle;
- The frame is composed of 16 bits words;
- Several types of frame are foreseen: zero suppressed, non zero suppressed, error;
- The frame size can be larger than 80 bits;
- The frame size is not know and must be encoded in the header;
- The GBT handle bits, not frames.

$\Longrightarrow$ How to recover from a de-synchronisation coming from a wrong frame length in the header (SEU...):

- Redundancy or special encoding:
  - Loss of bandwidth;
  - We need to be 100% safe...
- Handle the frame at the GBT level:
  - Modify the GBT protocol;
  - 24 bits can be used in the transmission only mode;
  - Would be nice if it's a common development.

Foreseen GBT/FE link:

- 16 bits words;
- Variable length frame.



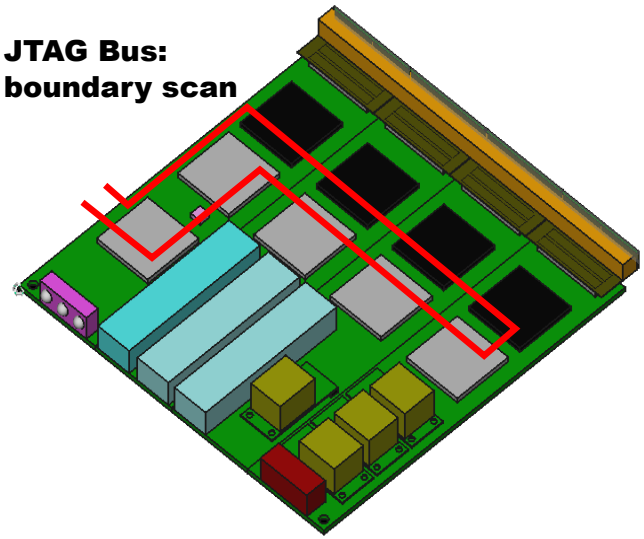
Test features

General test features

- JTAG interface for boundary scan;
- Board identification;
- Some LED.

Behavioural tests

- Analog injector;
- A RAM with a few events in the FE chip;
- Monitoring counters (SEU, processing...);
- Non Zero Suppress stream;
- Error frame ?



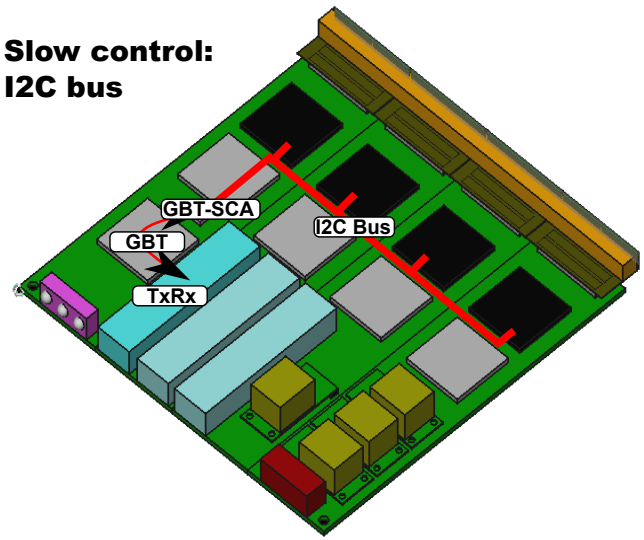
Configuration

Registers

The registers will be loaded by the I^2C interface.
For a 128 channel chip:

- Gain and offset: 1536b;
- Thresholds (by channel?): 1536b;
- Configuration: 512b.

Configuration for a PACIFIC chip: 3.6kb
Configuration for a board: 14.4kb
Configuration for a detector: 8.2Mb



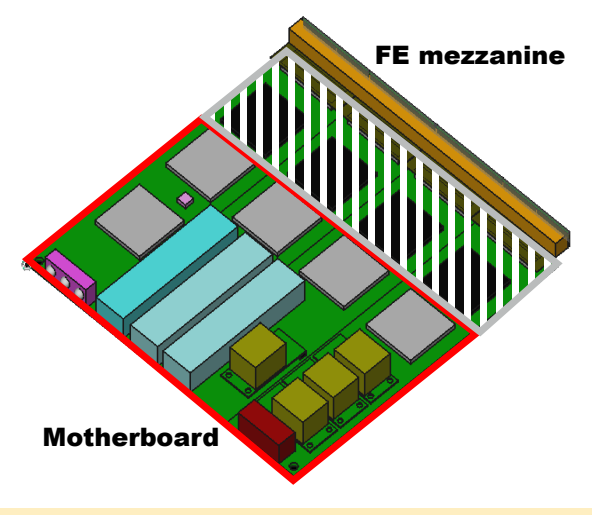
Foreseen development: Q4 2012/2013

Chip

- Develop, submit and test the basics blocks;
- Develop a one channel prototype.

Electronic

- Develop and test a GBT motherboard;



- Develop an acquisition system for the test of the mezzanine (using GLIB?).

Question to address

- Number of GBT/SiPM;
- Chip final specification;
- Number of channel/chip;
- ZS scheme;
- GBT protocol;
- GBT-ECS needs (1/board ?);
- Board size;
- SiPM noise level;
- Synergies on the test bench and software libraries ?
- Accurate power consumption.

Foreseen development: 2014

Chip

- Test the one/a few channel prototype;
- Develop the 64/128 channel chip.

Electronic

- Develop and characterize a detector prototype with the one channel chip;
- Develop the TELL40 firmware.

Question to address

- How to use a flip-chip BGA package;
- How to test 3000 chips off and on detector;
- How to test the boards off and on detector;
- How to change a board during the detector opration/shut-down;
- How to be able to follow a particular chip or board during its lifetime (database, fuse in the chip...).

Foreseen development: 2015

Chip

- Qualify the 64/128 channel chip performance before the production.
- Minimize the changes;
- Start the production.

Electronic

- Develop a detector prototype with the 64/128 channel chip;
- Develop the final boards;
- Develop the test-bench;
- Test the TELL40 firmware.

Question to address

- Maintenance guide.

Conclusion

The electronic for the central tracker is challenging:

- New type of tracker;
- Tight schedule;
- Limited manpower;
- Bandwidth needs, number of channels...
- Power consumption.

The bottlenecks have been identified and a lot of activities have started to address them:

- The shaper and pre-amp design;
- Physics simulations;
- SiPM characterization;
- Fibre characterization and module construction;
- Electronics collaborations.