# Tell40 development status


J.P. Cachemiche, PY.Duval,
F.Hachon, R. Le Gac, F.Rethoré

## Outline

- Overall boards development status
- AMC40 & AMC_TP status
- Current issues and solutions
- Next steps

# Hardware development status

## AMC40

- Delay during PCB manufacturing :
  - False contacts during electrical tests
  - Was due to misalignment of vias
  - New PCB had to be relaunched : now OK
- Board finally received from assembly manufacturer on **June 8th**
- Waiting for front plate

## AMC_TP

- Board received **end of May**

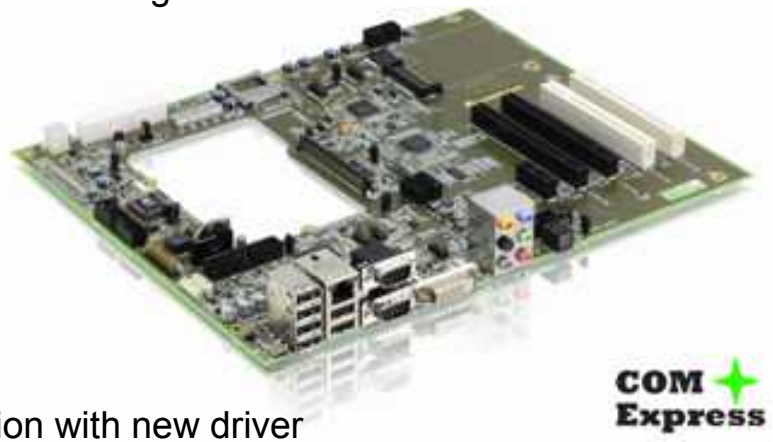
## ATCA40

- Design finished : **routing starts now**

# Software development status

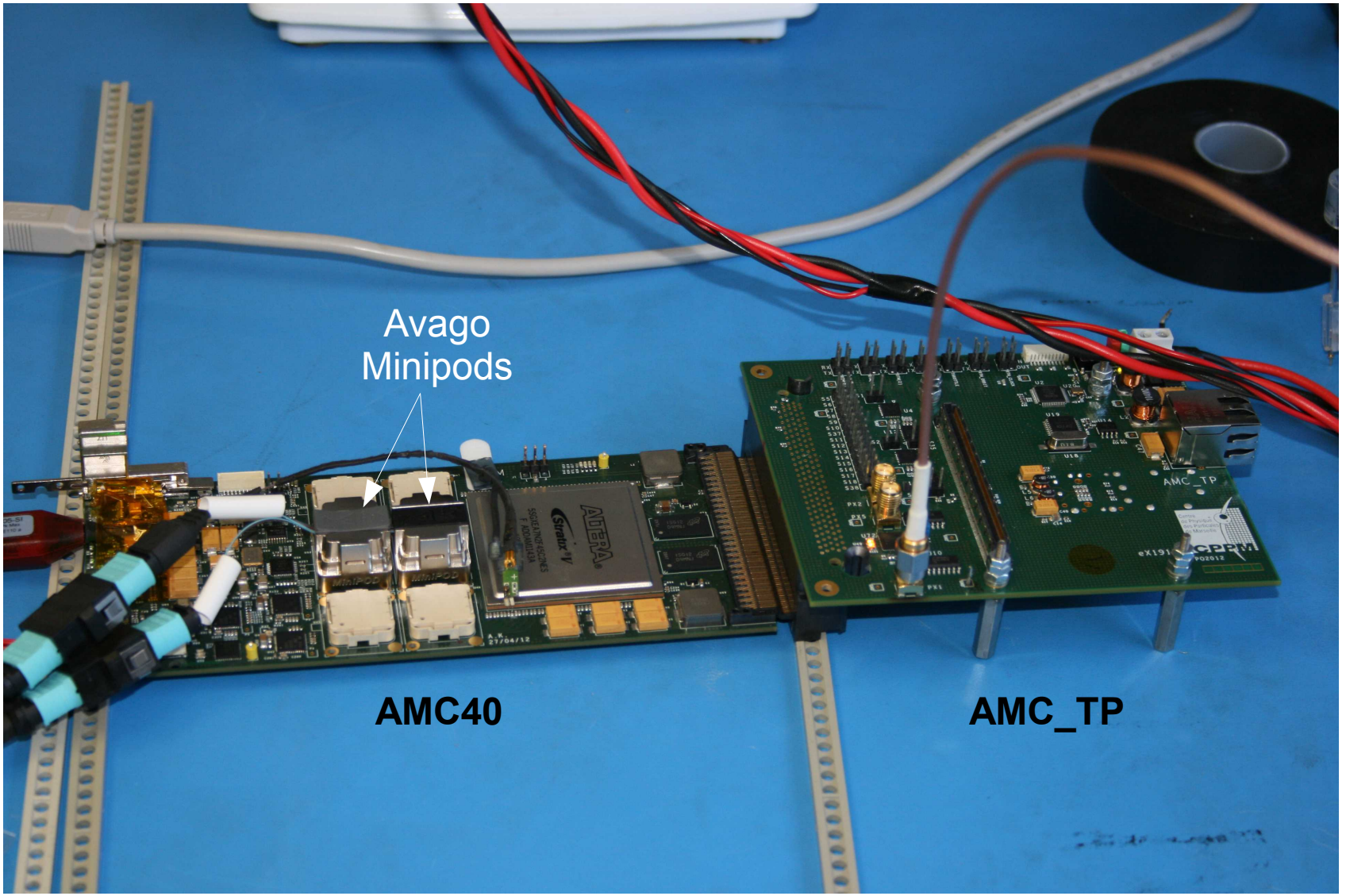
## Linux boot

- Use of a Kontron design kit for early implementation :
  - Allows having a display, keyboard, disk interface, etc …
  - AMC_TP as well as ATCA40 will only have an GbE interface
    - Network bootstrap must be parameterized on the design kit




- SL62 boot OK from an attached hard disk
- Network boot does not work with SL62
  - Whereas it works with Fedora ...
  - Should be a problem with a driver too old
    - Niko contacted for recompiling an SL62 version with new driver

# AMC40 & AMC40 debug status



# What works (or doesn't) after 3 days

## AMC40

- Power supplies all OK except 3.0V on GBT optical transceiver:
  - Not investigated yet
- Power sequencing (to cope with engineering sample bug): OK
- MAX V programmation: OK
- Stratix V GX programmation: OK
- NIOS core running with basic QSYS environment
- PLL access through SPI bus: OK
- PLL does not lock:
  - Under investigation

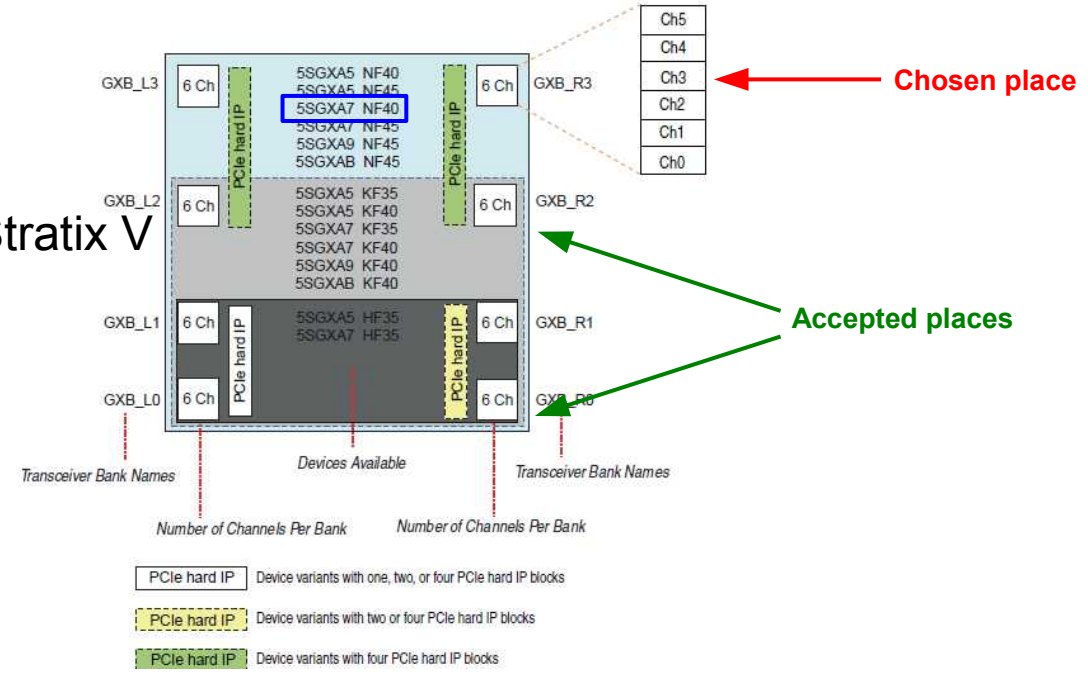
## AMC_TP

- Harware all OK
- Linux boot does not work

# Current issues and solutions (1/2)

## PCIe problem detected

- Compilation errors when routing the PCIe hardware IP on bloc R3
- Detected too late : manufacturing of PCB already done
- Causes :
  - Confusing Altera documentation
  - PCIe MAC Harware IP only compilable since few weeks: we tested placement with PCIe PHY only, and it worked !!!
- No more VHDL IP from Altera for Stratix V
- Former Stratix IV version of VHDL IP not usable
  - Reason unclear
  - Ongoing discussion with Altera



# Current issues and solutions (1/2)

## PCIe issue : possible solutions

- Short term :
  - Allowed serial input for PCIe is currently a 10GbE I/O or a GBT I/O
    - We have an optical driver on the AMC_TP board, not currently connected to PCIe link, but can be connected with a minimum hardware modification
- Medium term :
  - Minimum rerouting of the AMC board by sacificing one 10 GbE link:
    - cost ~ 3.5 k€
    - Can be used for card dupplication
  - Use a COTS PCIe MAC IP :
    - Several companies contacted
    - Some very expensive ~ 15 k€
  - Write a minimum PCIe MAC layer
    - Under evaluation: should not be so difficult
    - Manpower ?
- Long term:
  - Reroute the board and flip the FPGA by 180 ° 

# Conclusion

## Next steps

- Find the best Cost/Manpower/Efficiency solution for PCIe issue so that early users had their boards on time
- Continue debug with :
  - Test and BER measurements of 10Gbits/s optical links
  - Test and BER measurements of GBT links
  - Test and integration of a 10 GbE IP from Altera
  - Fixed phase clock extraction
- Encapsulate design in easy to use QSYS modules :
  - GBT interfaces
  - 10 GbE
- Integrate TFC emulation in collaboration with Richard and Federico
- Provide a minimum test setup environment with documentation