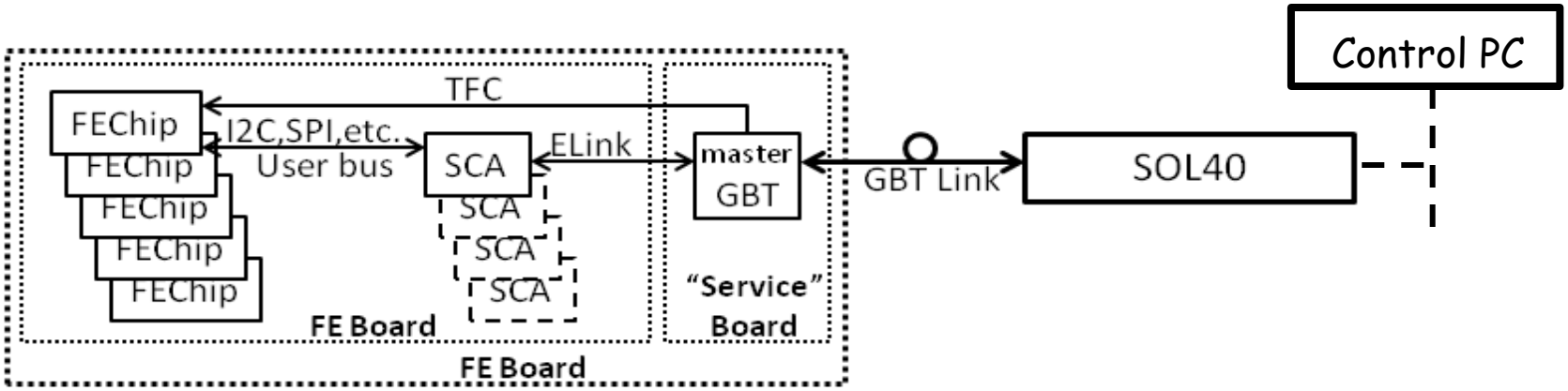
ECS - FE Interface

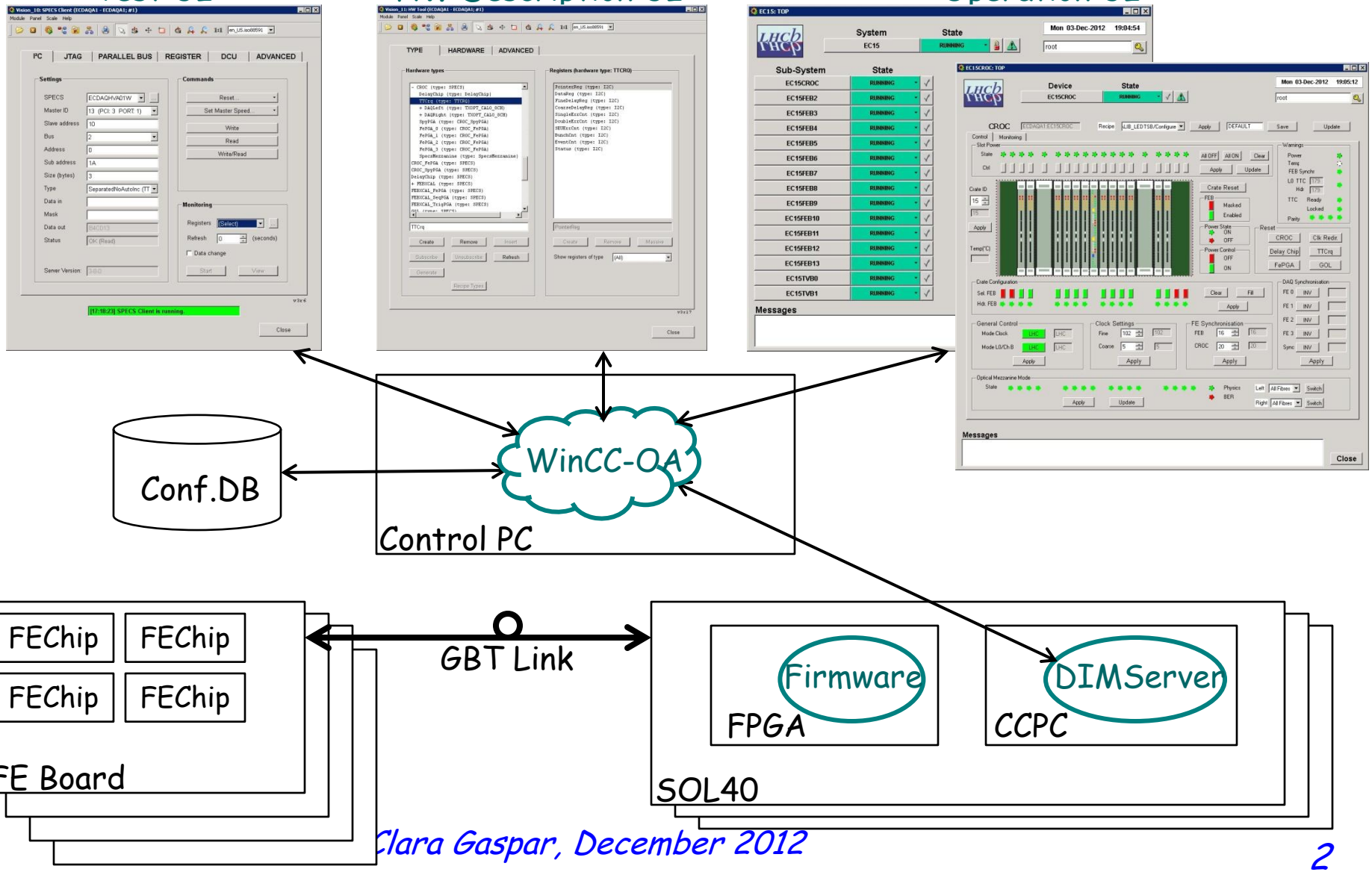


- **Available Board protocols (GBT-SCA):**
  - 16 x I2C master controllers
  - 1 x JTAG master controller
  - 32 x ADC channels (multiplexed)
  - 1 x Memory bus (32 bits) controller
  - 4 x PIA (Parallel Interface Adapter) controllers
  - 1 x SPI (Serial Peripheral Interface) bus ➡ SPI using independent chip selects (daisy chained SPI not allowed)
  - 4 x DAC channels
- **FE Chip Register Address:**

<SOL-ip><GBT-i><SCA-j><ProtoCode><I2C-k><I2C-add>[<I2C-s.add>]

fixed **variable**

ECS FE Dataflow



Scalability & Efficiency

- **Configuration and Monitoring speed**
  - Is not just data size / bandwidth
  - To be taken into account:
    - How the data is distributed, for ex.:
      - A few large registers or many small ones
    - Are blocking operations needed, for ex.:
      - A register needs to be set and read-back before configuring the next one
      - or read-modify-write operations that need to be done by the back-end
    - Which user protocol is used and how it is used, for ex.:
      - Some I2C devices needed an extra I2C operation to write a sub-address before the block of data could be written
      - Some did not implement auto-increment so block transfer could not be used