AMC40 Firmware Coordination

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Stéphane T'Jampens

13 december 2012
LHCb upgrade Electronics meeting

Outline

1. Kick off meeting
2. Coordination
3. Methodology
4. Workshop

1. Kick off meeting

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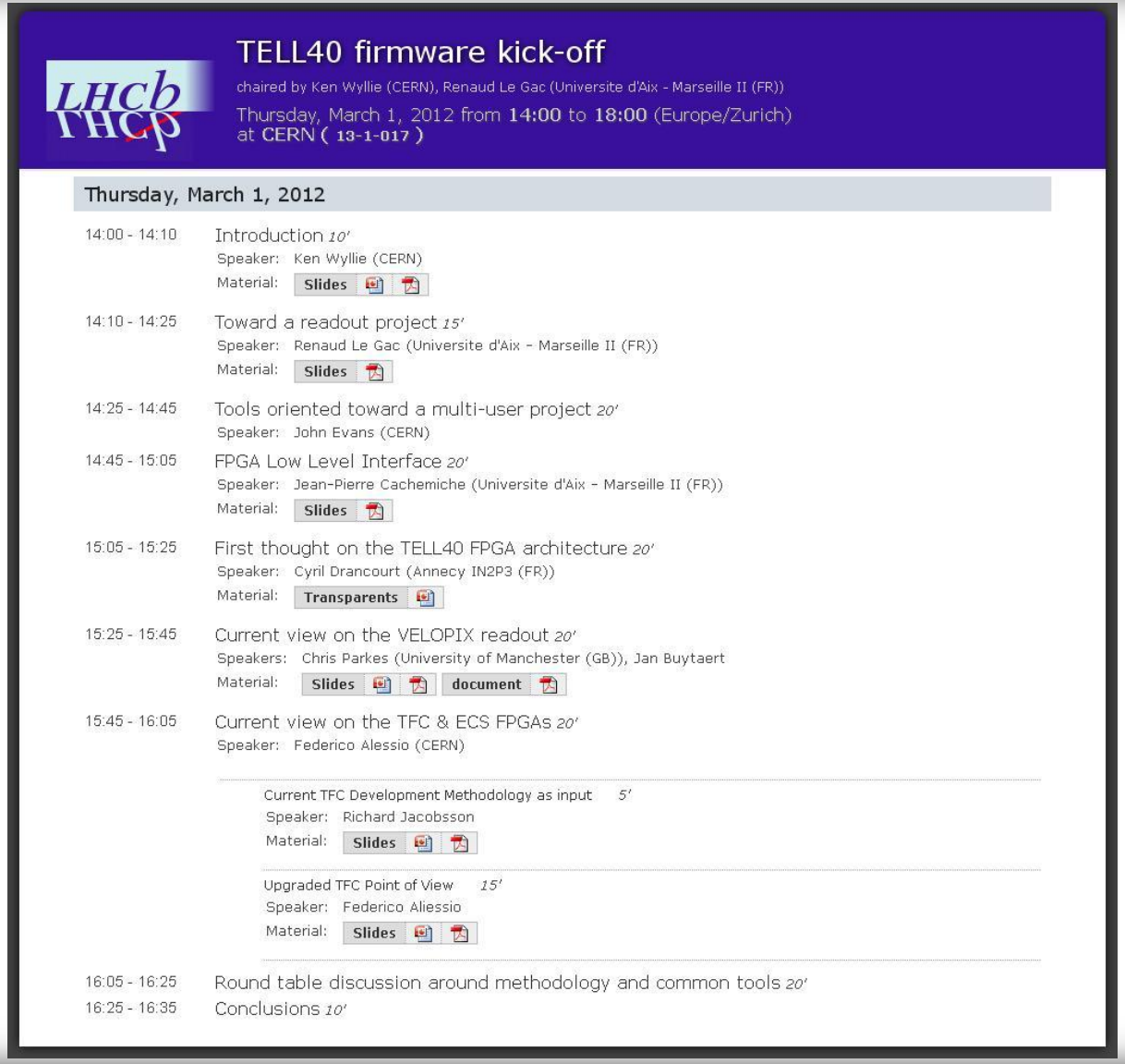

TELL40 firmware kick-off

chaired by Ken Wyllie (CERN), Renaud Le Gac (Universite d'Aix - Marseille II (FR))

Thursday, March 1, 2012 from 14:00 to 18:00 (Europe/Zurich)
at CERN (13-1-017)

Thursday, March 1, 2012

14:00 - 14:10 Introduction *10'*
Speaker: Ken Wyllie (CERN)
Material: Slides

14:10 - 14:25 Toward a readout project *15'*
Speaker: Renaud Le Gac (Universite d'Aix - Marseille II (FR))
Material: Slides

14:25 - 14:45 Tools oriented toward a multi-user project *20'*
Speaker: John Evans (CERN)

14:45 - 15:05 FPGA Low Level Interface *20'*
Speaker: Jean-Pierre Cachemiche (Universite d'Aix - Marseille II (FR))
Material: Slides

15:05 - 15:25 First thought on the TELL40 FPGA architecture *20'*
Speaker: Cyril Drancourt (Annecy IN2P3 (FR))
Material: Transparents

15:25 - 15:45 Current view on the VELOPIX readout *20'*
Speakers: Chris Parkes (University of Manchester (GB)), Jan Buytaert
Material: Slides document

15:45 - 16:05 Current view on the TFC & ECS FPGAs *20'*
Speaker: Federico Alessio (CERN)

- Current TFC Development Methodology as input *5'*
  Speaker: Richard Jacobsson
  Material: Slides
- Upgraded TFC Point of View *15'*
  Speaker: Federico Aliessio
  Material: Slides

16:05 - 16:25 Round table discussion around methodology and common tools *20'*
16:25 - 16:35 Conclusions *10'*

Team

We are going to use a new generation of fpga.

Such a big FPGA requires to have multi developers for one firmware. The way to work on a FPGA is changing, we can't do it alone.

We need to work together.

From that comes the idea of a common firmware as much as possible, since we electronics engineers are lacking.

We need people to organize how and how much we can do a common firmware.

But we need to work as a Team

Firmwares development coordinators

LAPP accepted to play the role of coordinators

Laboratoire d'Annecy le Vieux de Physique des Particules

Coordinator of the firmwares development team :

- Guillaume Vouters (Electronic Coord.)
- Cyril Drancourt (Electronic Coord.)
- Stephane T'Jampens (Scientific Coord.)

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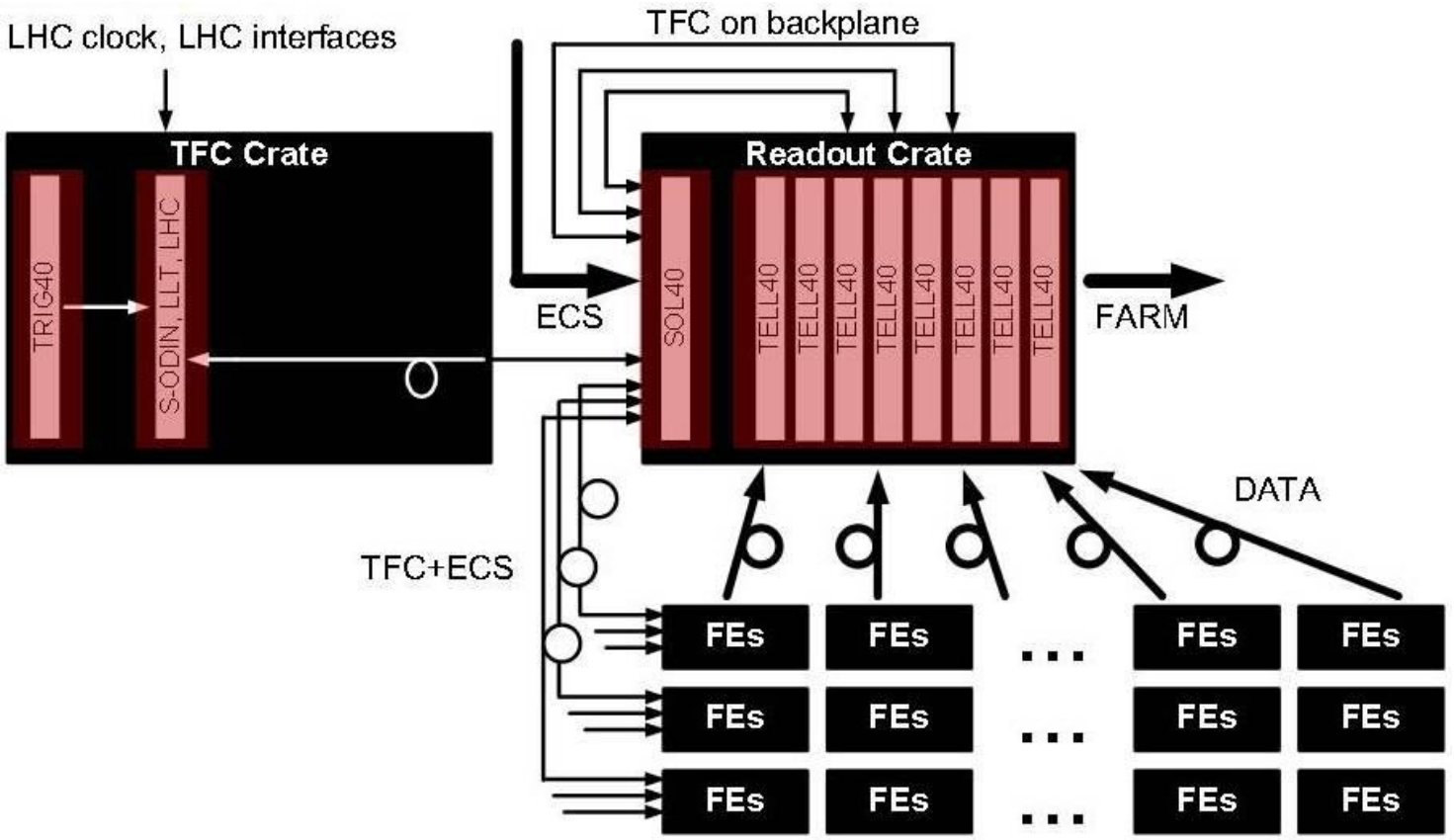
Upgrade Electronic Setup



The current organization

WP 1.2.2	Firmware development	Participant(s)	∅(FTE)	Cost	Developpers
0	Coordination	Annecy		–	Stéphane T'Jampens + Cyril Drancourt
1	Specifications, documentation and reviews	Annecy		–	Stéphane T'Jampens + Cyril Drancourt
2	Low Level Interface	Marseille	6	–	Jean-Pierre Cachemiche et al.
3	Data Centre Bridging	CERN		–	Rainer Schwemmen
4	TELL40 MEPs building	Annecy (tbc)	4	–	Cyril Drancourt et al.
5	TELL40 generic user	Annecy (tbc)	2	–	Cyril Drancourt et al.
6	ODIN40, TFC&ECS	CERN		–	Federico Alessio + Richard Jacobsson
7	VELO pixel	Manchester, AGH-Krakow		–	Chris Park et al. + Tomasz Szumlak et al.
8	VELO strip	Manchester, AGH-Krakow		–	Chris Park et al. + Tomasz Szumlak et al.
9	Central Fiber Tracker			–	
10	Scilicon Strip Tracker			–	
11	OT	Dormunt		–	Stefan Swientek et al.
12	RICH	Cambridge		–	Stephen Wotton
13	TORCH			–	
14	CALO			–	
15	MUON	Cagliari, Frascati		–	Adriano Lai + Paolo Ciambrone et al
16	LLT CALO	Annecy	2.5	–	Cyril Drancourt et al.
17	LLT MUON	Marseille	2	–	Jean-Pierre Cachemiche et al.
18	LLT L0DU	Clermont		–	Régis Lefèvre et al.
19	CCPC and test bench	Rio (CBPF)			André Massaferri

To be updated !!

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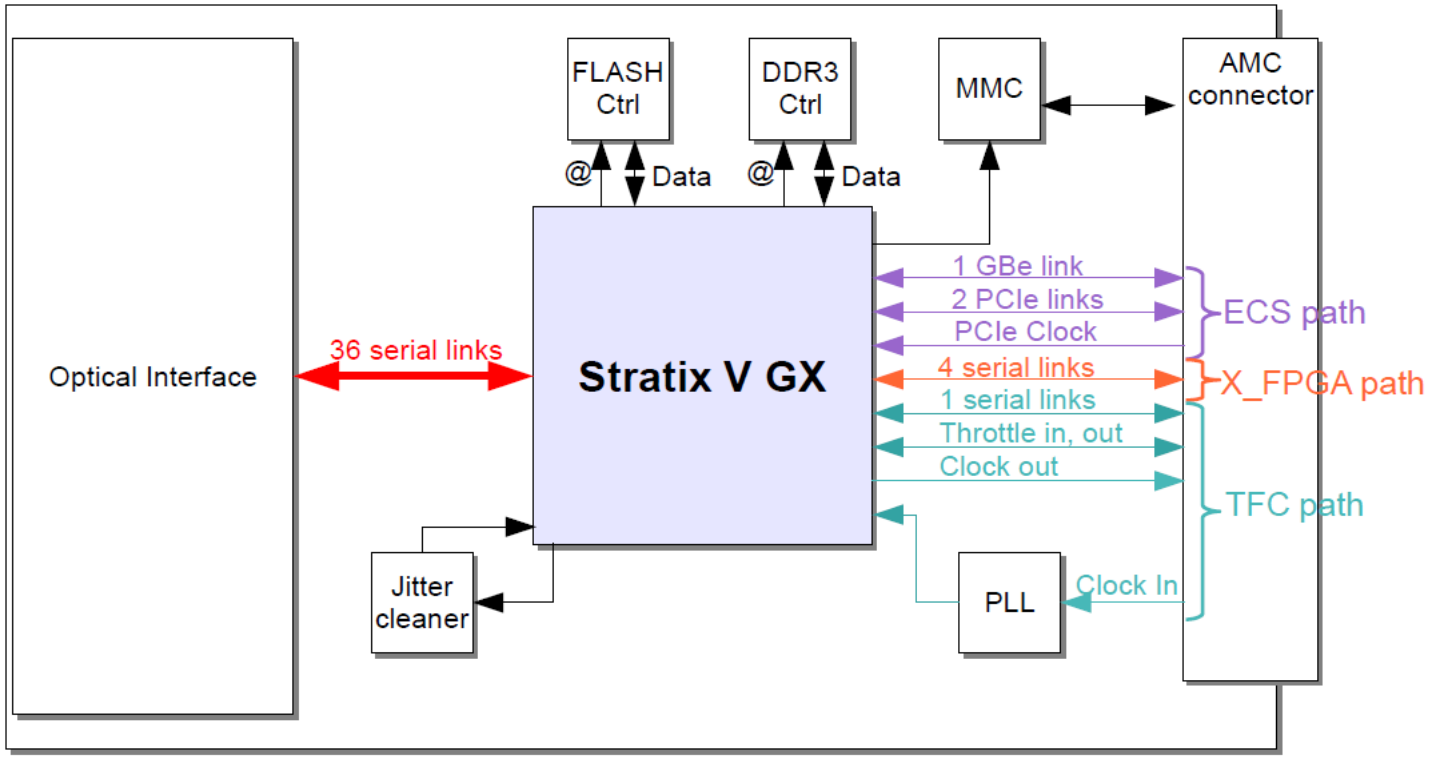
AMC40

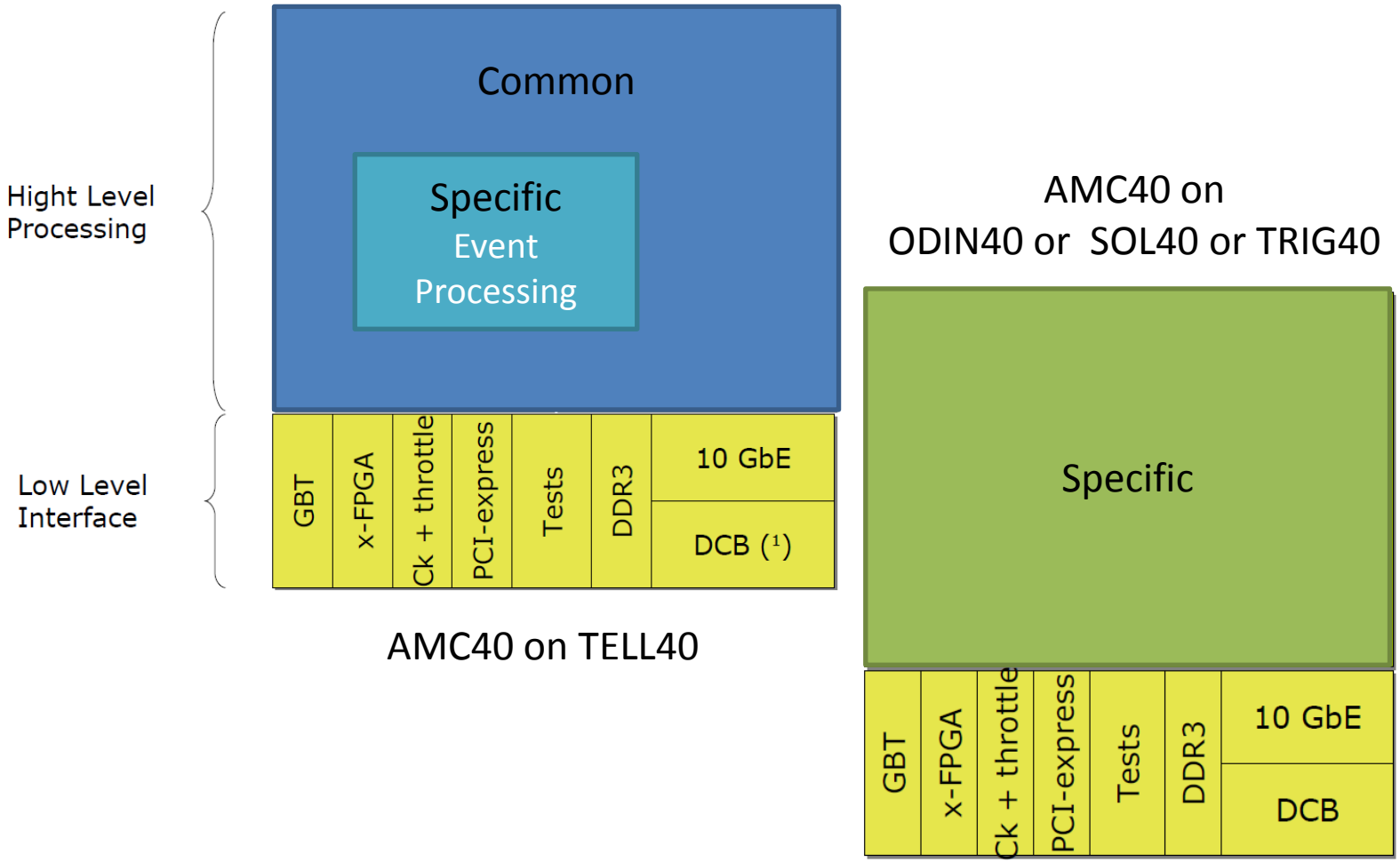


STRATIX V

Package	Stratix V GX								Stratix V GT		Stratix V GS					Stratix V E	
	A3	A4	A5	A7	A9	AB	B5	B6	C5	C7	D3	D4	D5	D6	D8	E9	EB
EH29-H780	✓										✓	✓					
HF35-F1152 (2)	✓	✓	✓	✓							✓	✓	✓				
KF35-F1152	✓	✓	✓	✓													
KF40-F1517 / KH40-H1517	✓	✓	✓	✓	✓	✓						✓	✓	✓	✓		
NF40 / KF40-F1517 (3)			✓	✓					✓	✓							
RF40-F1517							✓	✓									
H40-H1517																✓	✓
RF43-F1760							✓	✓									
NF45-F1932			✓	✓	✓	✓								✓	✓		
F45-F1932																✓	✓

The choice of the FPGA needs to be validated !!

STRATIX V firmware



Work Environment

- Mailing Lists (We need your contacts)

- Versioning (SVN, git ?)

- Twiki

- Bug tracking (To report the possible bugs)

  ➔ Forge Redmind

- Firmware development Tools

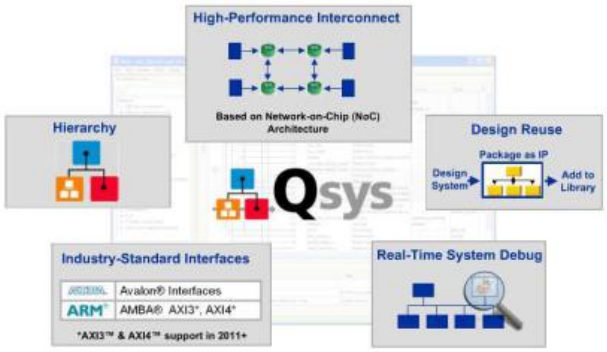
Firmware development

Needs

- A simple and unique development tool
- Clear separation between common functions and specific code
- Hierarchical approach
- Quick design
- Test bench for every developed function and for the whole board

→ **Quartus + QSYS**

QSYS



Powerful system integration tool

Save time by avoiding writing HDL code for interconnection

Mainly two kinds of interface

- Avalon **Memory mapped** interfaces**:**
  - Commands
  - Reading and writing of control registers
  - Memory control
- Avalon **Streaming** interface**:**
  - Data flow

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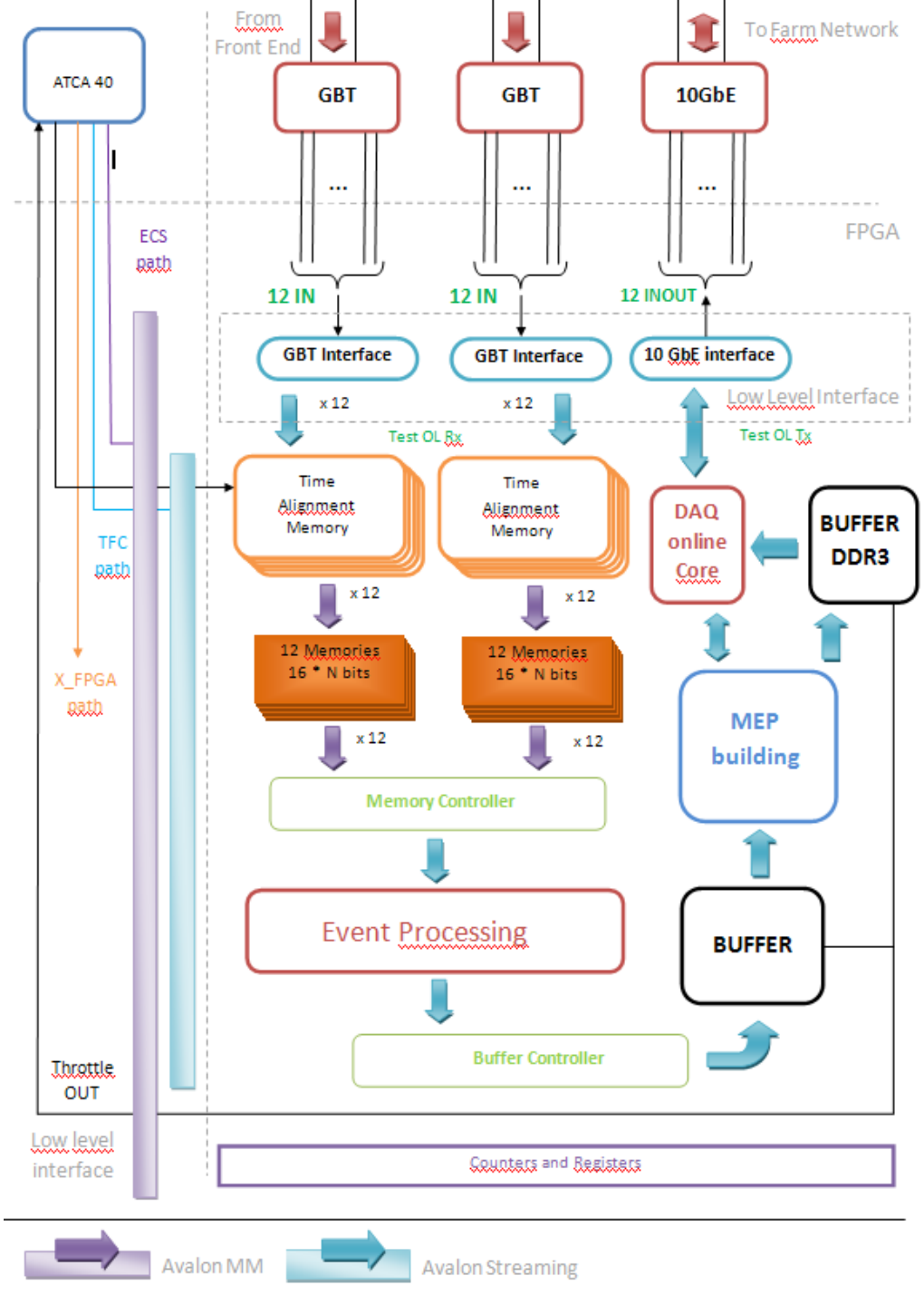
3. Methodology



Premilinary User Code architecture

To be discussed and improved with detector and DAQ requirements

Specification

- Low level interface (Marseille)

- TELL40 algorithm (LAPP)

- Specific user data processing (Each Detector)

What we need to know

Most important first :

- Contact list

We need to know who to contact and meet
to talk about the detector needs

Please send an email with a contact list to

→ guillaume.vouters@lapp.in2p3.fr

Then :

- Front End Header Structure
- Interfaces for the event processing bloc
- Data length max with NZS
- Etc …

We will try to meet you between January and February
to understand the detectors needs.

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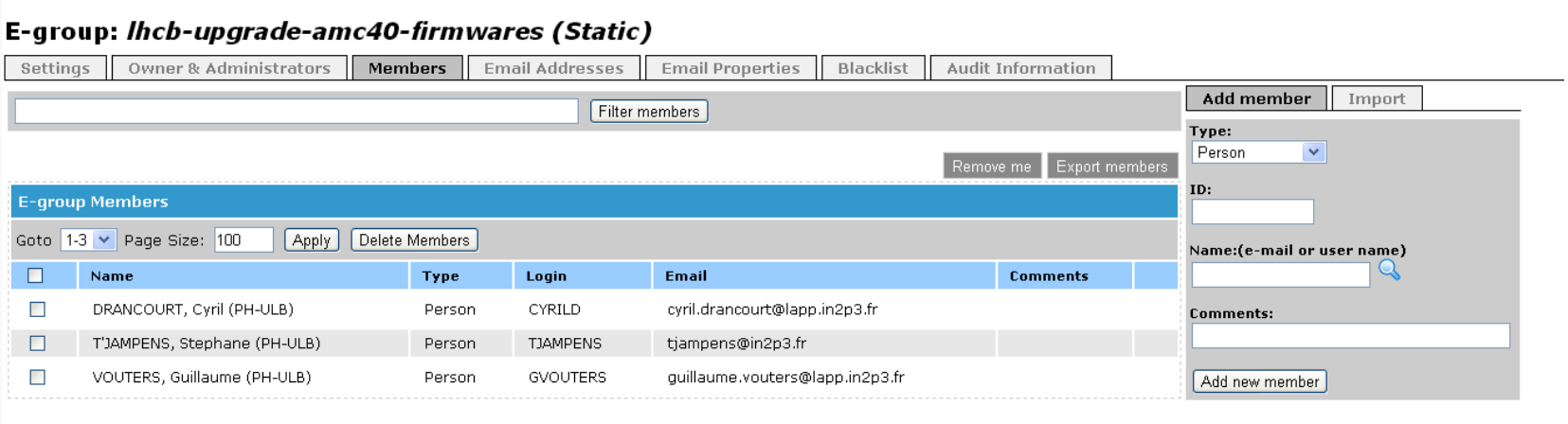
https://e-groups.cern.ch/e-groups/Egroup.do?egroupName=lhcb-upgrade-amc40-firmwares&tab=3



AMC40 firmware development Workshop

Planned on mid March 2013 at CERN

The purpose is to gather firmware developers to discuss in particular about :

- Work environment
- Development tools
- Specifications
- QSYS Blocks
- Interfaces

Conclusion

Coordination is needed as we need to work together as a Team

That means we need to see each detector group and the DAQ online one to understand the needs and manage to do something compliant and convenient for everybody.

We need to use the same environment (SVN, Twiki, Bug tracking) and tools (Quartus and Qsys)

A Workshop will be organized on mid March 2013

Thank you for your attention

Backup Slides

Beware !!

Compilation is tremendously long

→You need at least **20 Gb of RAM and 64 bits processor**

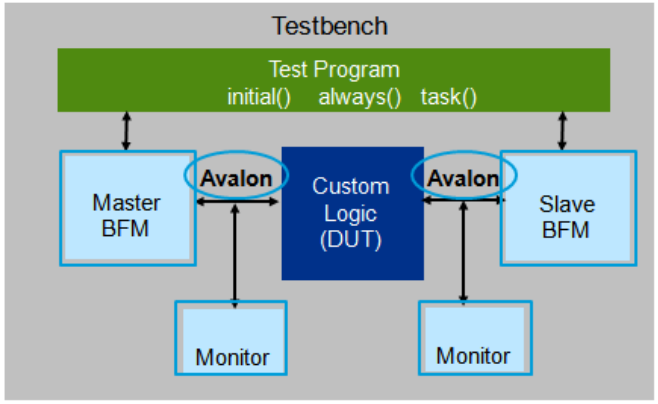
→ **32 bits does not compile !**

→ 4 cores or more strongly advised.

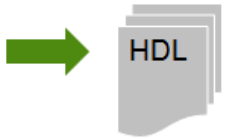
Tools

Test benches

- High level function calls through Bus Functional Modules (BFM)
- QSYS automatically generates a test bench



- Standard interfaces enable reuse of your testing environment
- Qsys provides a suite of verification IPs
- Qsys automatically generates a testbench



AMC40 Architecture