VELO upgrade Front-end ECS

LHCb upgrade electronics meeting

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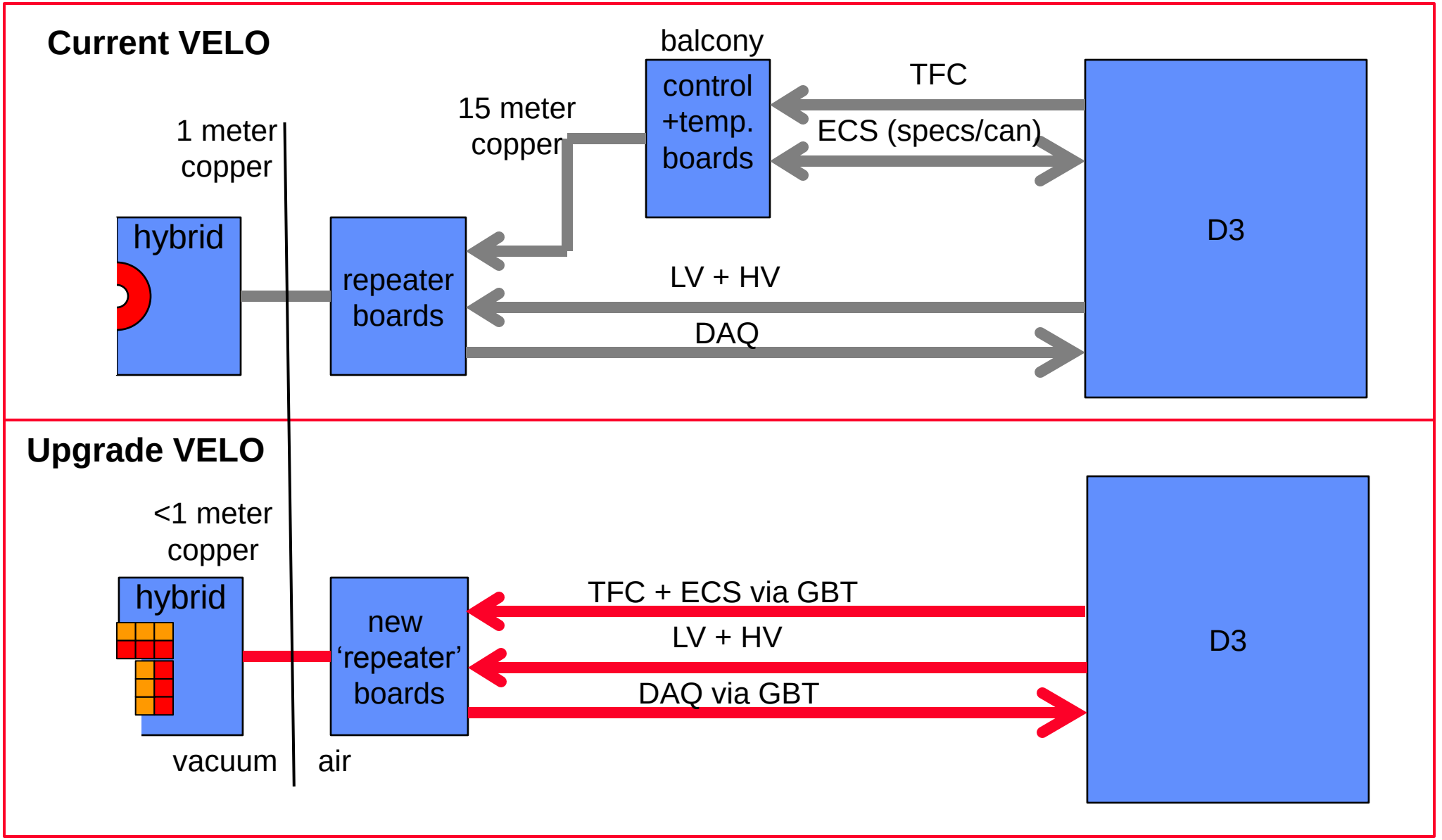
on behalf of the VELO upgrade group

Nothing is fixed, open for discussion

reminder 2 VELO upgrade options: Strips and Pixels

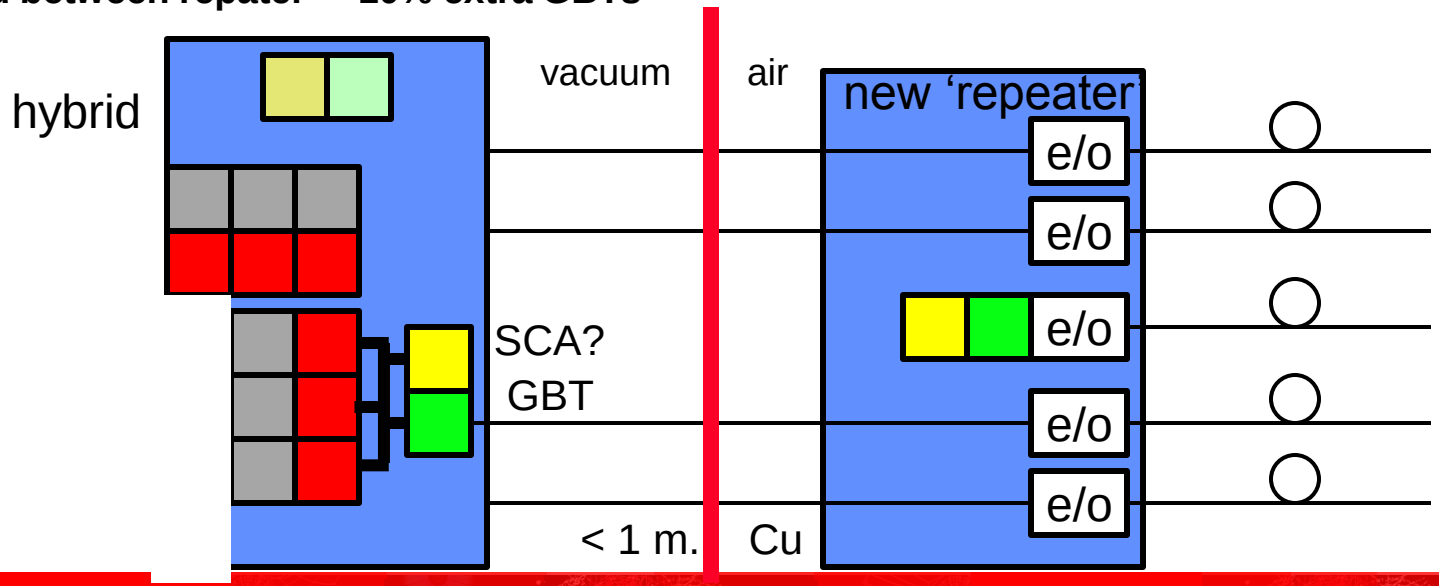
- Front-end chips are being designed for both a strip and pixel option
  - ECS interface not yet fixed, so open for discussion
- We have 21-26 stations depending on option
- 1 station = 2 modules, one on each side of the beam
- Strips: double sided module: 20 FE chips per side (R/Phi)
  - 2 halves * 21 stations * 2 sides (R/Phi) * 20 chips = 1680 chips, 128 channels each
  - So ~80 'boards/hybrids', 20 chips each
- Pixels: "single" sided module: 12 FE chips
  - 2 halves * 26 stations * 12 chips = 624 chips, 64k pixels each
  - So ~50 boards, 12 chips each
- In the following I will mainly show the pixel option (unintentional bias)
  - Interface & configuration for strip option is same as other (silicon) detectors
  - Pixel option is more demanding in terms of number of configuration bits

Location of front-end electronics



Baseline: GBT+SCA on hybrid

- Electrical -> Optical conversion on air side
- Copper link at 4.8 Gbit/s to GBT chip vacuum tank
- Pixels: 1 GBT per 6 VeloPix chips -> 2 GBT for ECS per 'hybrid' -> ~100 in total
  - individual clock per VeloPix (low jitter)
  - common TFC signals? (GBT driving capabilities)
  - configuration via GBT e-link? (next slide)
- Strips: 1 GBT per hybrid? -> ~ 80 GBT for ECS in total
  - clock buffering / jitter ?
  - I2C protocol (16 times I2C per SCA, 20 needed)
- Common: additional ECS GBT needed for monitoring temp, power on 'repeater'
  - GBT shared between repater ~10% extra GBTs



Question

- Do we want/need a SCA on the Pixel hybrid?
- From the VeloPix chip design point of view we prefer ‘direct’ e-links for configuration
  - SPI-like protocol (close to TimePix3)
  - Discussion with chip designers ongoing
- Need a dedicated meeting with ECS (and TFC) responsibles to discuss the possibilities
  - So this is only an advance warning….

Data volume

- It is too early to give final/detailed numbers, so estimates only
- Pixel matrix configuration ~1 byte per pixel -> 64k per chip -> ~300-350 kByte per GBT link -> 60 – 70 MByte for whole VELO
  - minimum data size on single address: ~512 bytes due to serial shifting in matrix
  - but could also opt for 64k in one go -> buffering in SOL40?
- Pixel periphery: 20 – 30 registers, 8 – 32 bits wide
  - DAC registers
  - Various counters (e.g. SEU)
  - Voltage/current/temperature monitors
- Strips will have much less config data:
- 2560 strips per GBT instead of 320k pixels, and few bytes per strip instead of 1 -> 10 kByte per hybrid? -> ~ 1 Mbyte in total?
- Strip periphery registers: comparable to pixels I guess
- Monitoring rate 1 Hz -> Volume < 1 kByte/s/GBT (t.b.c)
- GBT on Repeater: V / I / T monitoring only -> several tens of addresses
  - I2C protocol (t.b.c.)

BACK-UP SLIDES

Issues that need further study

- **Configuration protocol**
  - Pixel: SPI-like preferred
  - Strip: I2C (t.b.c.)
  - trade-off: speed vs complexity
- **How to handle the chip calibration (threshold equalization)**
  - requires (long) sequence of
    - set mask
    - scan threshold and take data
  - Will take almost forever with standard PVSS stepping mechanism
  - -> Add specific features to VELOpix to speed up this process
  - Want possibility to read out data via e-links
  - How substantial volume … 64 kByte (1 byte counter per pixel)