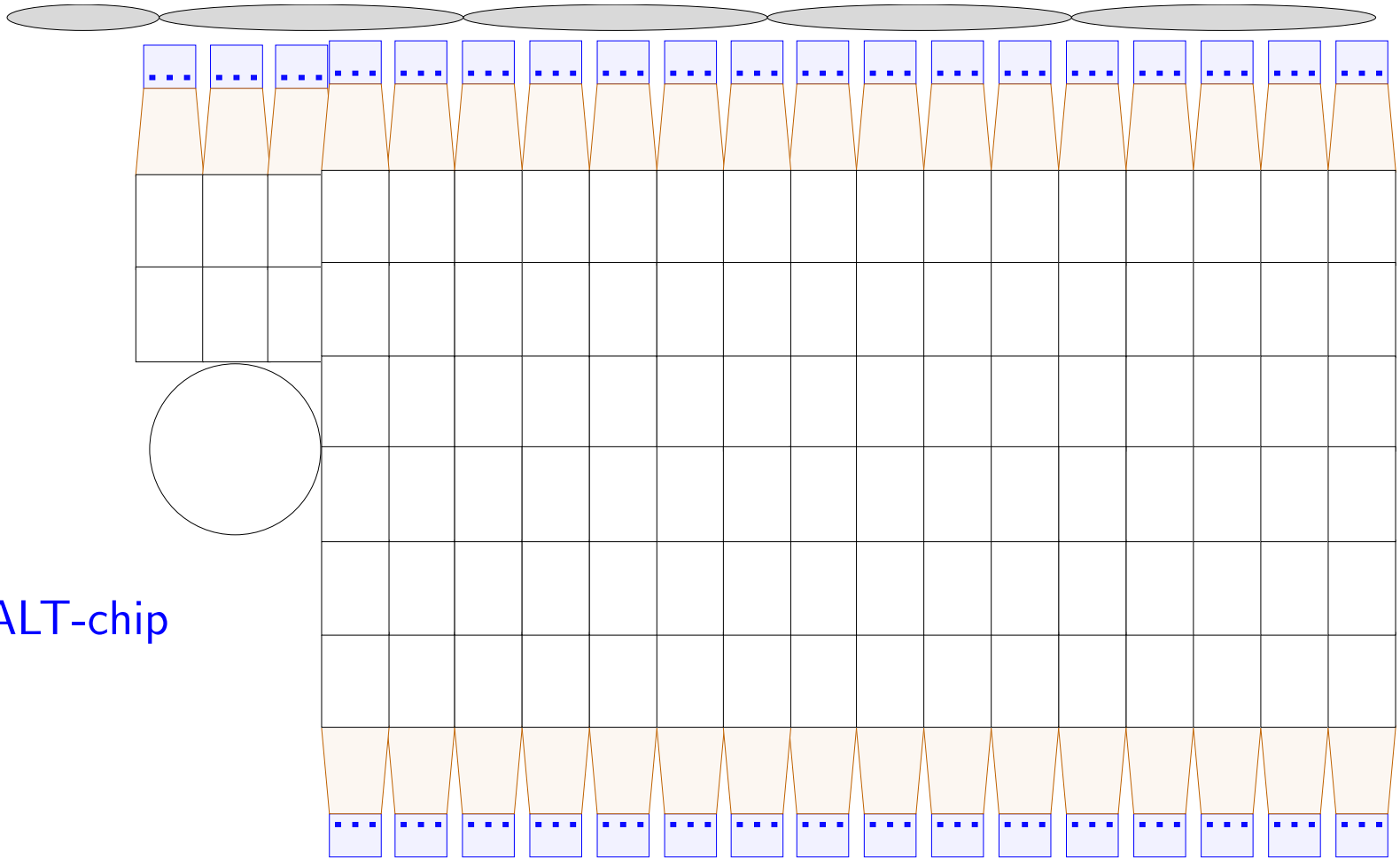
# Si-IT and ECS

- Detector "size" reminder
- Questionnaire

# Upgrade Si-IT



- 128 channels/SALT-chip
- 3 SALTs/hybrid
- 70 hybrids/layer
- 10 layers
- 2100 FE-chips.

# Questionnaire: Si-IT

2 Number of GBT Links: ∼400 (have to work out patch panel..)

3 Number of FE Boards (/Service Boards):
700 VFE-boards: hybrid with 3 chips ←∼ 2.5 m→Service-board
40 Service-boards: 1 master GBT, 20 SCA(1/hybrid?), 10 GBT-links.

4 Number of SCA chips per masterGBT: 20 (if 1 SCA/hybrid)

5 Number of User buses per SCA chip: 1 (if 1 SCA/hybrid/3-SALT-chips)

6 Type of User buses used: I2C

7 Number of registers per VFE Board: 384 channels, all need:
8-bit pedestal
8-bit threshold
1-bit mask
some set-up currents/voltages etc.. Hence: ∼10 kbit / VFE-board.

8 Data volume per VFE Board for configuration: 10 kbit

9 Data volume per VFE Board for monitoring (and how often):
Voltage/temperature etc.. Less than once/minute: 1 bit/s?