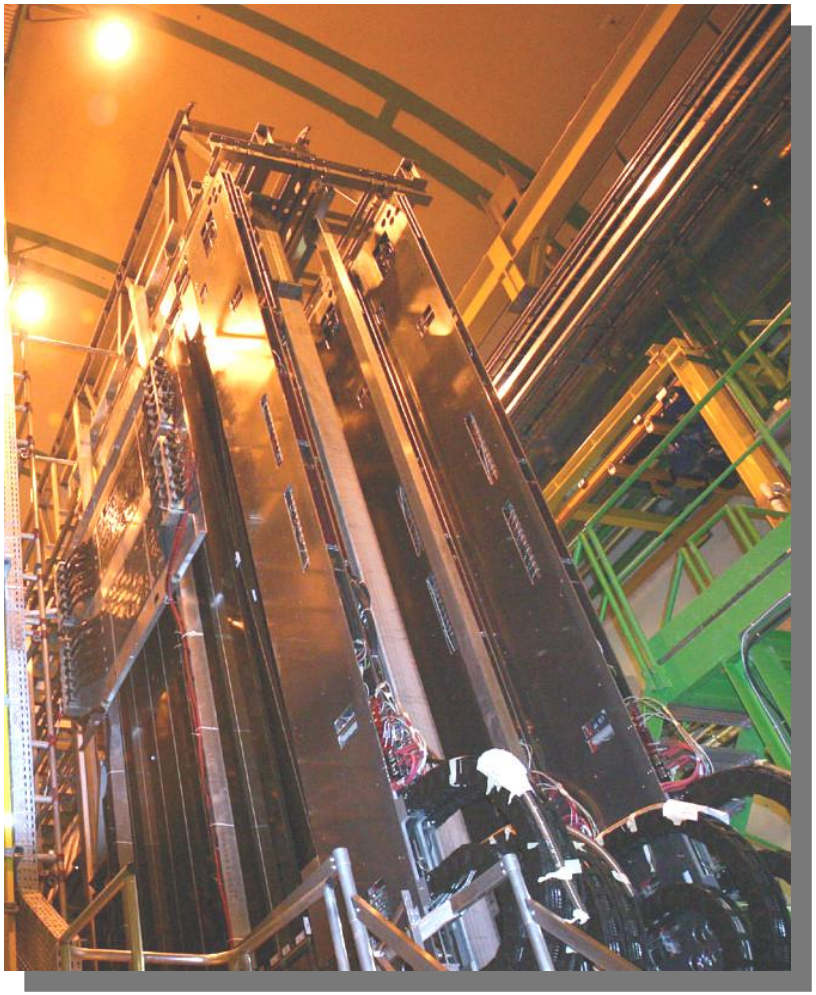
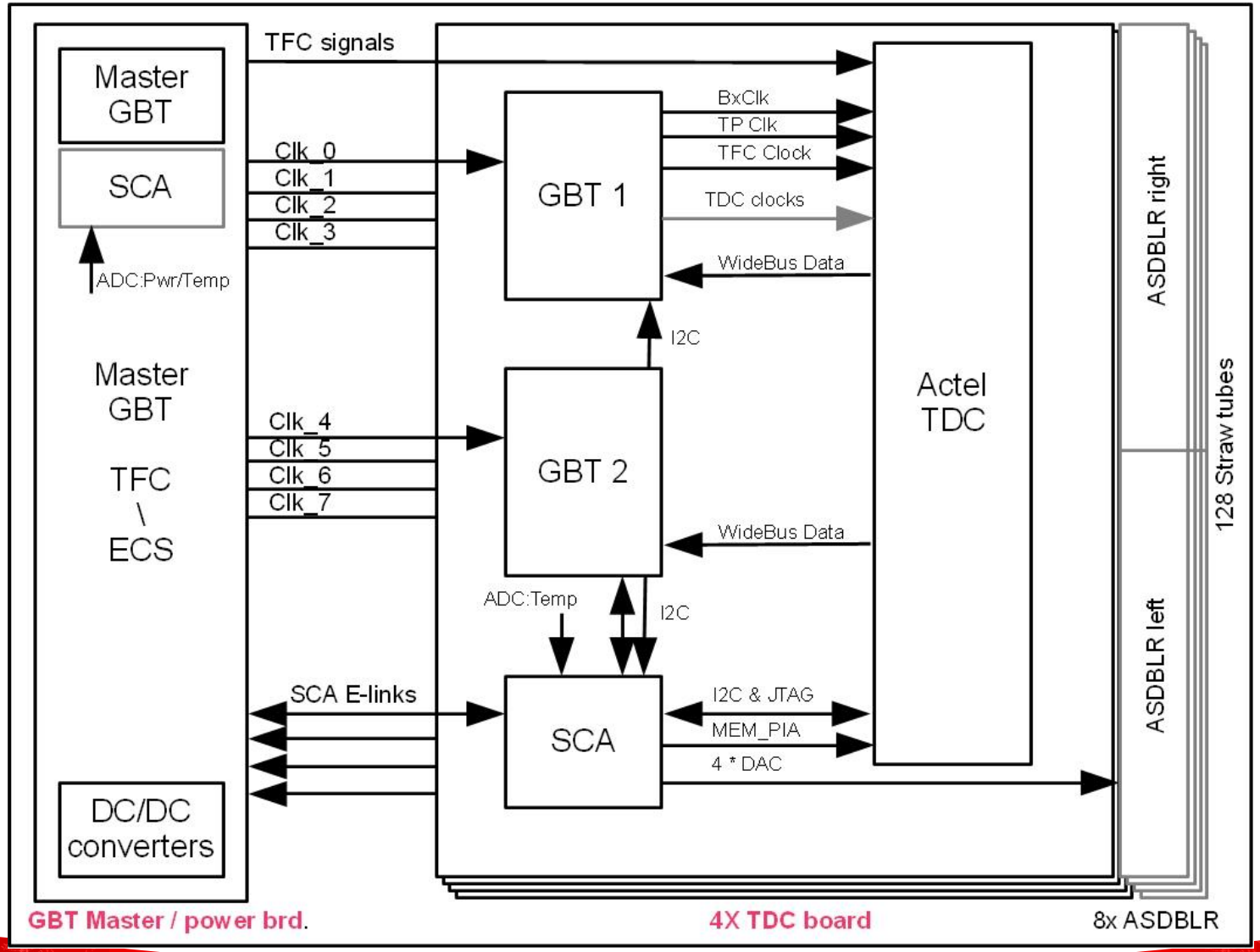
LHCb Outer Tracker Upgrade ECS interface

- Outline
  - Front end box Architecture
  - SCA User buses
  - Registers
  - Configuration before run
  - Monitoring during run
  - Additional registers
  - Two other upgrade scenarios

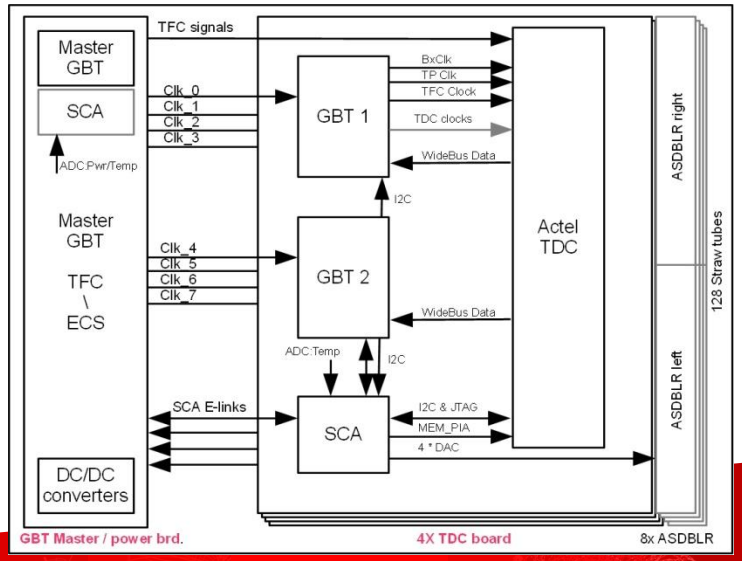


Front-end box ECS/TFC architecture



Front-end box GBT&SCA

- 432 Front end boxes, each:
  - 1 GBT master/power board (replaces: GOL board)
    - Referred as "service board"
    - 1 Master GBT (hardwired configured, except clocks)
    - 1 SCA for monitoring (power, temperature, etc.)
  - 4 Actel TDC boards (replaces: OTIS boards)
    - 2 data transmitter GBT's
    - 1 SCA (Actel TDC conf. GBT conf., monitoring)
  - 8 ASDBLR boards (unchanged)
- Total:
  - 3888 GBT's
  - 2160 SCA's



SCA User buses

- SCA per TDC board (1728 TDC boards)
  - 3 × I^2C (two GBT's, 1 Actel FPGA)
  - 1 × JTAG, (re-)program Actel FPGA
  - 4 × DAC, ASDBLR thresholds
  - 2 × ADC, (temperature monitoring)
  - 4 bits MEM-PIA, (power-up resets via ECS)
  - Total User buses: 4 SCA's, with 7 buses per SCA
- SCA master/power board(432 TDC boards)
  - 16 × ADC (temperature , voltage, current and magnetic field monitoring)
  - Total: 1 user bus (I assume only 1 bus per ADC?)
- Total per FE box:
  - User Buses: 4 × 7+1=29

Registers per FE Box

- 9 registers per Actel TDC (36 per FE)
  - Channel mask (R/W), Instruction (R/W), Status (R/W), Seu count (R), Rst Count (R), Spy memory (R), Bcnt offset (R/W), TFC offset (R/W), Address/ID (R)
- 60 SCA registers:
  - 27 ADC, 16 DAC, 16 MEM-PIA
  - JTAG: 700kBytes

GBT registers not completely known yet (needs some iteration)

- GBT registers
  - 8 data GBT's
    - 4 GBT × 3(to 8) clock delay settings
    - Wide-bus mode
    - …
  - Master GBT
    - 8 clock delay settings
    - Master ECS/TFC mode selected (hardwired/burned?)
    - …

Data volume for configuration

- Per FE box:
  - Actel TDC registers
    - 16 bytes channel mask
    - TFC delay 4 × 1 byte
    - Bcnt Offset 4 × 2 bytes
    - Status write 4 × 2 bytes (resets counters/fifo's, soft reset)
    - Instruction 4 × 2 bytes
  - SCA registers:
    - 16 Threshold voltage DAC's : 16 Bytes
    - 8 × lda-tia (versatile link) ?? ~16 Bytes (if needed: bias, modulation current)
  - GBT registers
    - data GBT's × 3 (to 8) clock out conf. ~64 bytes
    - data GBT's in wide bus format conf. ?? bytes
    - Master GBT: 8 clock out conf. ~64bytes
    - Master GBT: configuration/mode
- Preliminary estimate per FE box:
  - 76 Bytes + GBT bytes
- Total OT: 32832 Bytes (SCA) + ?? (GBT's, probably ~2 times more)

Data volume for monitoring

- Per FE box: Monitoring (say ~1Hz)
  - Actel TDC
    - SEU counter, 4 × 4 bytes
    - Reset counter, 4 × 4 bytes
    - PLL loss of lock counter, 4 × 4 bytes
    - Status, 4 × 2 bytes
    - Address/ID, 4 × 2 bytes
  - SCA (ADC's times 12 bit)
    - Magnetic field sensor: 1
    - Temperature,:5 × 2
    - Voltage: 7
    - Current: 7(shunt)
  - GBT status
    - Unknown (SEU, error counters, status ??)
- Total per FE box:
  - 102 Bytes + "??" (GBT)
- Total OT: 44.064 Bytes/s + ?? (GBT's, presumably smaller)

And don't forget…

- Per FE box: Debugging (thus hopefully seldom used!?)
  - Actel TDC spy registers
    - FIFO 56bits × 16pos per 16 TDC channels (8 registers)
    - Total: 896 bytes per FE box
- Actel Proasic3e firmware programming
  - Only during technical stops -> no time limitation
  - Re-programming via JTAG
  - One ~700kByte bitstream
    - Is SCA capable of handling large bitstreams ??
  - Single JTAG operation needed
    - Segmented programming not supported by Actel (I asked)
  - Can SCA->JTAG speed be limited ??
    - Programming flash memory, limited speed
  - Goal: firmware the same for all 1728 Actel devices
    - Possibility to specify >1 firmware types for debugging purpose ?
  - CCPC Jam Stapl player: SCA alternative ??

Two other OT Upgrade scenarios

All I said is valid for the "Nikhef" OT-straws electronics upgrade!

Notice that:

- There is an alternative straws-electronics upgrade design (Heidelberg) based on Altera FPGA's
  - I guess that number of registers and data would globally be ~same
  - Re-configure of Altera firmware needed during run??
    - ~1 device per minute
    - Multiple techniques, scrubbing complete re-programming
- If part of the straw modules are replaced by SCIFI modules and only ~50% of straws electronics is upgraded
  - Number of registers un-changed
  - Data volume decreases

Spare slides

Actel TDC I²C register details

- Preliminary!

Device	Register	I2C addr.	Register Sub-addr.	R/W	Length (bytes)	Def. Value
Actel TDC	Revision ID	10h	00h	R	4	-
	Instruction	10h	01h	R/W	2	0
	Channel mask	10h	02h	R/W	4	FFFFh
	Status/Reset	10h	03h	R/W	4	-
	Spy data lo	10h	04h	R	7*16	-
	Spy data hi	10h	05h	R	7*16	-
	Counter Seu	10h	06h	R	4	0
	Counter Bcntrst	10h	07h	R	4	0
	Offsets	10h	08h	R/W	4	0