VICTR testing

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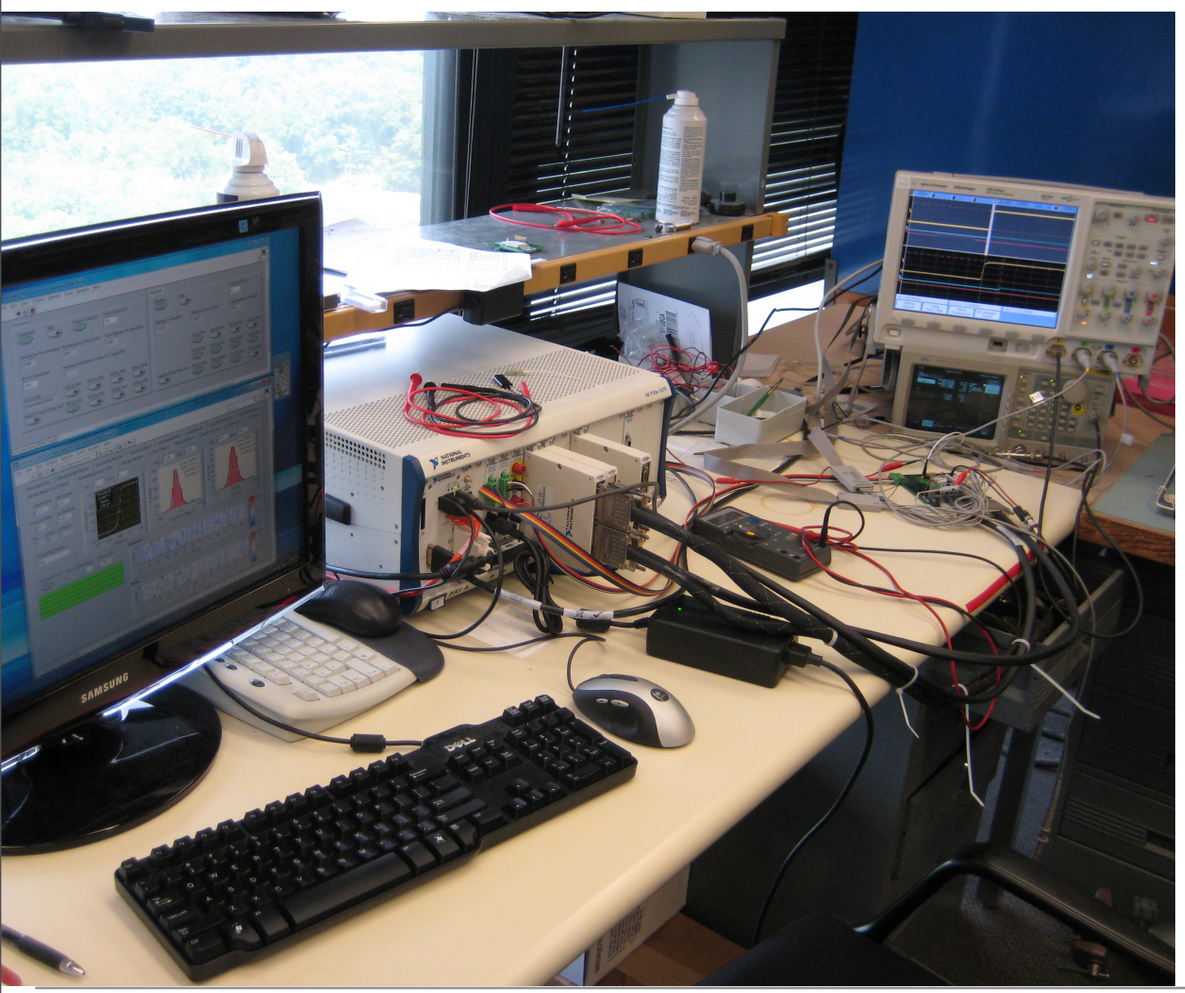
Outline

- Review past tests
  - Time walk
  - Turn-on curves
  - Threshold & noise maps
  - Threshold tuning
  - Cross-talk problem
- Recent progress
  - Power requirements
  - ASD characteristics
- Future plans

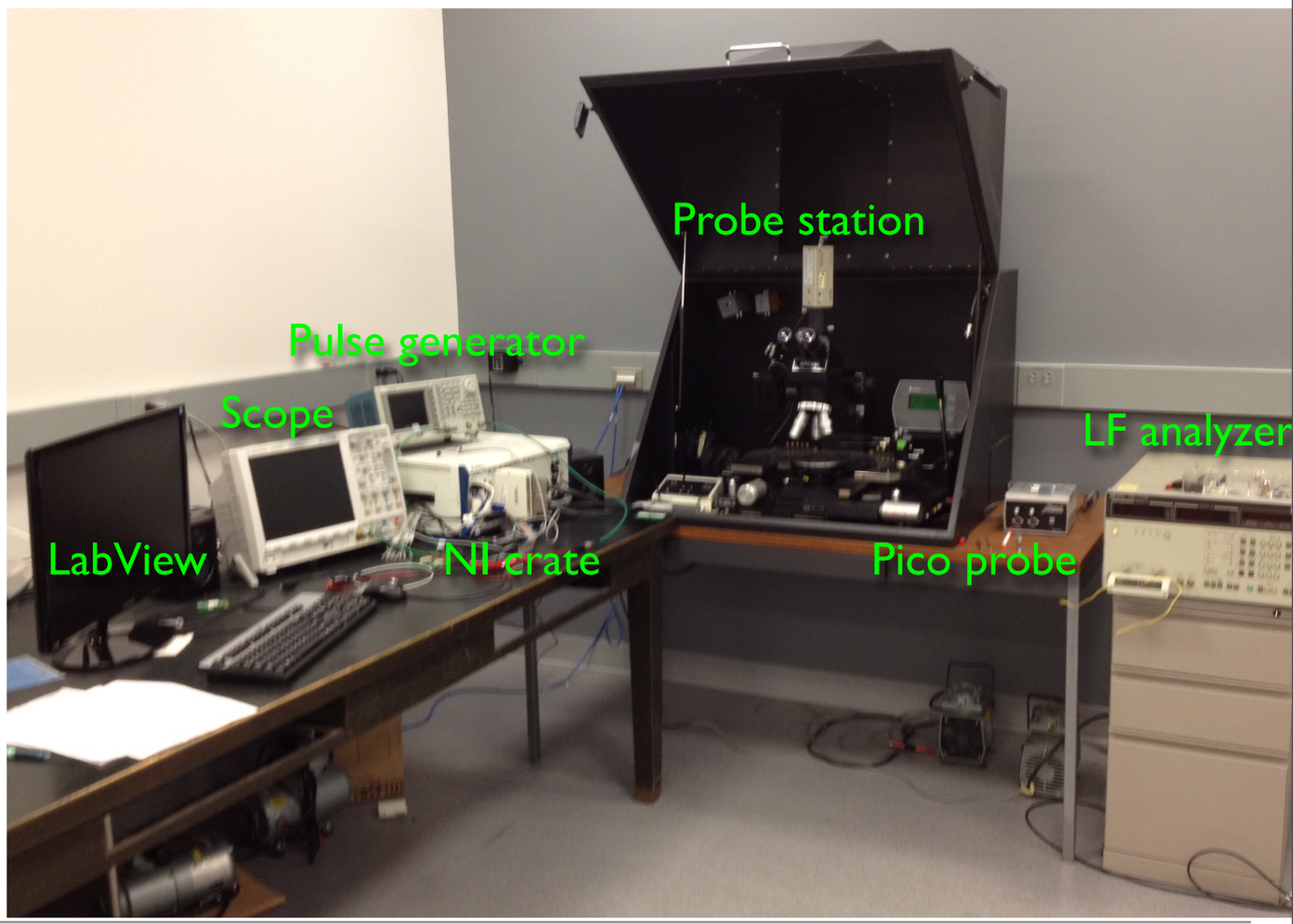
Test stands

- National Instruments FlexRIO system with FPGA
- We have test stands at FNAL and now at Cornell
- I'm continuing doing tests from Cornell

FNAL

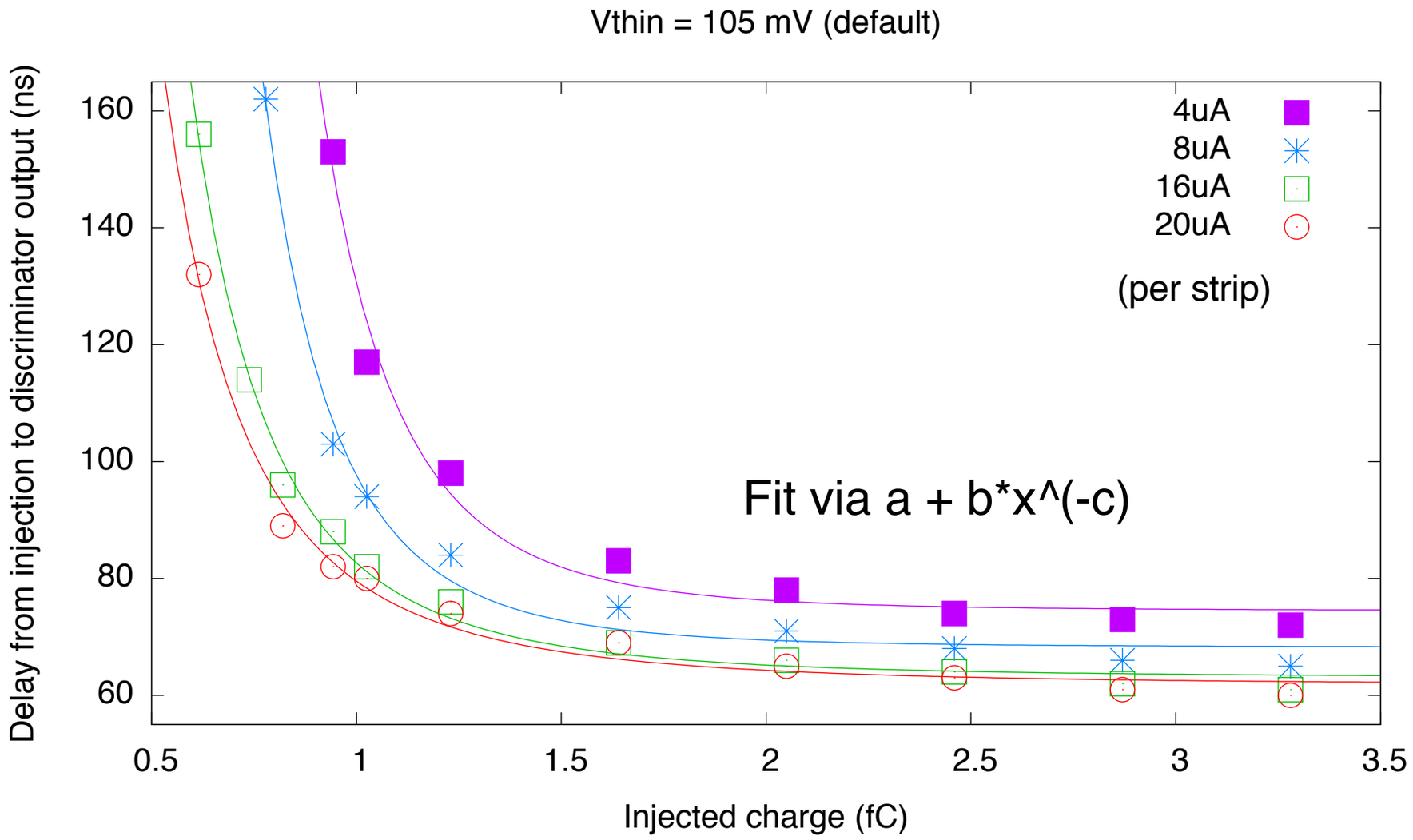


Cornell



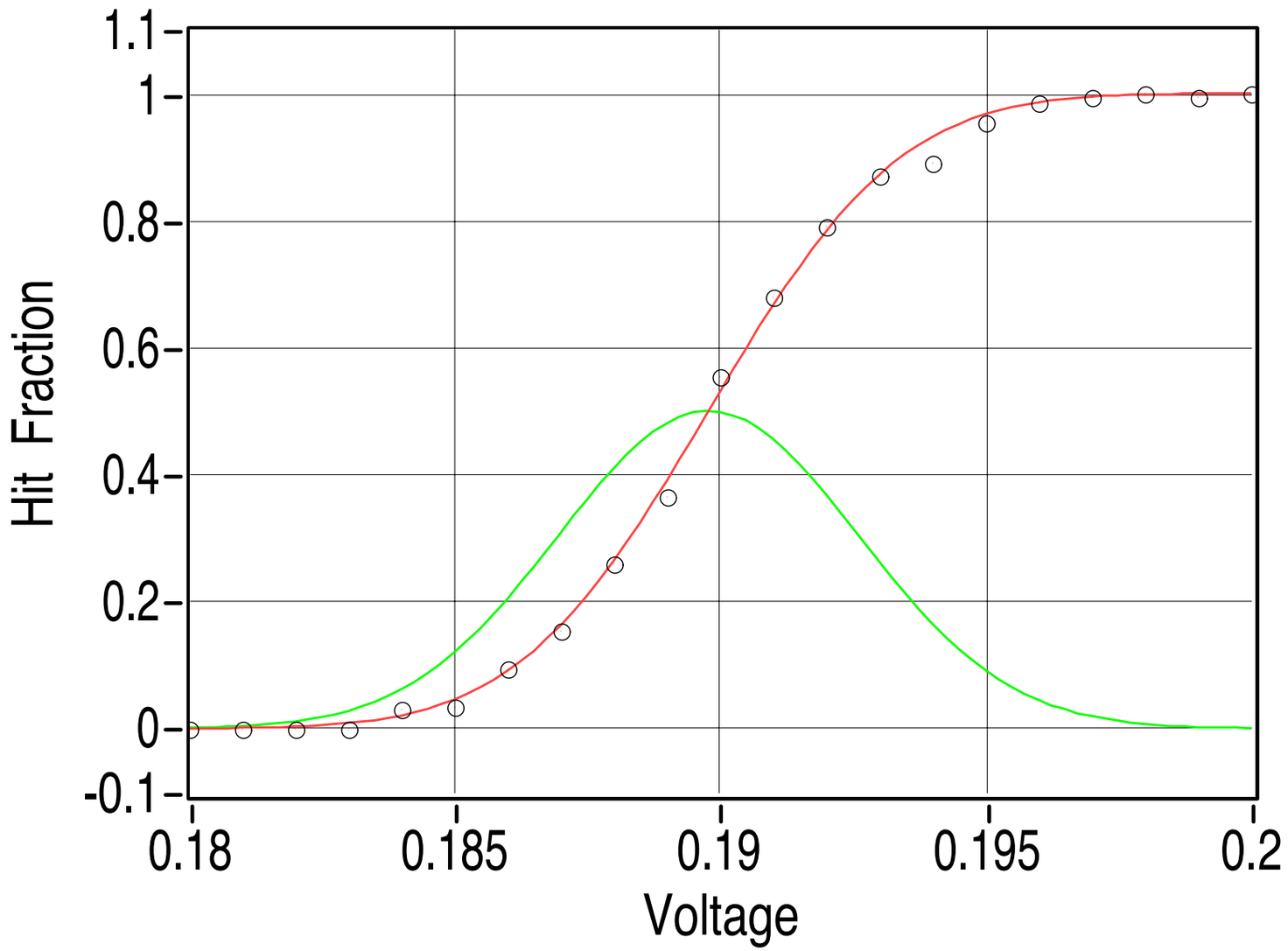
Time walk measurements

- Looking at a single strip, inject charge with a square wave and scan over voltages
- Convert the voltage to amount of charge assuming the design capacitance of the charge injection capacitors
- Measure with a scope the time delay between the charge injection and detection
- Multiple curves: Vary the preamp bias voltage to adjust the front end bias current



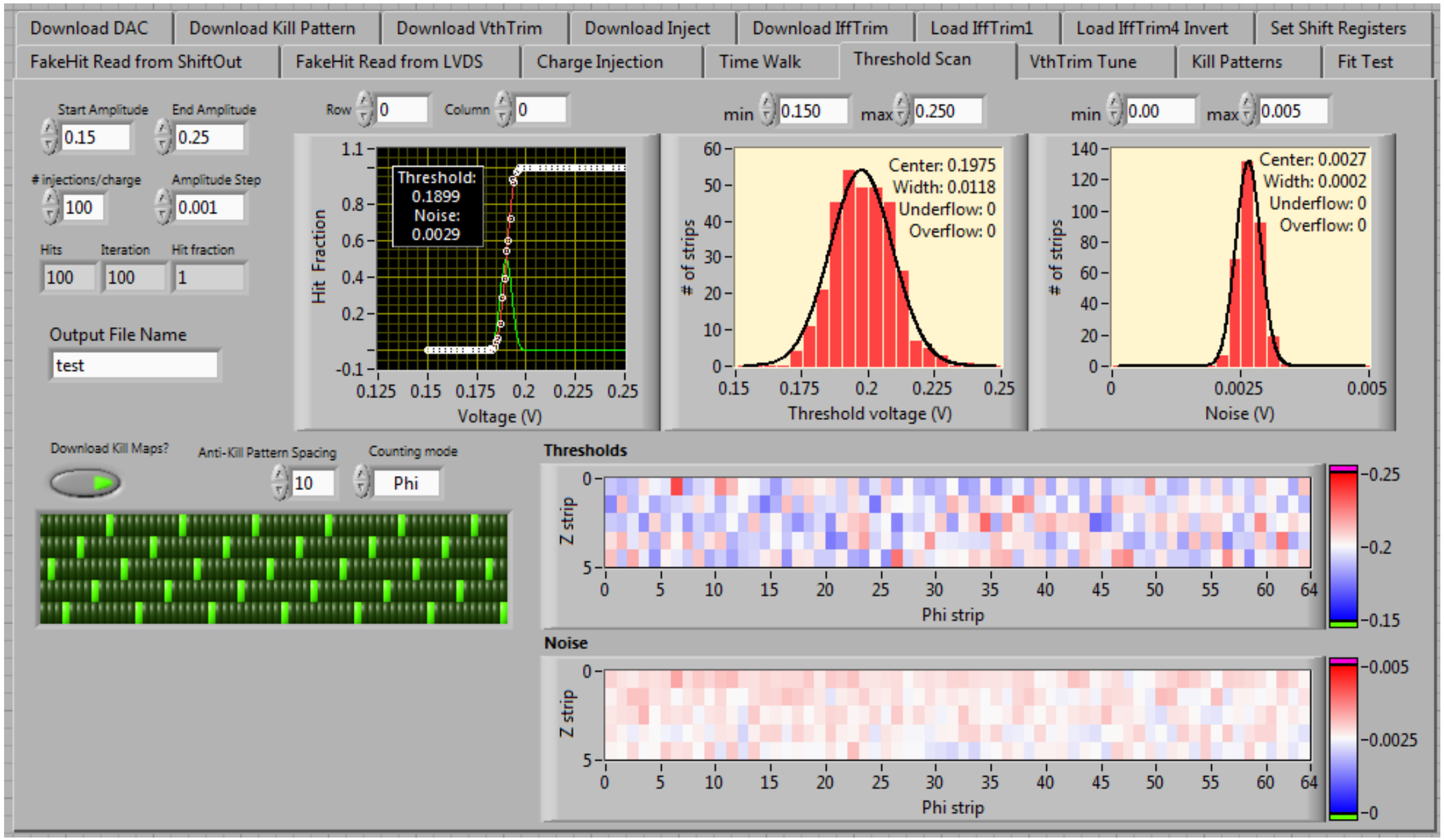
Turn-on curves

- For each charge injection voltage value, inject the charge many times and count the number detected
- Fit data to a cumulative gaussian
  - Width of the gaussian gives a measure of the noise



Threshold scans

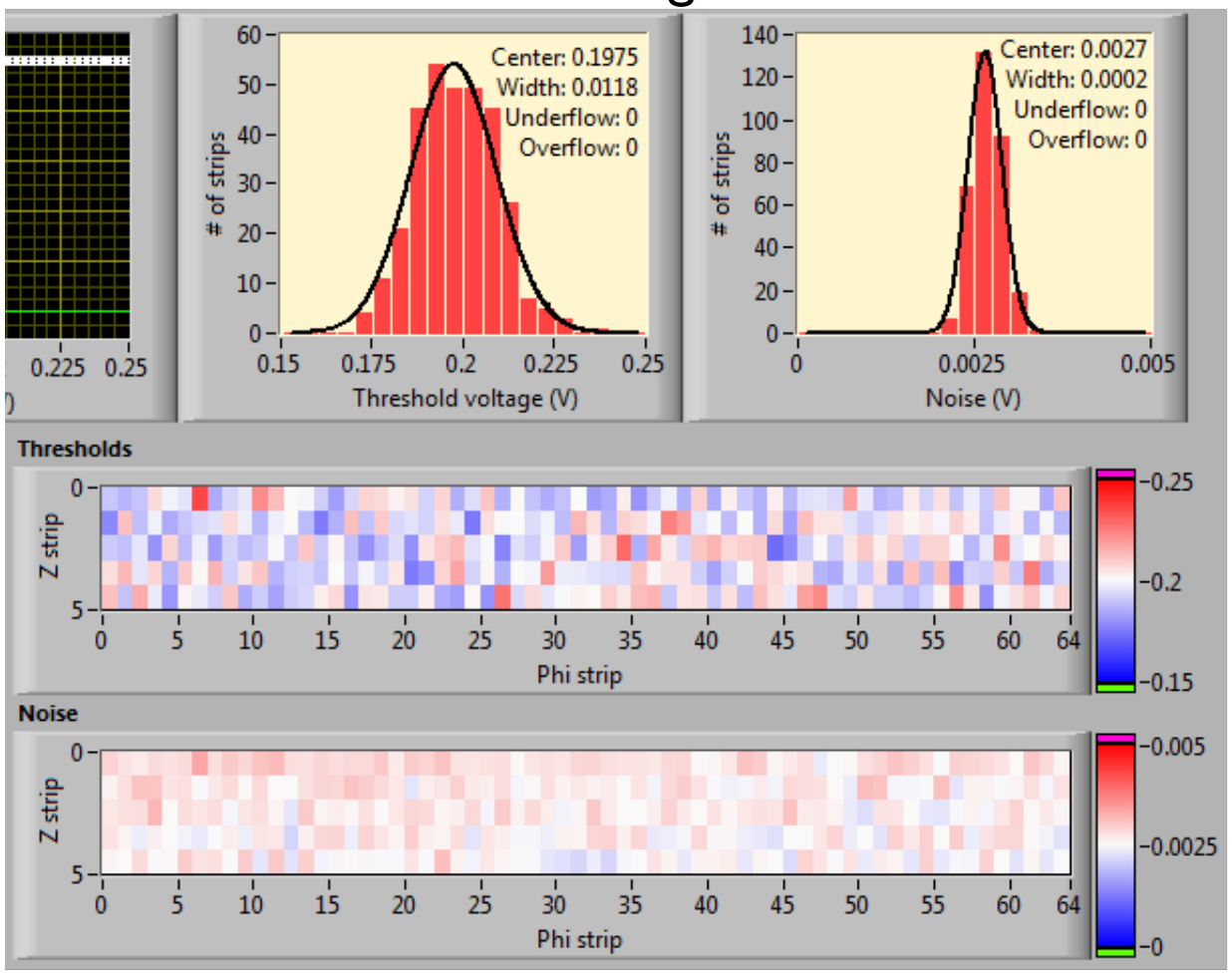
- Collect the turn on curves for all the strips
  - Able to control which strips are activated at the same time, to study cross talk effects
- Display histograms and 2D maps of the threshold and noise values
- Do not see any strong systematic effects. Looks good.



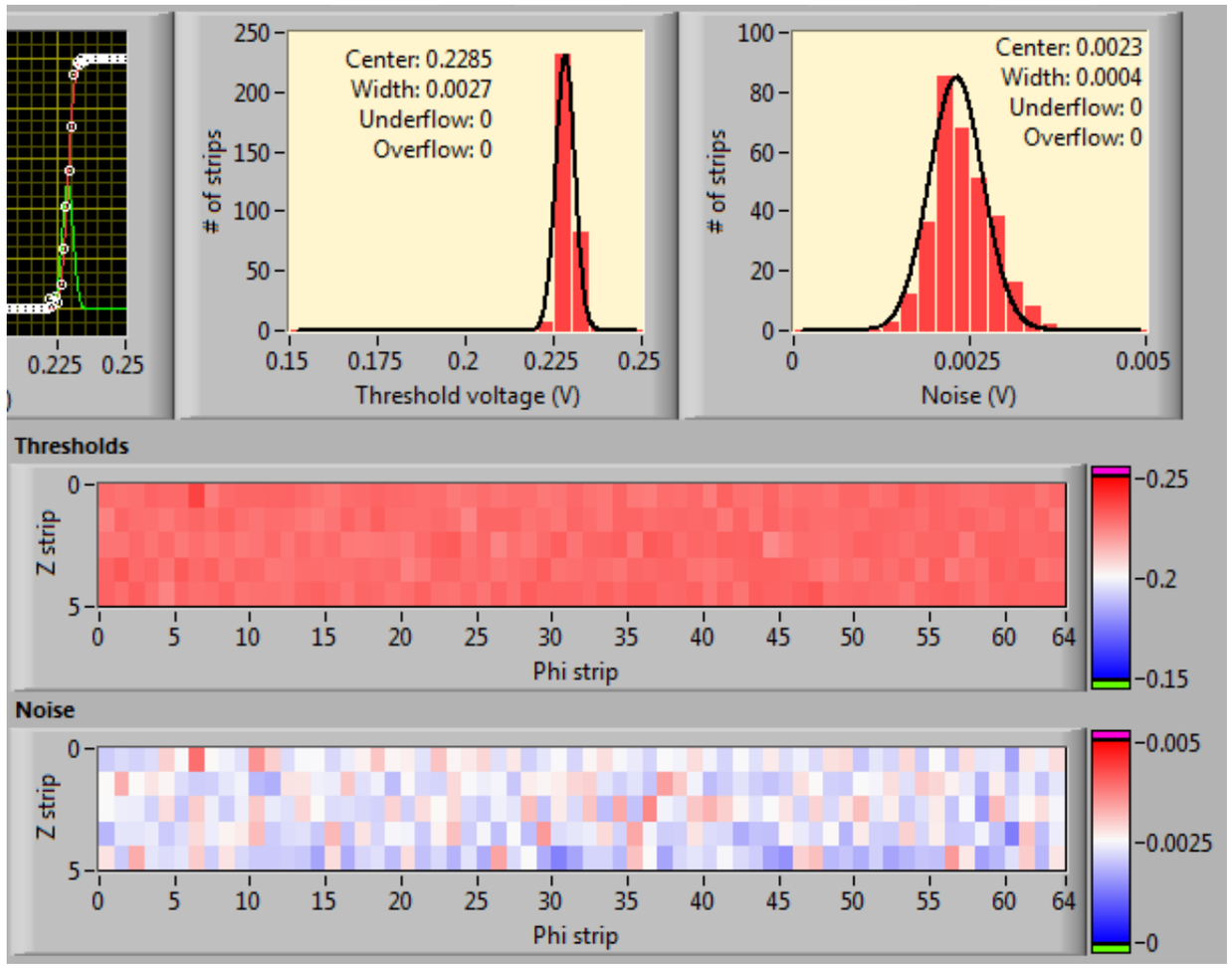
Threshold tuning

- We would like all strips operating at the same threshold
- Each strip has a variable 5-bit threshold trim
- After tuning: threshold distribution width goes from ~12 mV to ~3 mV
- Can be done iteratively
  - ~ 3 mV → ~ 1 mV

No-trimming

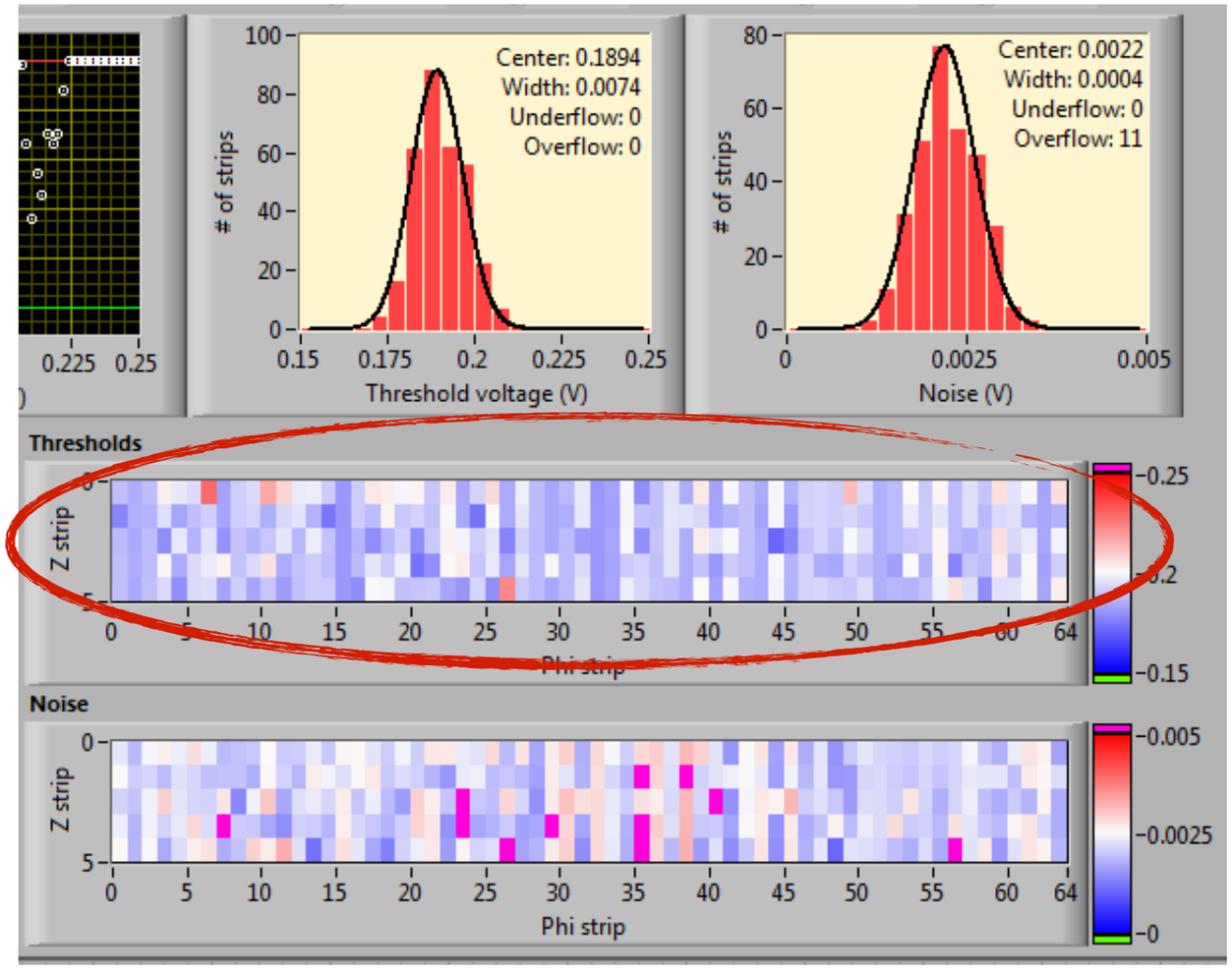


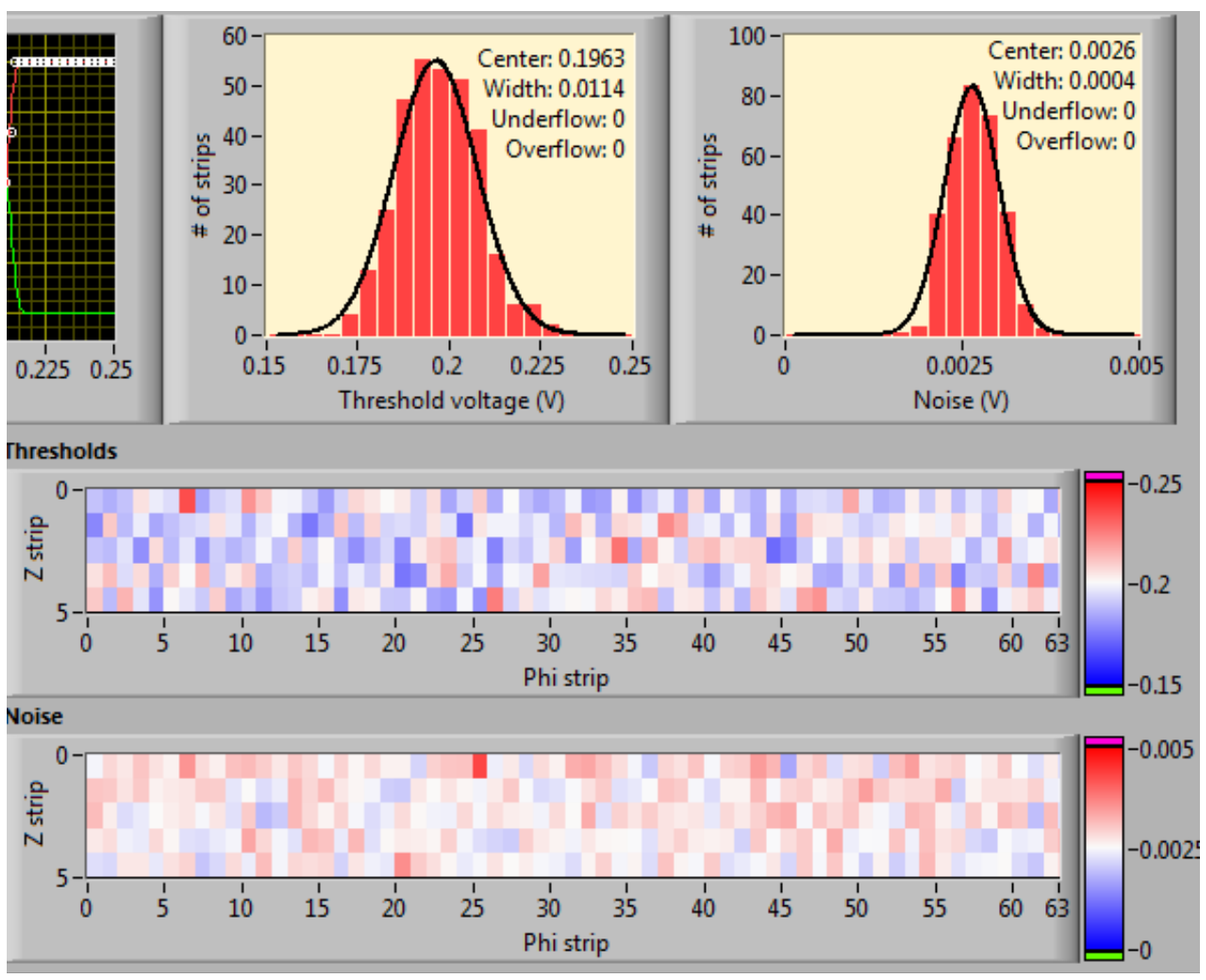
Tuned once



Crosstalk problem

- We see a difference between the measured threshold maps when all strips are all activated at once (left) versus activated in isolation (right):

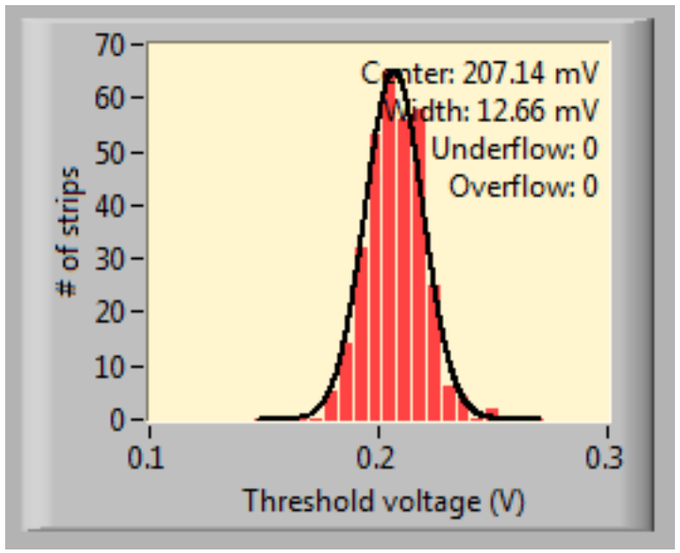


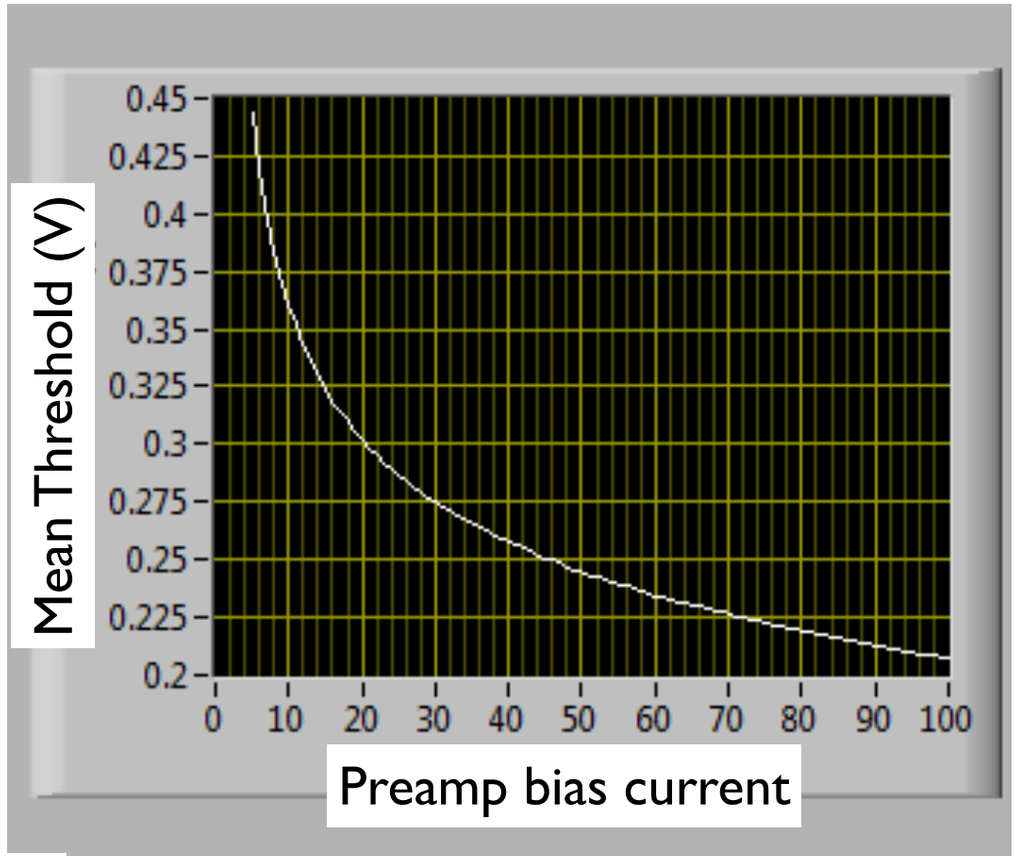


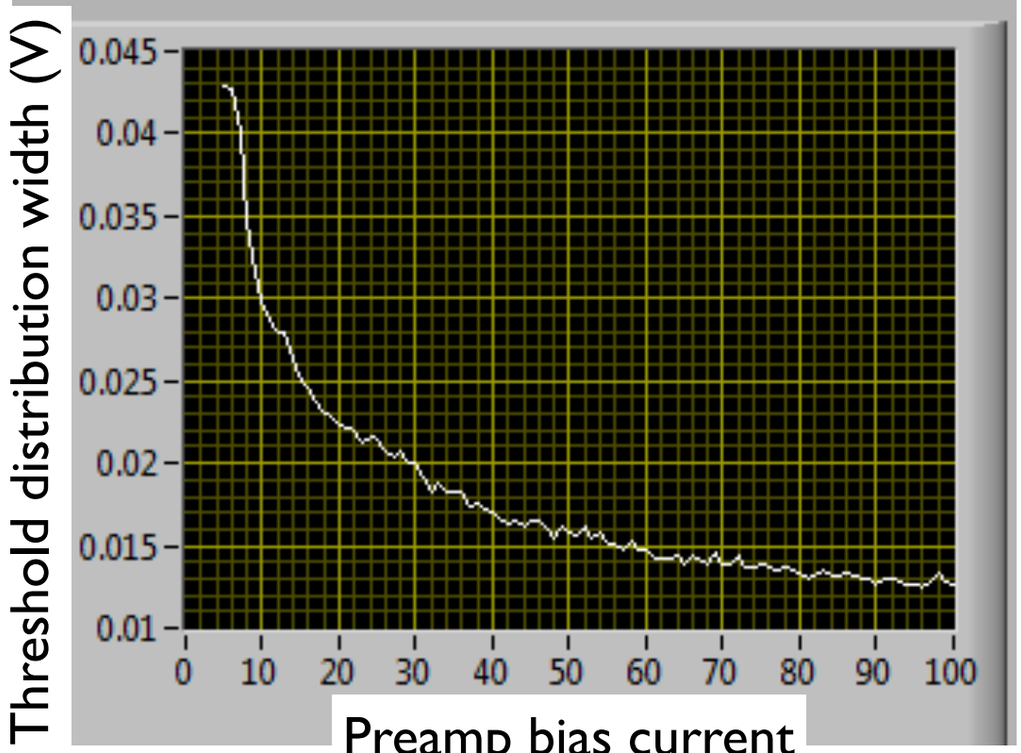
- Likely a problem with the layout. Add shielding in future version

Power requirements

- Q: How much power needs to be supplied to achieve required sensitivity?



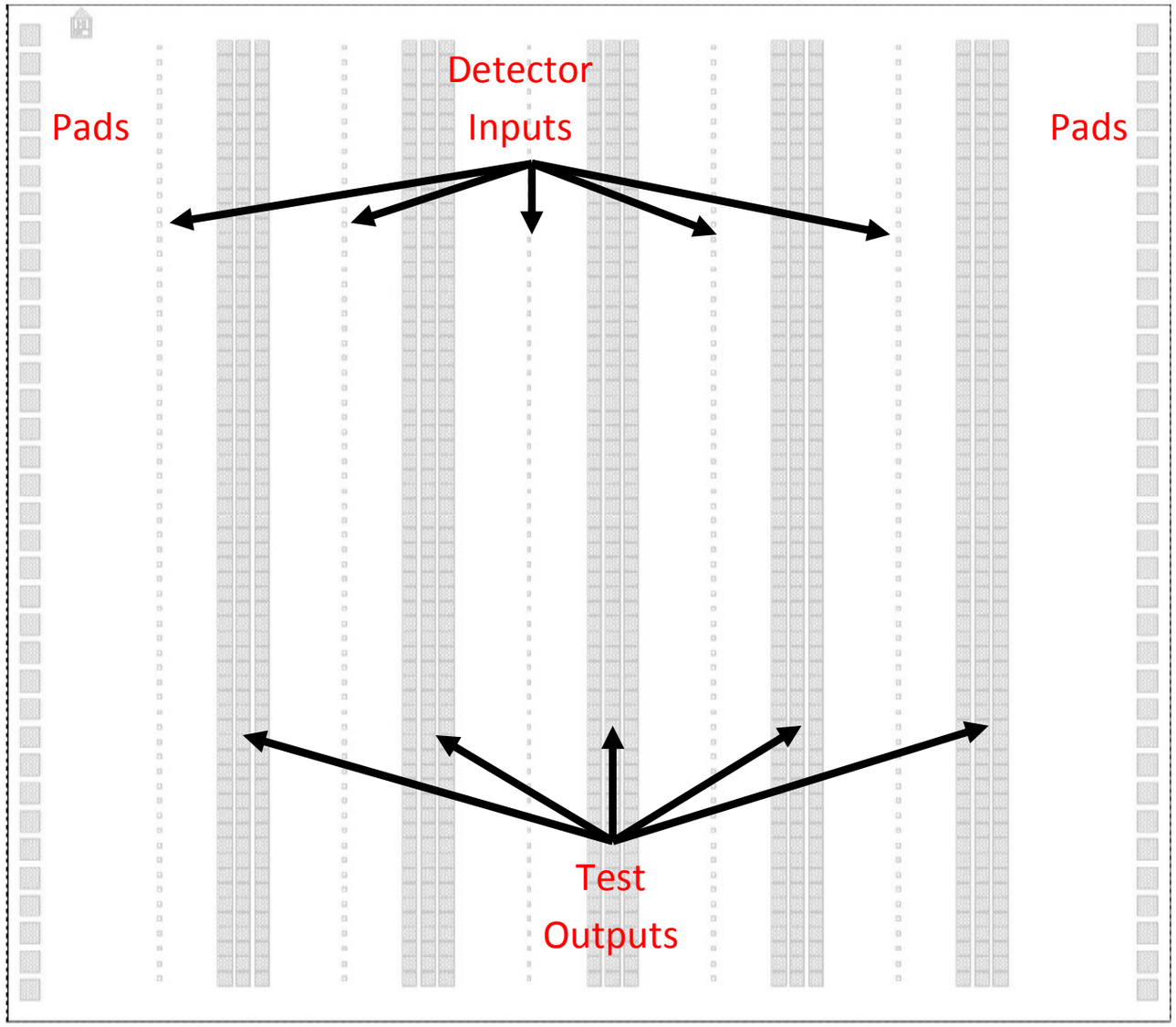




ASD characteristics

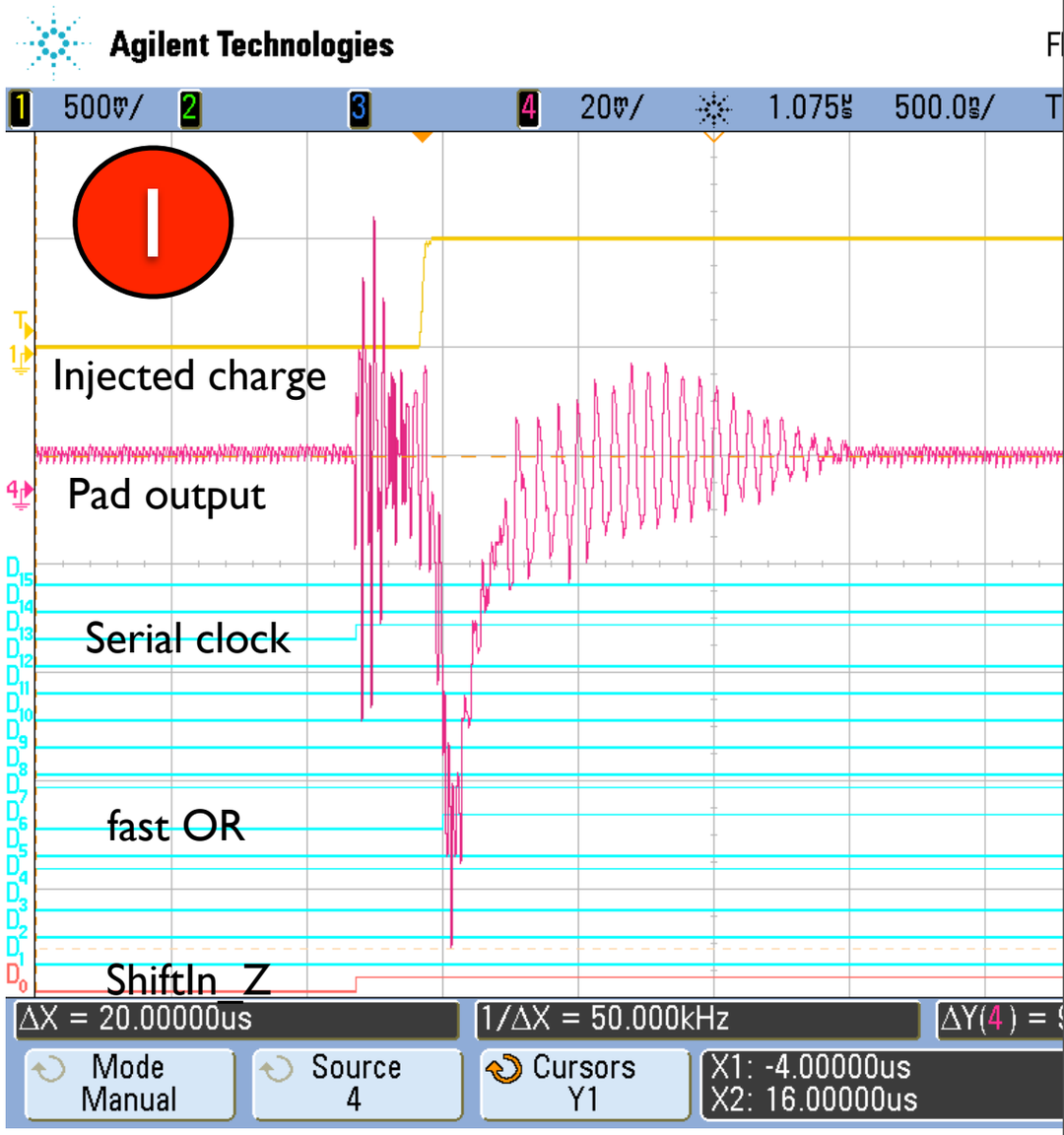
- On top surface of 3D chips:
- Sensor inputs
- 3 debug pads:
  - Preamplifier output
  - Amplifier output
  - Discriminator output

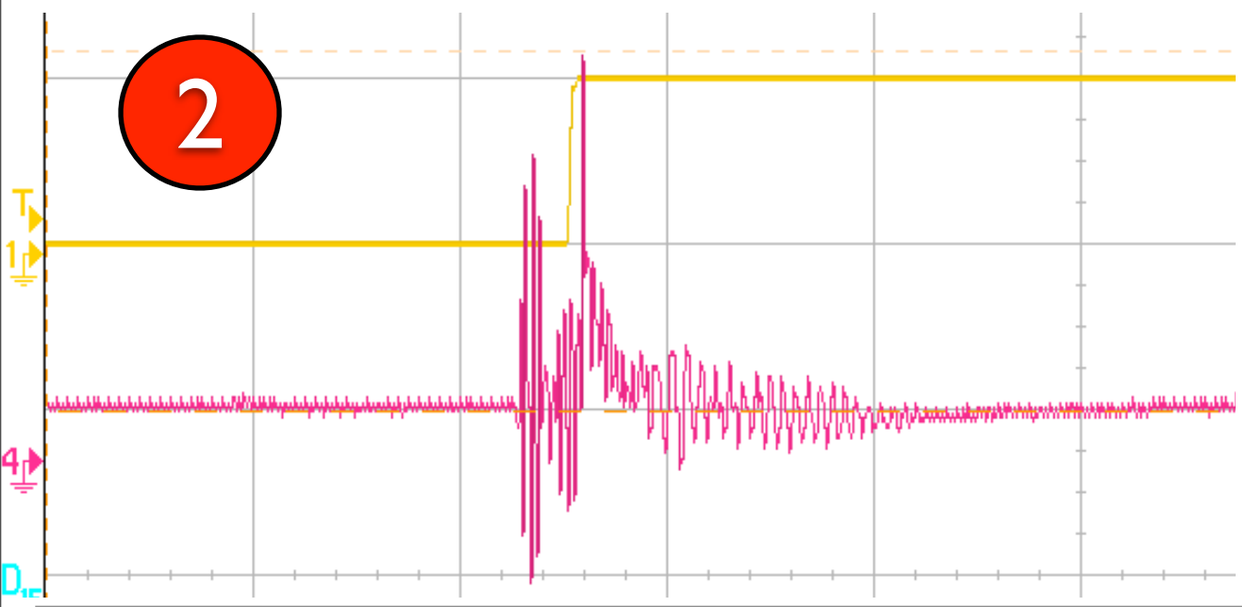
- Use probe station and picoprobe to access these

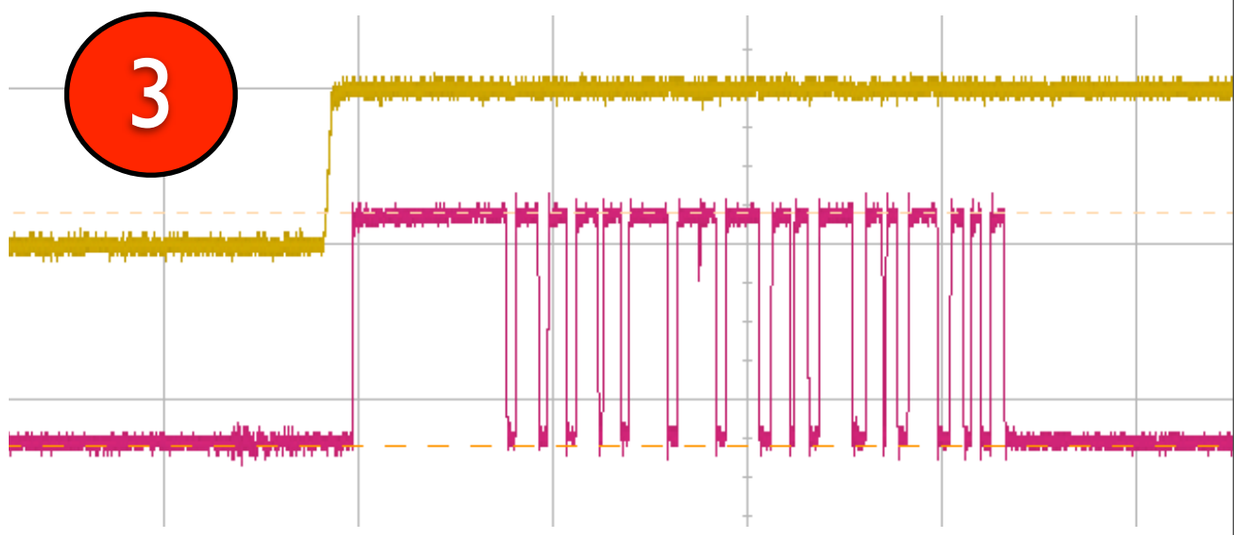


ASD characteristics

1. Preamplifier output
   - Pickup from serial clock or ShiftIn_Z (?)
   - Ringing
2. Amplifier output
   - Very small/no signal. Layout problem?
3. Discriminator output
   - See effect of ringing
   - At high input voltages, 2nd delayed turn-on (not shown)







Future plans

- Short-term plan:
  - Understand ASD characteristics/issues
  - Connect capacitors in place of sensors and characterize
    - Get more realistic measurements with this (turn on curves, time walk)
    - We have made some progress already
  - Measure capacitance of charge injection capacitors to know how much charge is being injected for a given voltage

backup

Crosstalk problem

- One possible explanation for what we see is due to the geometry of the chip
- In each strip set, the 5 discriminator output lines run the same distance to achieve the same capacitance
- This means the Z<0> line runs past each of the sensor pads, about 10 microns away
- Like a capacitor, it may introduce some extra charge in the subsequent front ends causing their thresholds to lower