VICTR II Update

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Status

- Verilog model for the test chip is complete
  - 16 bit input register
  - full data transfer in phi direction
  - No Z transfer (tested with phi transfer)
  - Complete output transfer with asynchronous pipeline
  - chip can serve as both generator and receiver so we can build a complete colum readout

Status II

- Program has been written to generate random input patterns (no physics) and compute the chip results
- Verilog model reads in a file of these patterns and compares the chip calculations to the file
- Straightforward to change this to physics siulations

Hardware Design

- G. Magazzu at Santa Barbara has started on chip layout.
  - Generated VHDL model of some of the circuits and compiled them with Cadence
- Jim Hoff will start around March 1 on other aspects of the design

Plans

- About 3 Months of detailed engineering required for the test chip
- Hope for a chip submission in late summer