

Oxford Technical Report

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Outline

- **Main beam fast feedback**
- **Drive beam phase feed-forward**
- **Laserwire – covered by P. Karataev**

Main beam fast feedback

Collaboration with MDI team

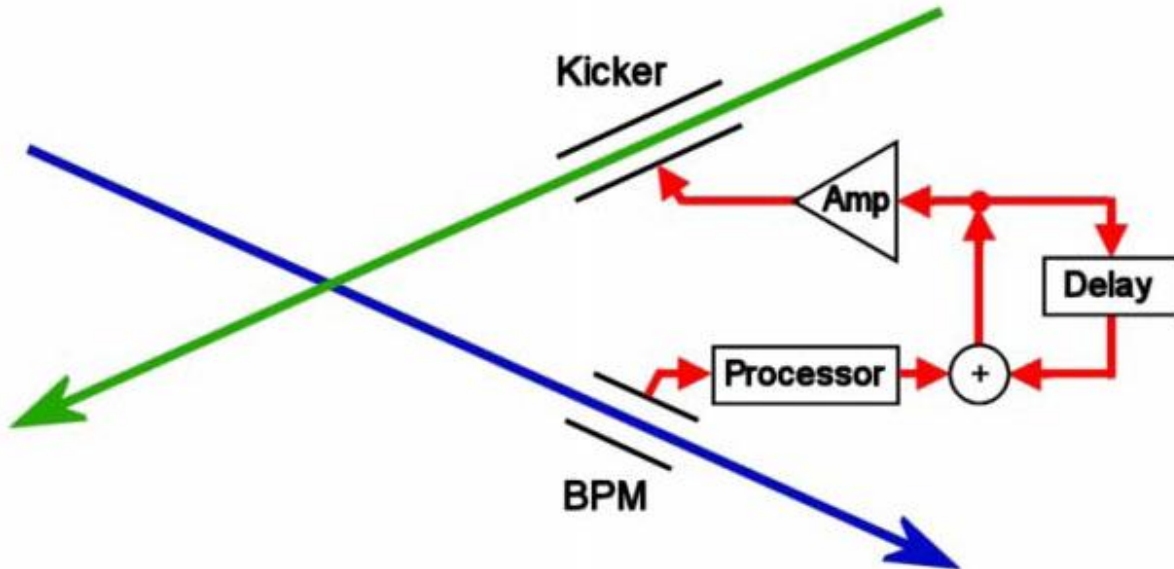
Coordinated by D. Schulte and L. Gatignon

CLIC intra-train IP FB system concept

Last line of defence
against relative
beam misalignment

Measure vertical
position of outgoing
beam and hence
beam-beam kick
angle

Use fast amplifier and
kicker to correct
vertical position of
beam incoming to IR



FONT – Feedback On Nanosecond Timescales

Main Beam IP FB Design Status

Conceptual design developed and documented in CLIC CDR

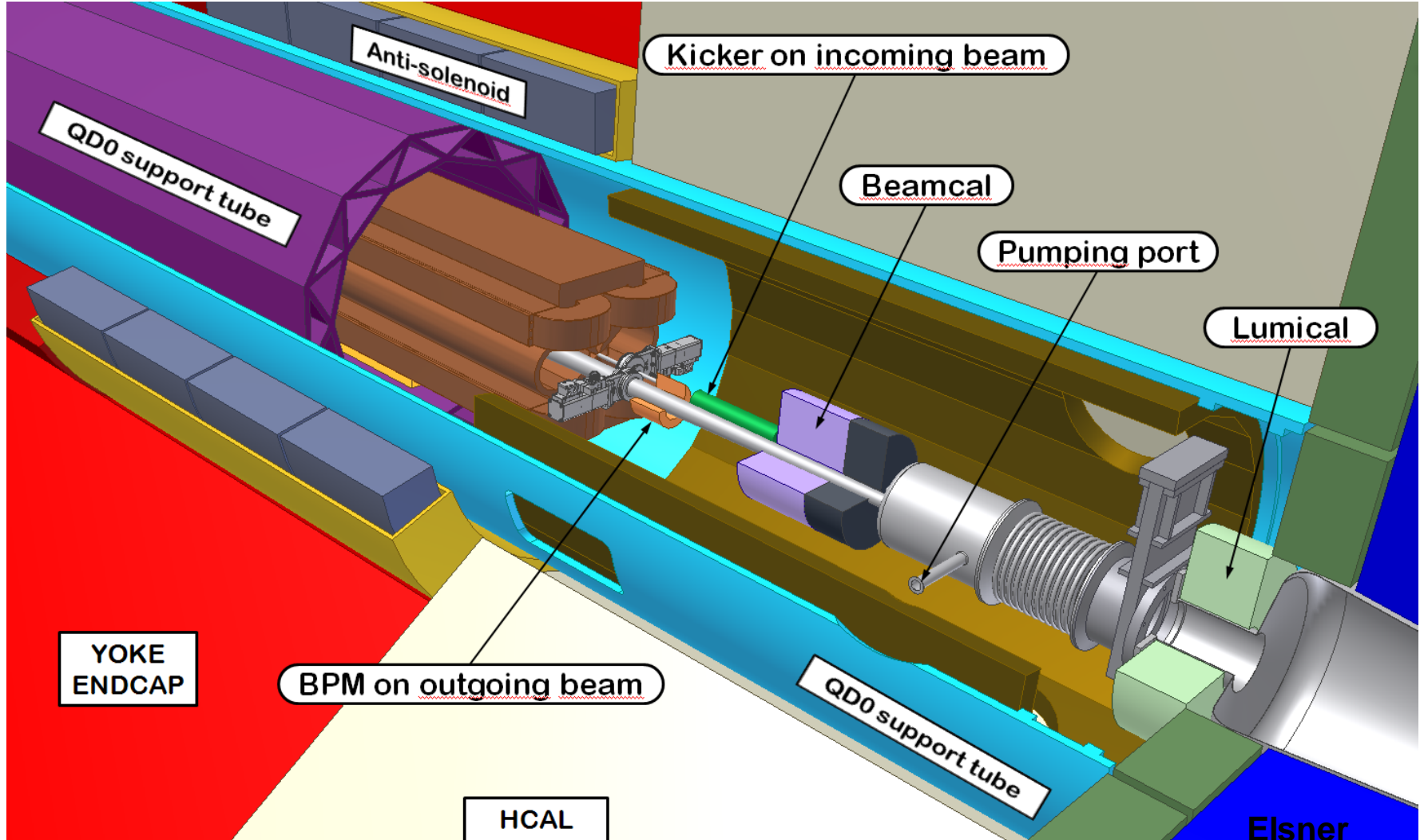
NB primary method for control of beam collision overlap is via vibration isolation of the FF magnets, and dynamic correction of residual component motions

IP position feedback:

**allows IP beam position correction of ± 50 nm of vertical beam motion,
and possibility to correct within bunchtrain duration**

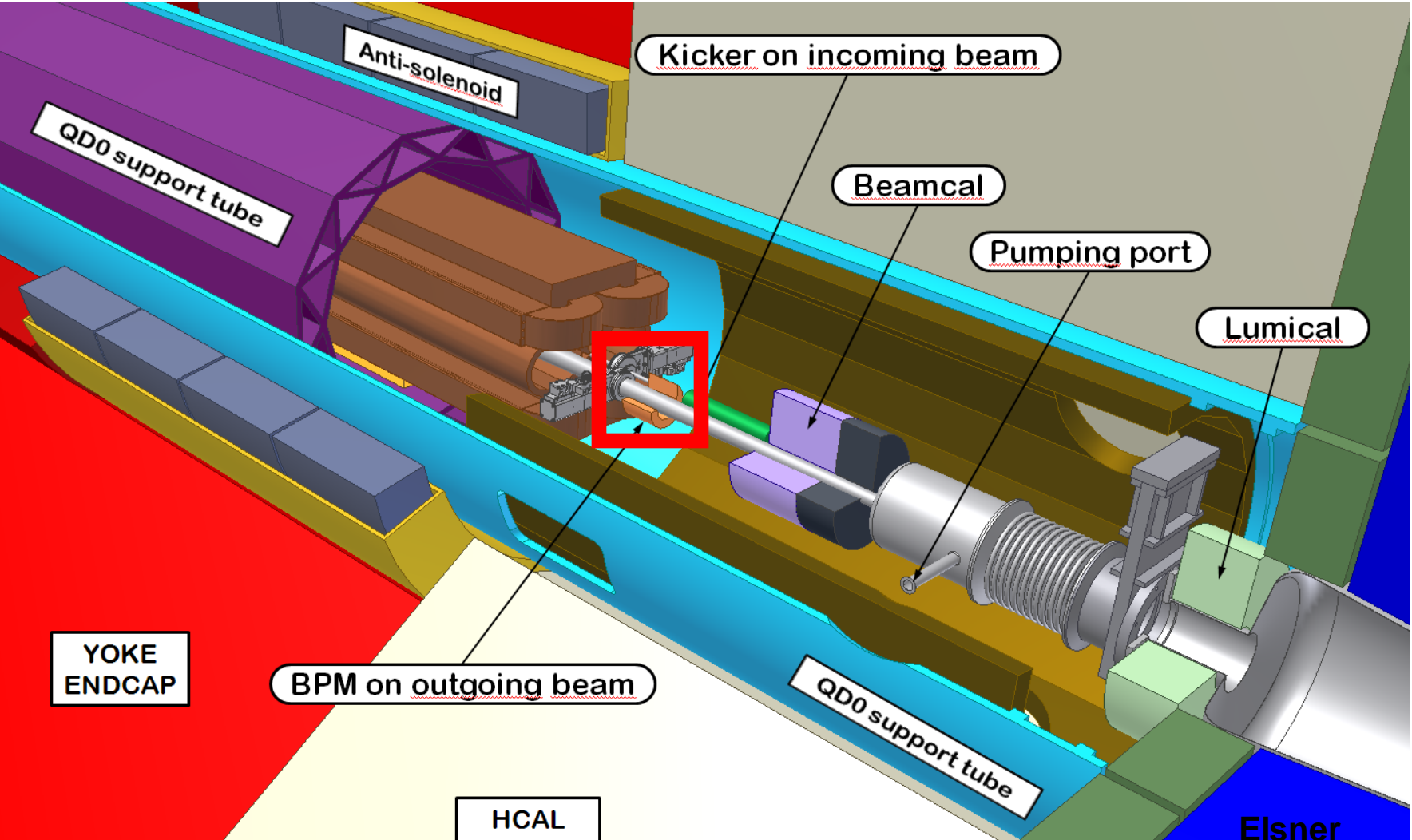
More realistic engineering design can be developed in next project phase

CLIC Final Doublet region



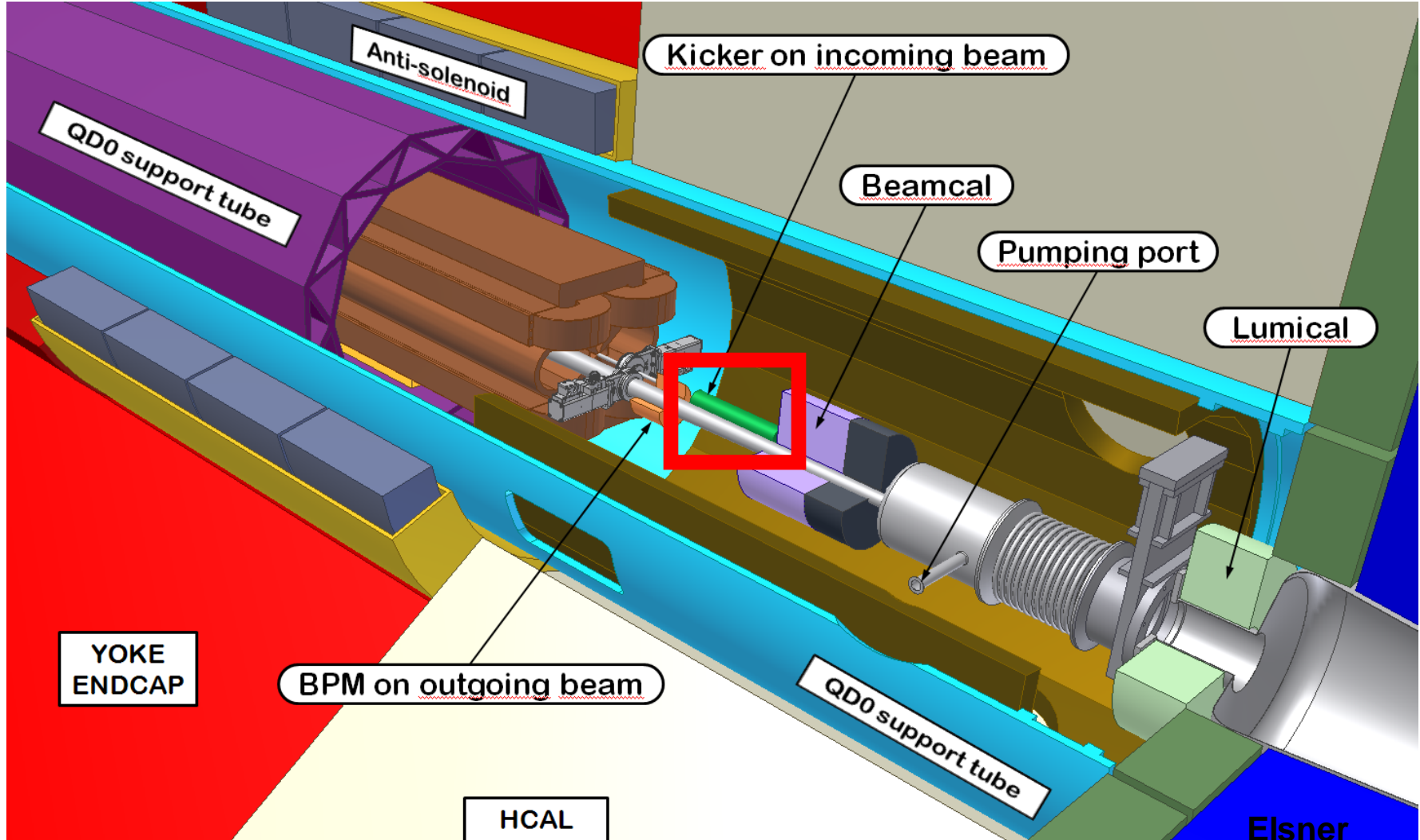
Elsner

CLIC Final Doublet region



Elsner

CLIC Final Doublet region



Elsner

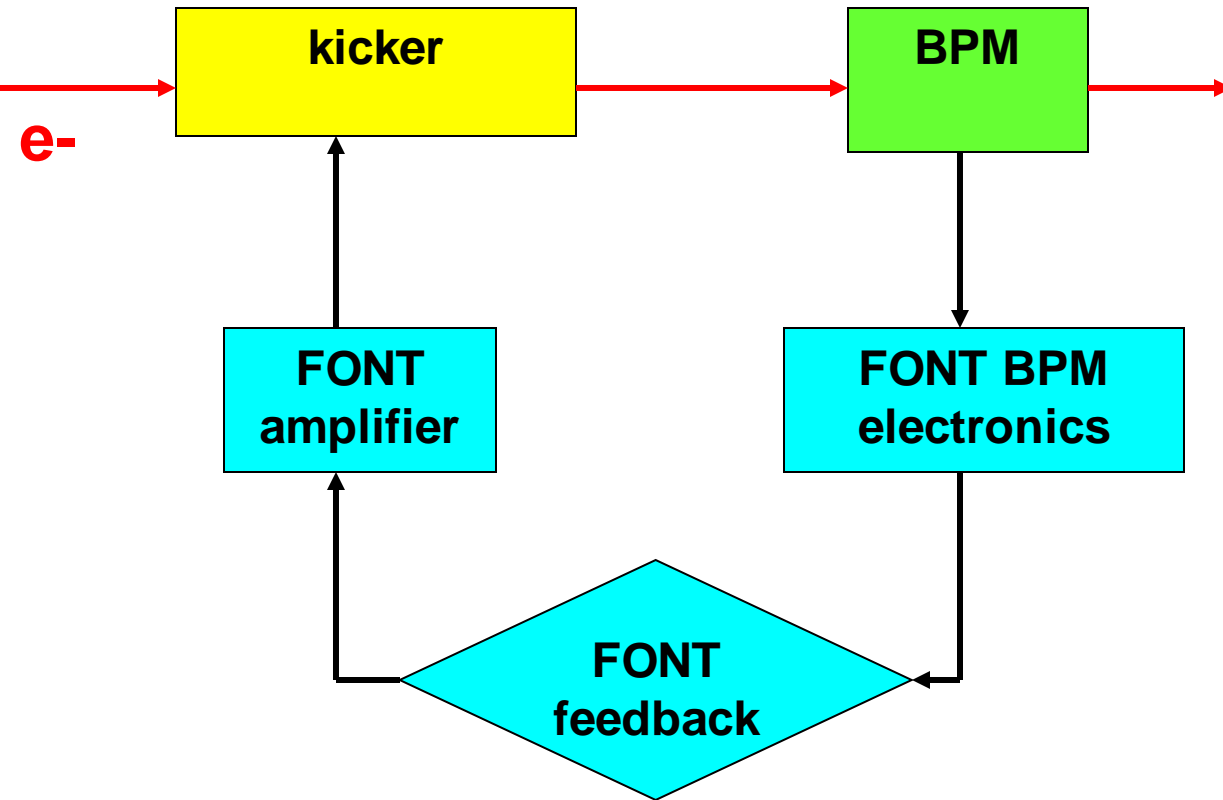
IP FB engineering issues

- **Engineering of real hardware optimised for tight spatial environment: BPM, kicker, cables ...**
- **Large (and spatially-varying) B-field → operation of ferrite components in kicker amplifier?!**
- **Further studies of radiation environment for FB system: was studied for ILC, so far preliminary for CLIC; where to put electronics? need to be rad hard? shielded?**
- **EM interference: beam ↔ FB electronics
kicker ↔ detector**

Main beam fast feedback

Prototype tests at ATF/ATF2

IP FB loop



FONT3 CLIC prototype at KEK/ATF

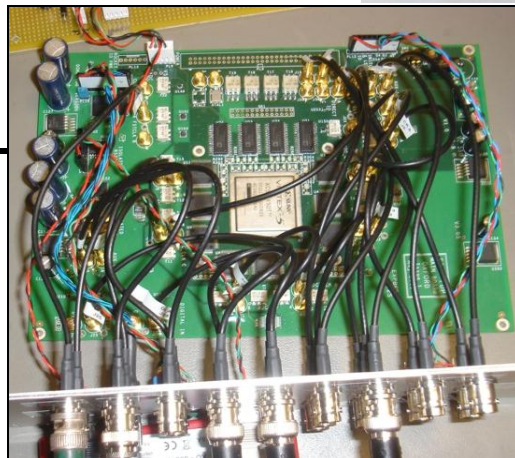
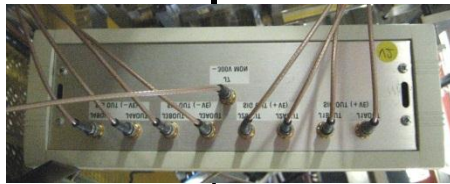
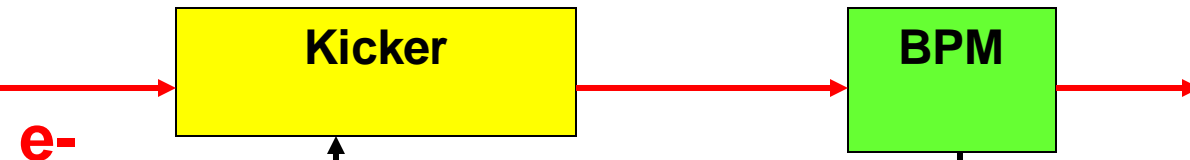
56ns train of bunches separated by 2.8ns



**FB loop closed with
electronics latency 13ns**

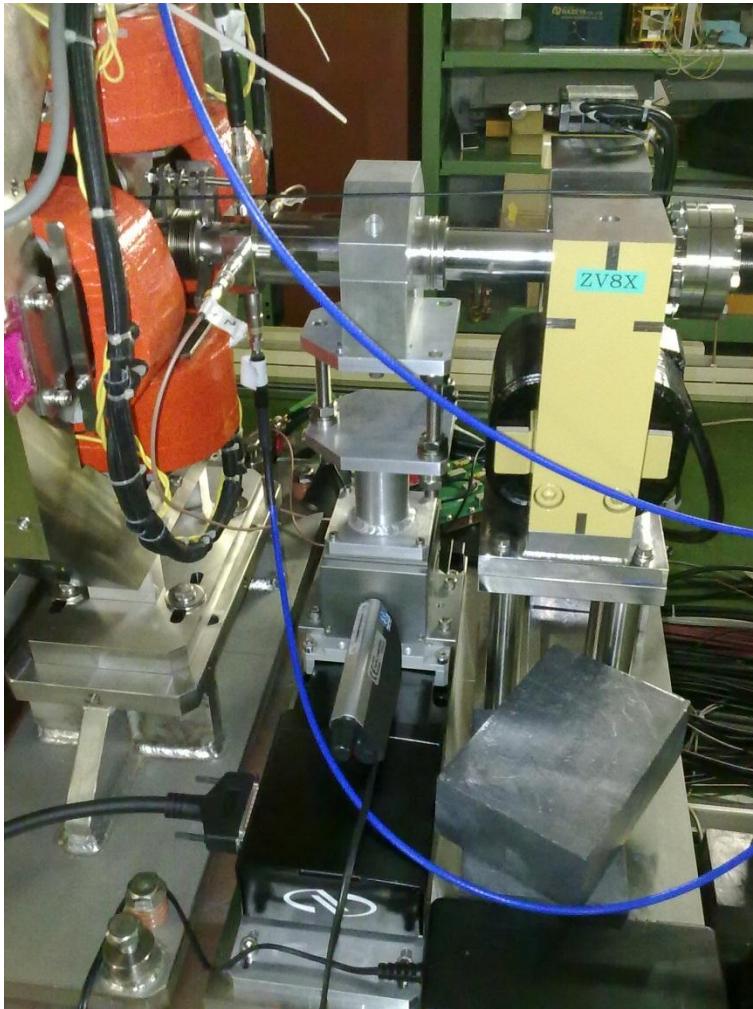
FONT5 at KEK/ATF2

300ns train of bunches separated by 150ns



BPM resolution ~ 1 μ m
Drive power > +-50nm @ CLIC

FONT5 beamline hardware

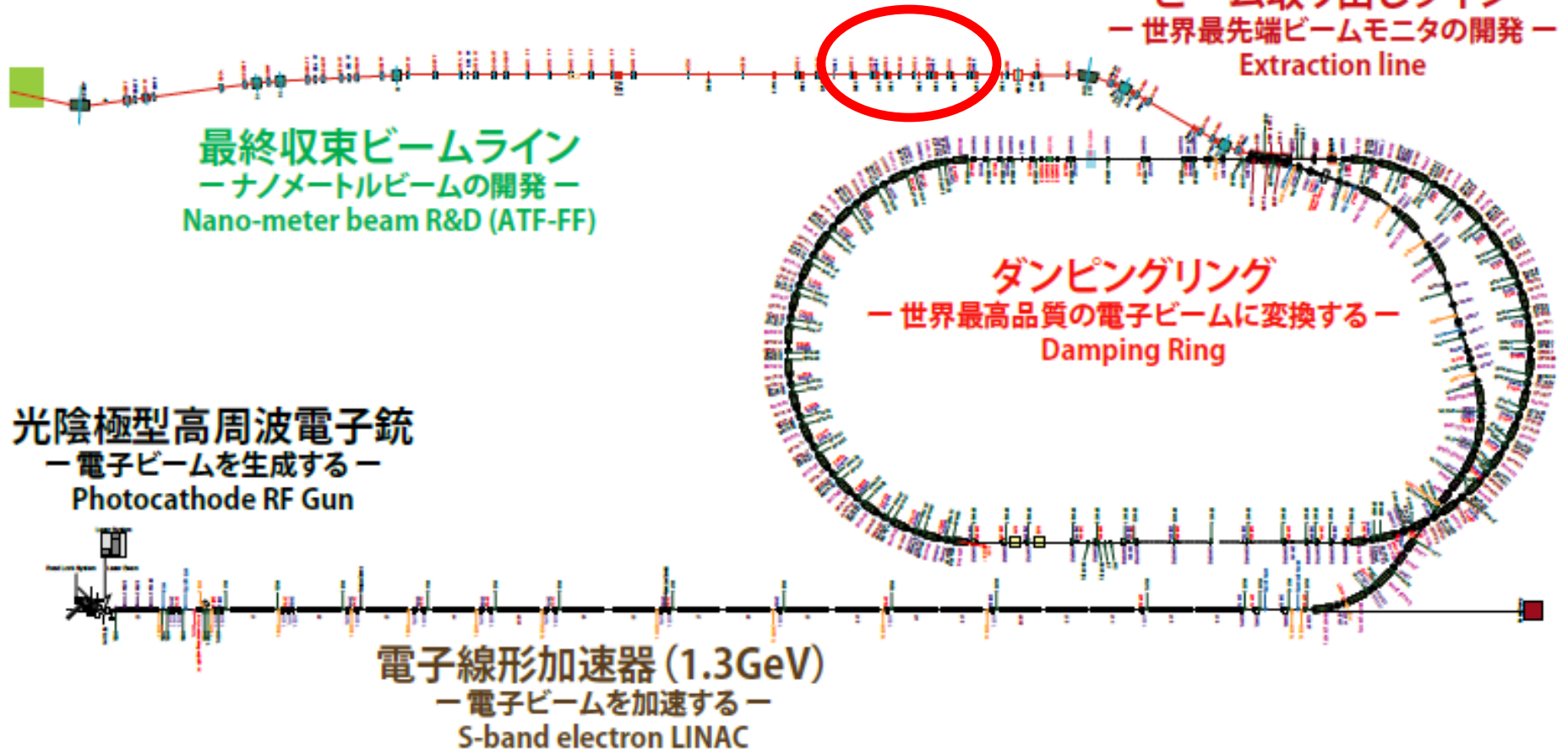


**3 BPMs and 2 kickers installed in
new ATF2 extraction line
February 2009;
BPM movers installed 2010**

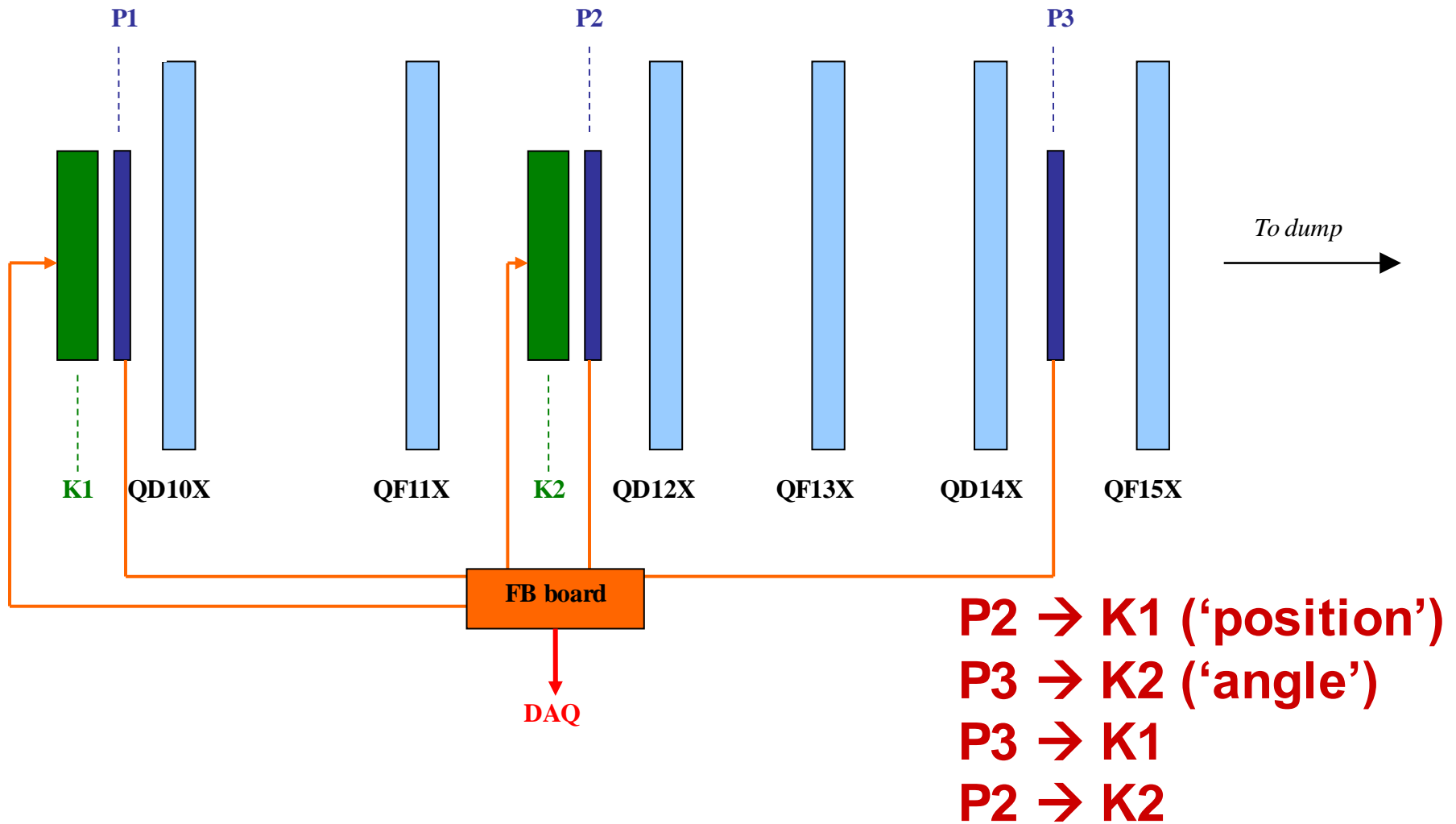


FONT5 location

ATF2 extraction line



FONT5 setup



R&D main aims

- **Demonstration of components + system suitable for CLIC (and ILC) IP FB, tested with real beam:**
stripline kicker, stripline BPM, analogue signal processor, fast RF amplifier, FB board
- **ATF2 goal 1: produce 37nm beam spot at IP**
micron-level stabilisation of beam at entrance to ATF2 final focus
- **ATF2 goal 2:**
nanometer-level stabilisation of beam at ATF2 IP using an IP FB

Ongoing R&D

- **Understanding/improving FB performance:**

Improving BPM resolution

Robert Apsimon PhD thesis

further DR extraction kicker timing studies

monitoring downstream BPMs + jitter tracking

Douglas Bett PhD thesis

- **Design of an ATF2 IP feedback system:**

Michael Davis PhD thesis

ATF2 programme 2011-12

- **June: check + repair hardware post-quake**
- **Nov/Dec: 2 dedicated shifts in each of 3 weeks**
- **March/April: 2 shifts in each of 2 weeks**
 - 1) setup, commissioning, BPM resolution, DR extraction kicker timing studies w. 2 bunches**
 - 2) re-establish FB, loop/gain studies**
 - 3) FB optimisation, downstream beam orbit tracking**

BPM processor resolution tests

- 3 BPM processors (5,7,10) on BPM P2

25/10/11 8-hour shift:

0.55 0.56 0.60 μm

0.56 0.54 0.51 μm

0.53 0.40 0.35 μm

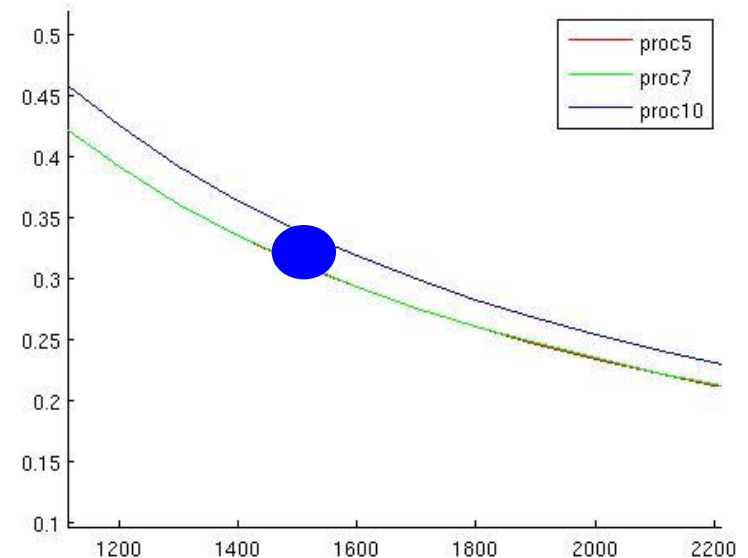
0.50 0.35 0.33 μm

0.45 0.44 0.35 μm

0.50 0.43 0.36 μm

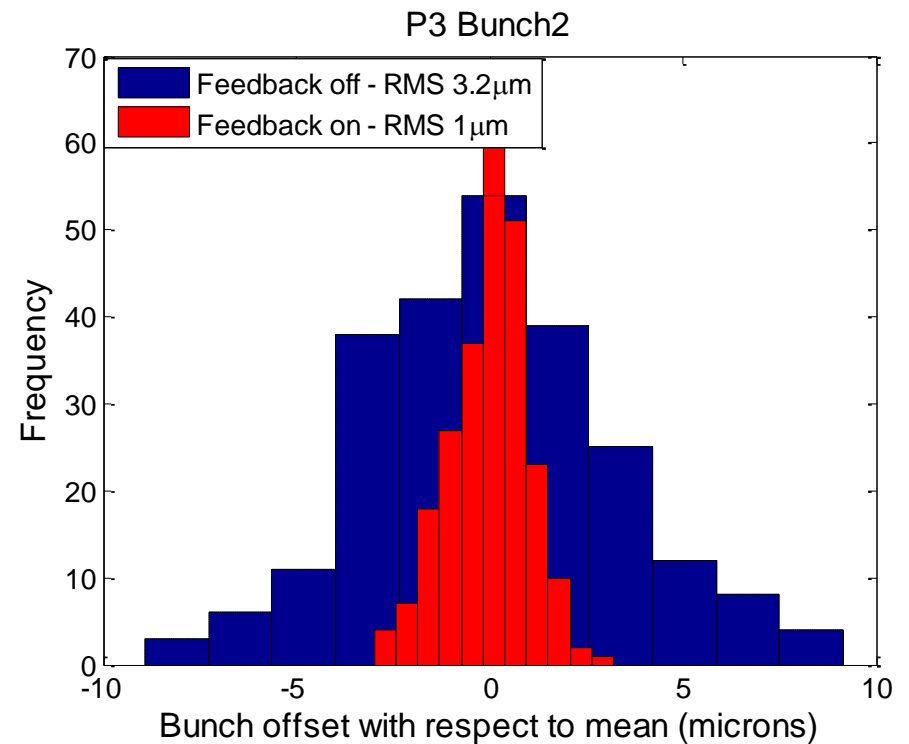
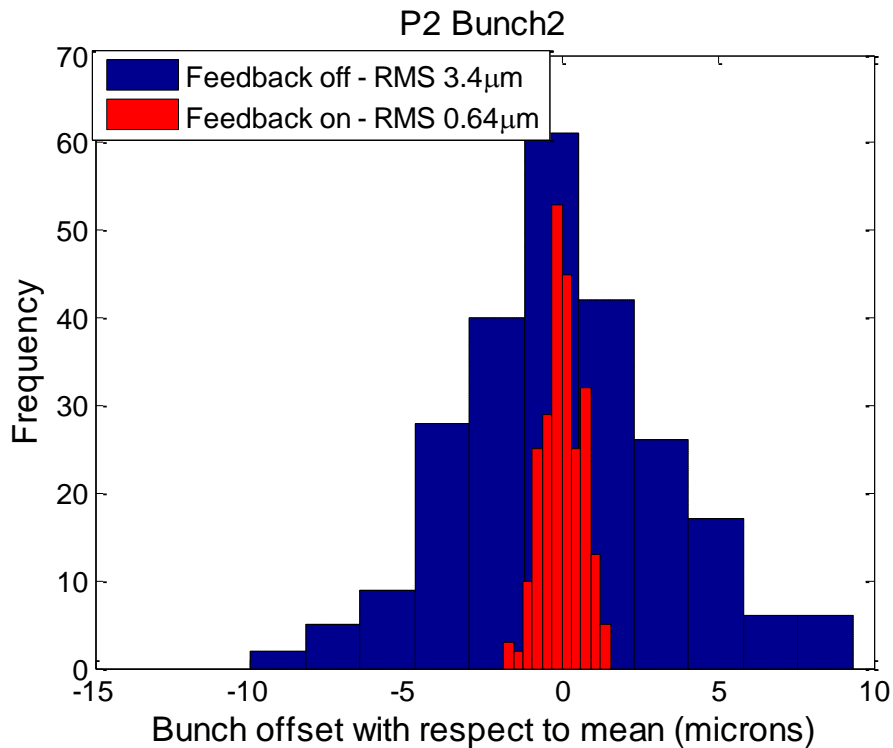
Beam position jitter 3- 4 μm

expectation from
ADC noise alone:



Feedback Performance

(example FB Run 6 13/12)



Feedback Performance

(example FB Run 6 13/12)

bunch

1

2

FB off

on

FB off

on

Jitter P2

3.42

3.39

3.42

0.64

P3

3.24

3.16

3.21

1.04

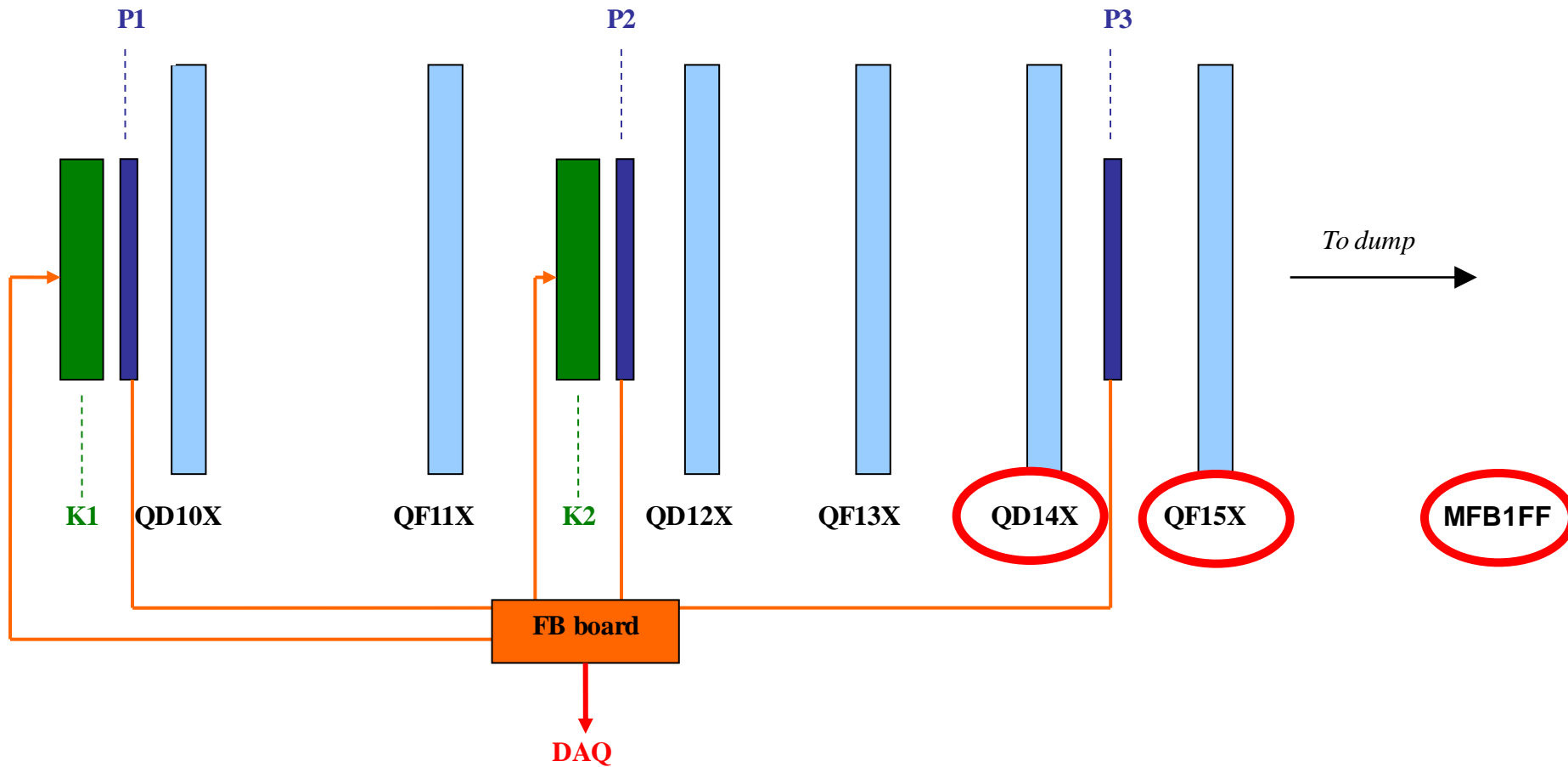
Feedback Performance

(example FB Run 6 13/12)

bunch	1		2		Pred.
	FB off	on	FB off	on	
Jitter P2	3.42	3.39	3.42	0.64	
1-2 correl	98%				0.67
P3	3.24	3.16	3.21	1.04	
1-2 correl	97%				0.83

$$\sigma_r^2 = \sigma_1^2 + \sigma_2^2 - 2\sigma_1\sigma_2\rho_{12} \geq 2\sigma_r^2$$

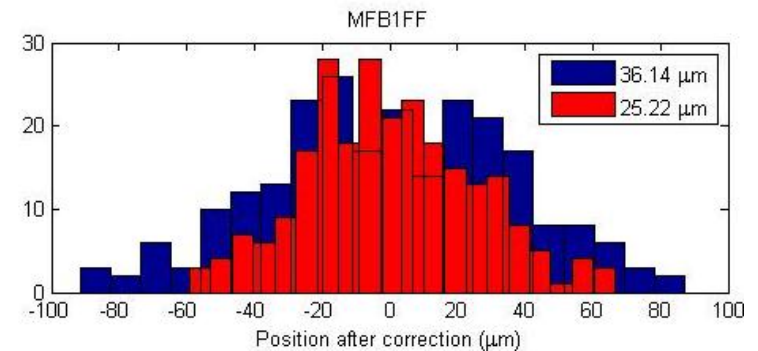
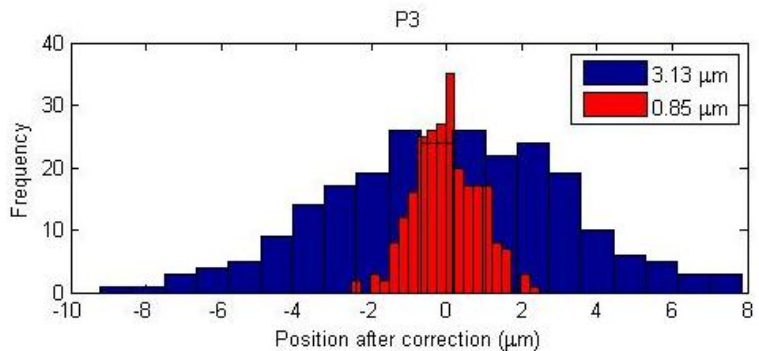
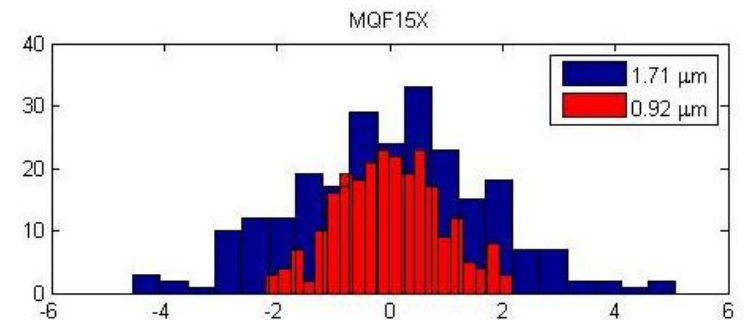
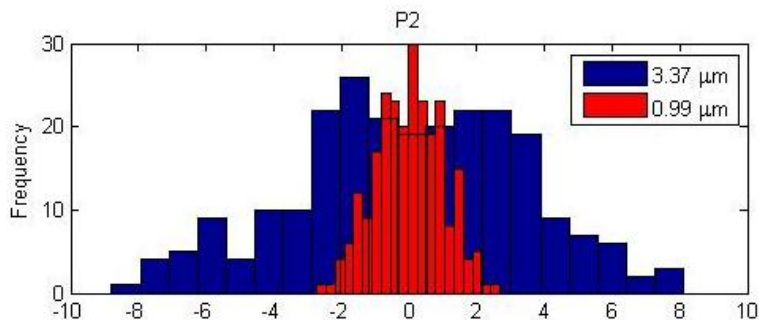
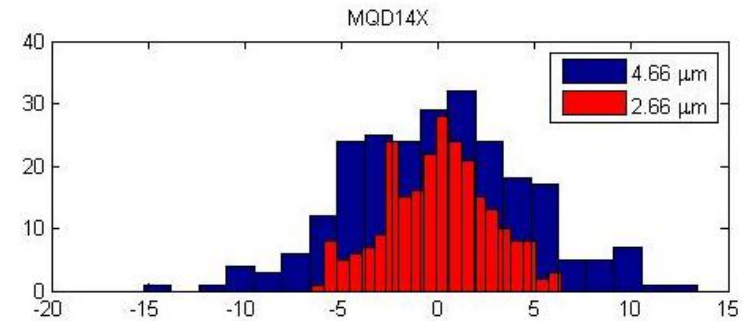
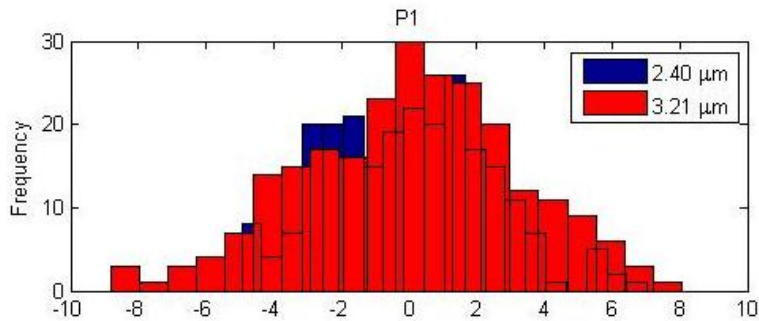
FONT5 setup Winter 2011-12



BPM resolutions (um)

P1	P2	P3	MQD14X	MQF15X	MFB1FF
0.59	0.44	0.44	0.51	0.49	0.98

FB performance, downstream ...



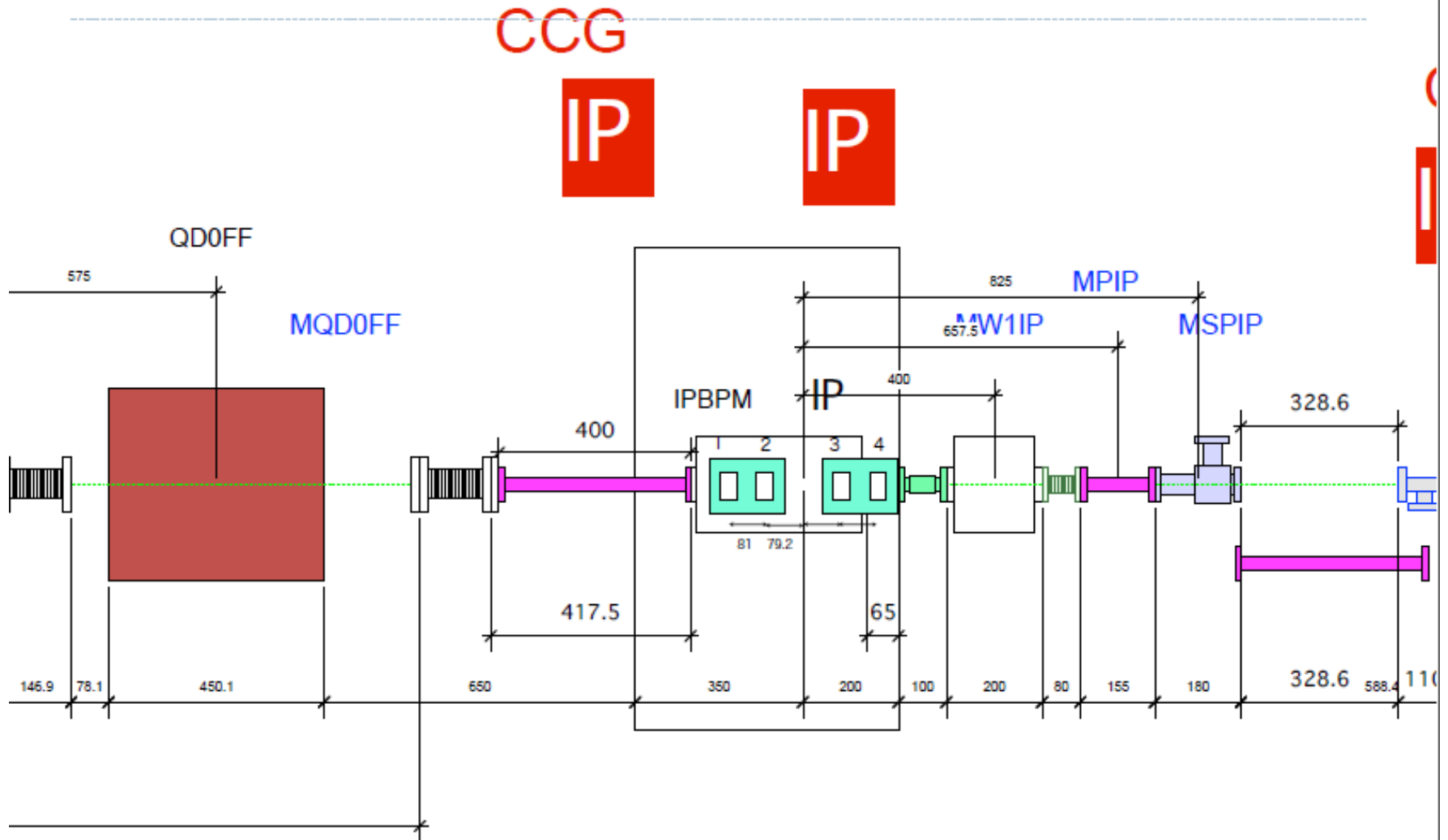
Main beam fast feedback

ATF2 IP FB design

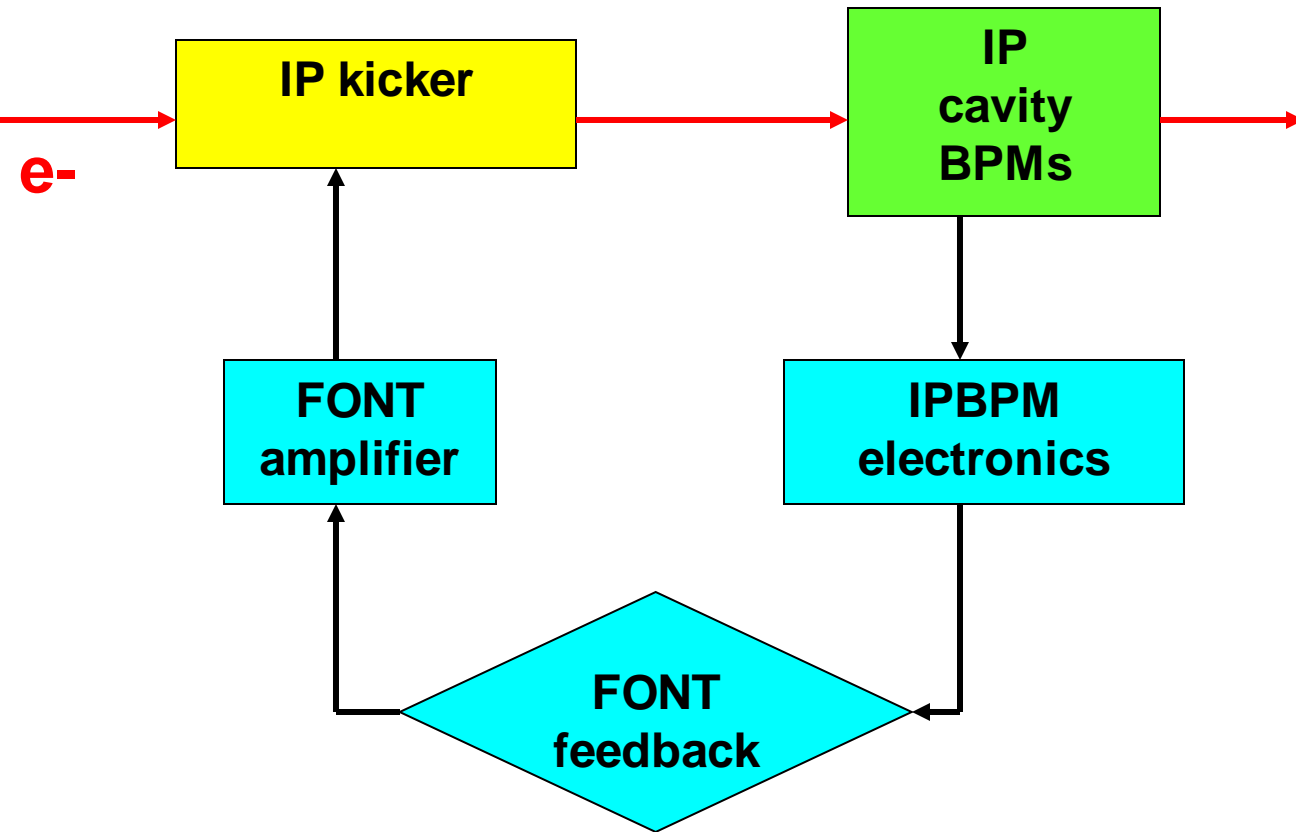
JAI Oxford

**in collaboration with JAI RHUL,
LAL, KEK and KNU**

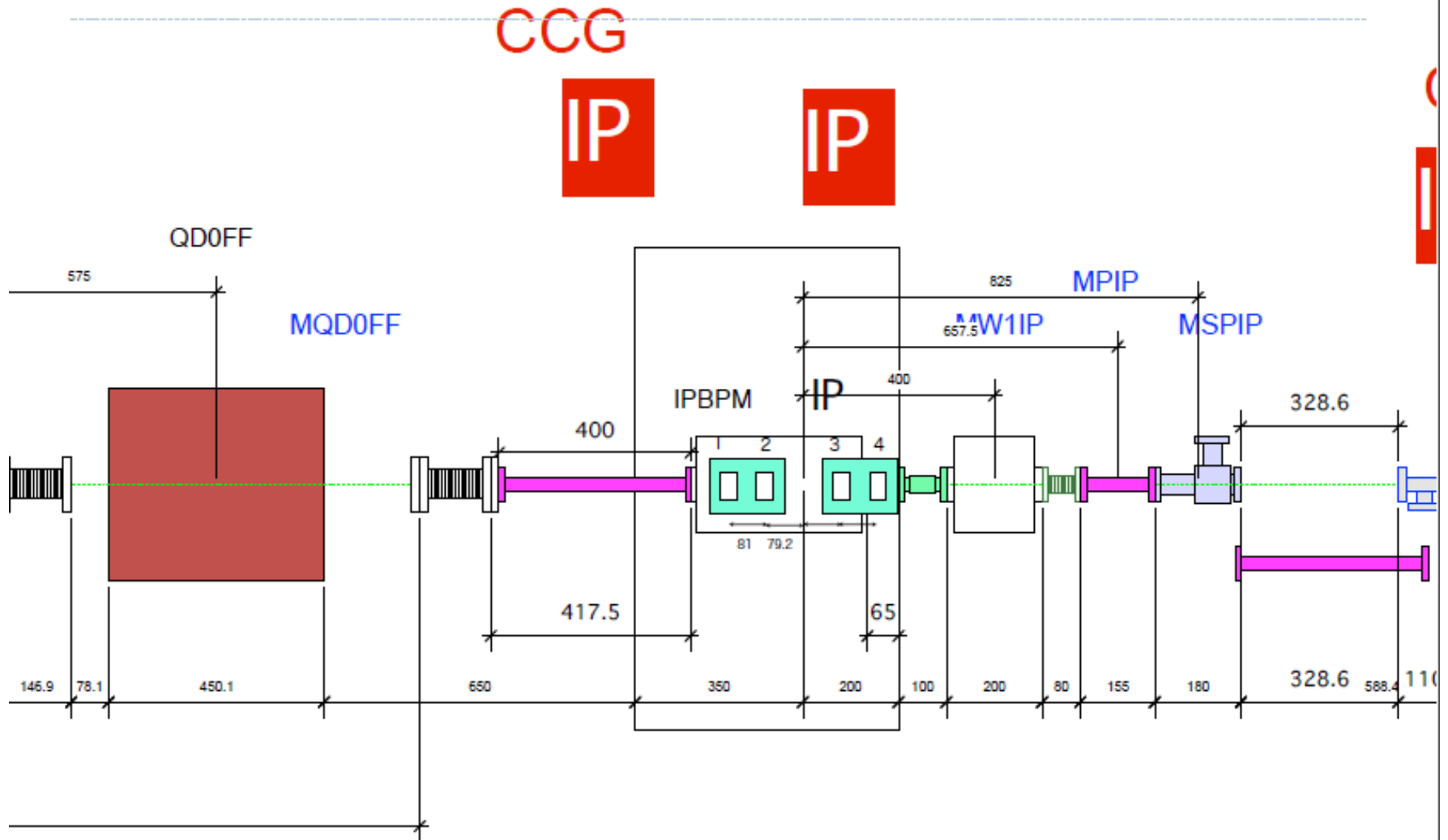
Eventual ATF2 IP configuration



IP FB loop

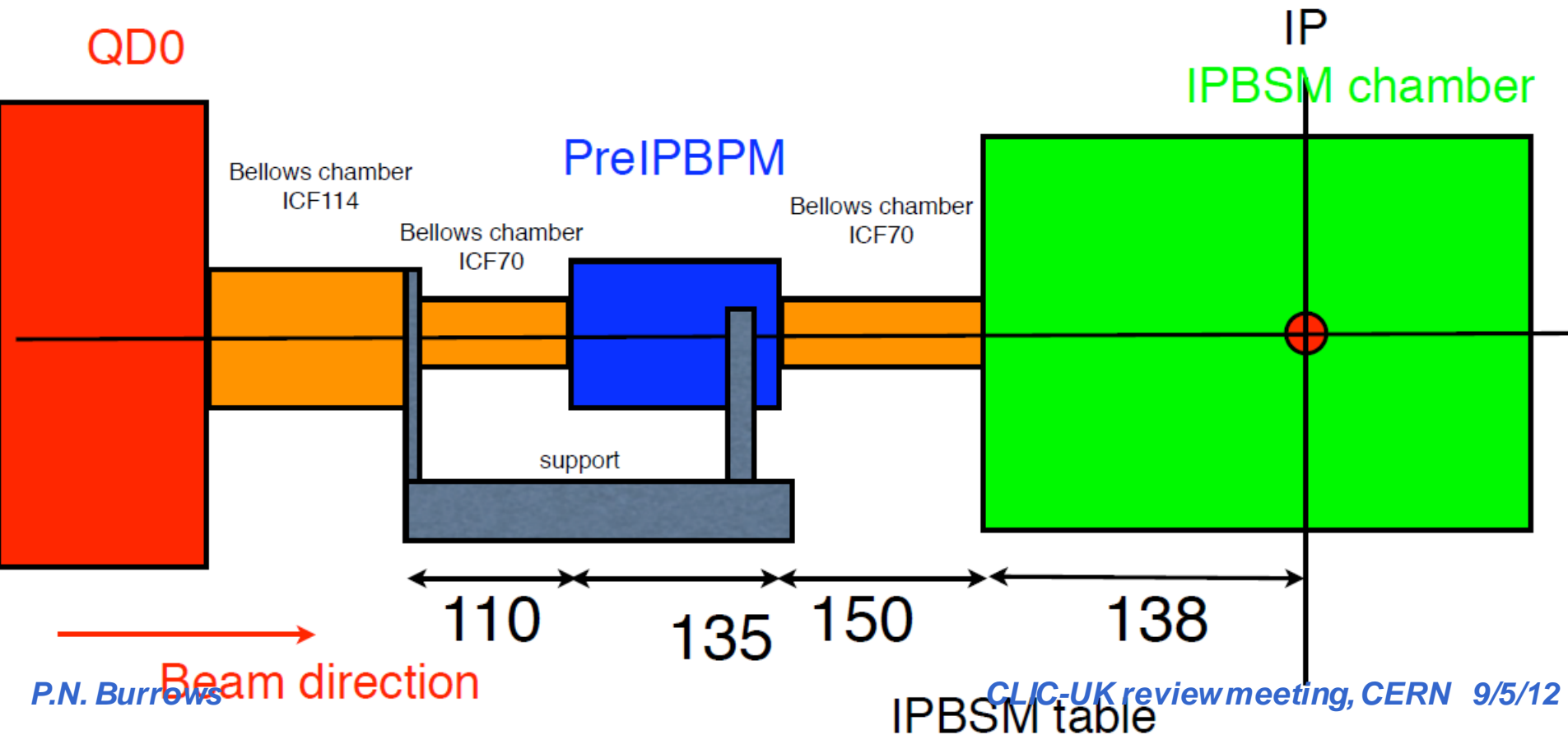


Eventual ATF2 IP configuration

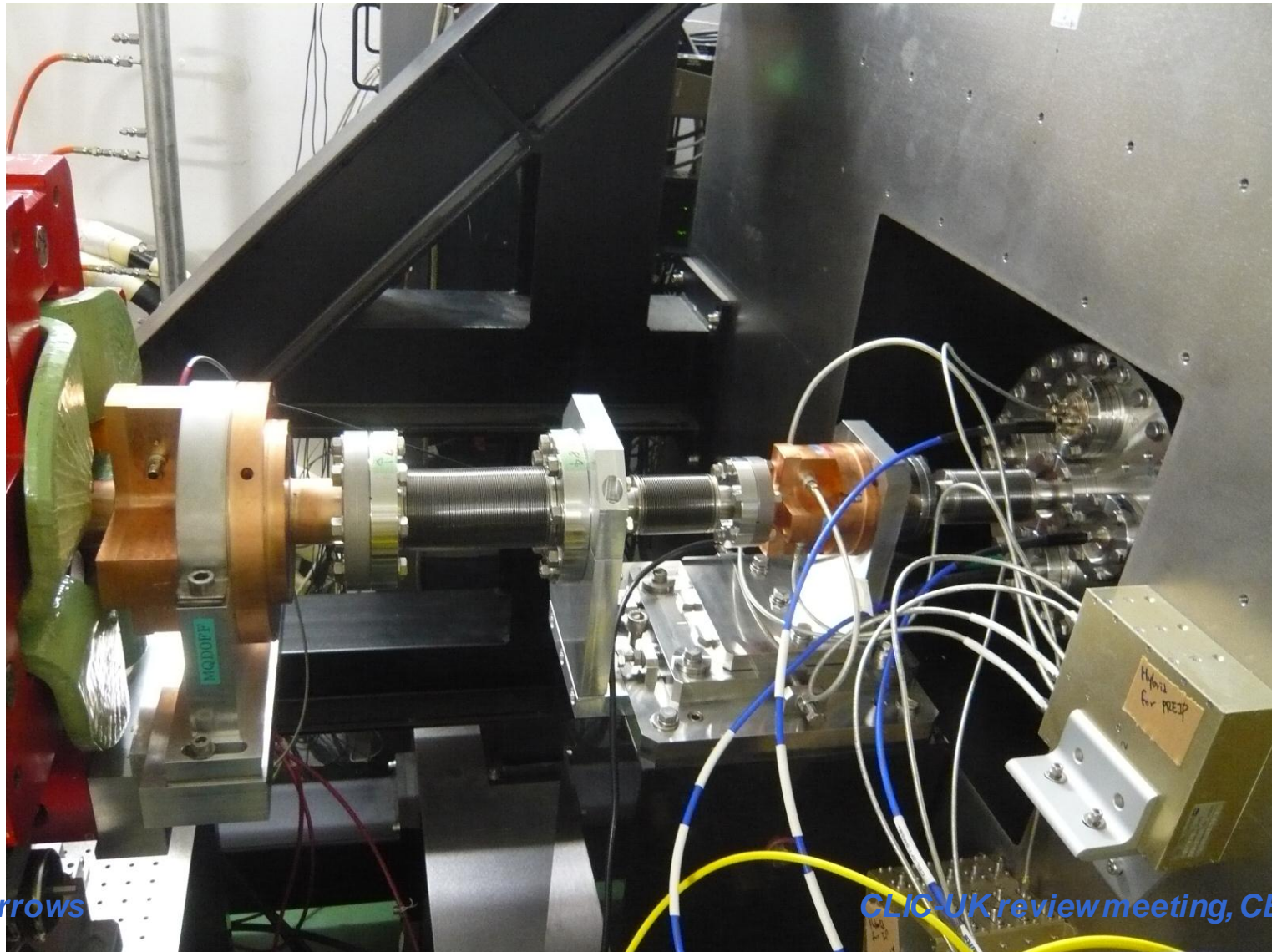


Current ATF2 IP configuration

- PreIPBPM is connected with ICF70 bellows at both ends for position adjustment.
- QDO is with ICF114 bellows for its position adjustment. (Since it needs to balance vacuum force for both ends, this should be ICF114 size.)
- ICF70-114 bellows joint is supported from PreIPBPM table.



Current actual layout



New kicker



Summary: ATF2 IPFB

- **Conceptual IPFB design established**
- **New kicker has been fabricated**
- **Use FONT amplifier to drive kicker**
- **Use FONT5 FB board for digitisation + signal processing**
- **Measurements indicate good beam quality for 2-bunch mode with up to 300ns bunch spacing**
- **Install kicker May, observe beam kick June**

Drive beam phase feed-forward

JAI Oxford

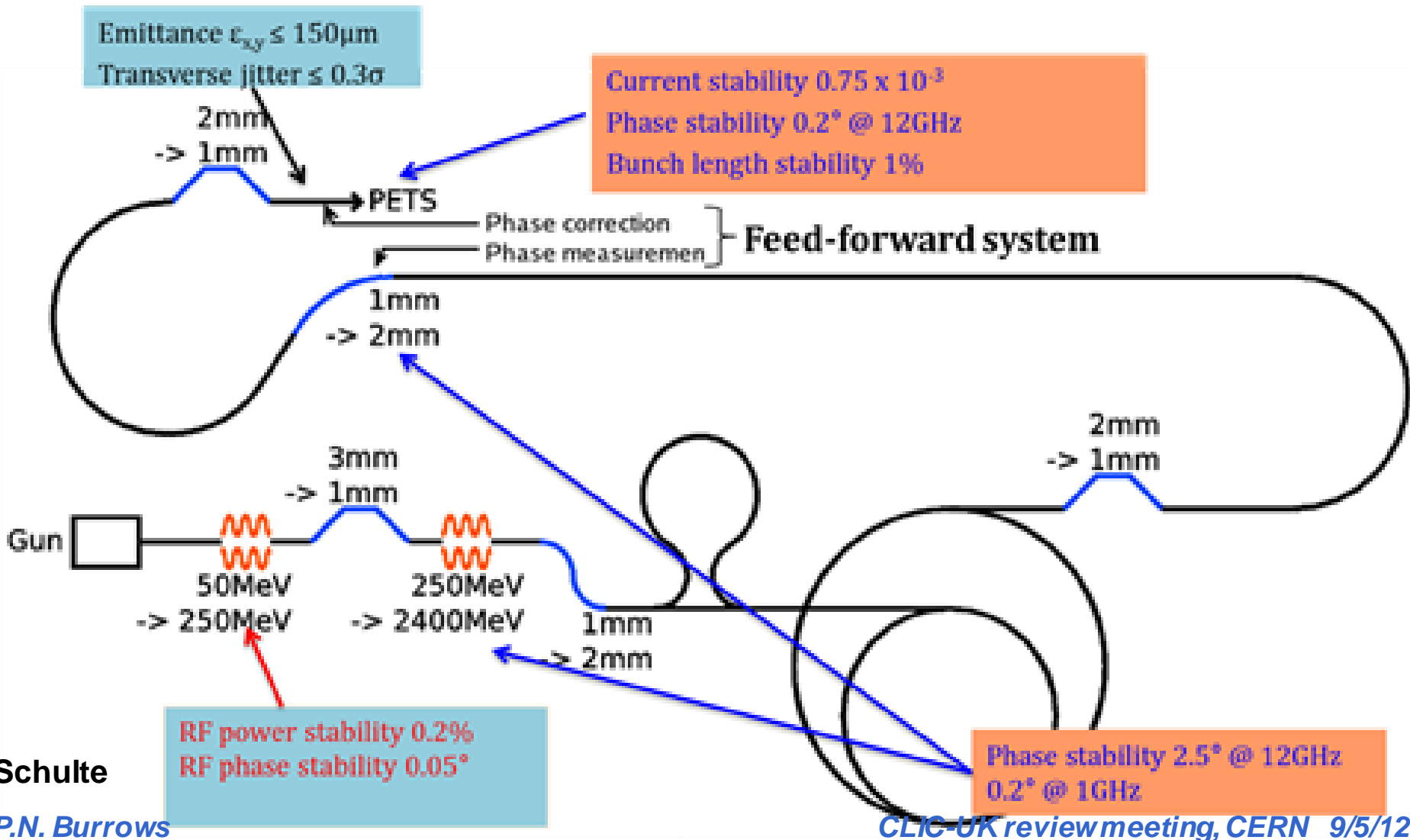
**in collaboration with CERN +
INFN-Frascati**

Coordinated by P. Skowronski

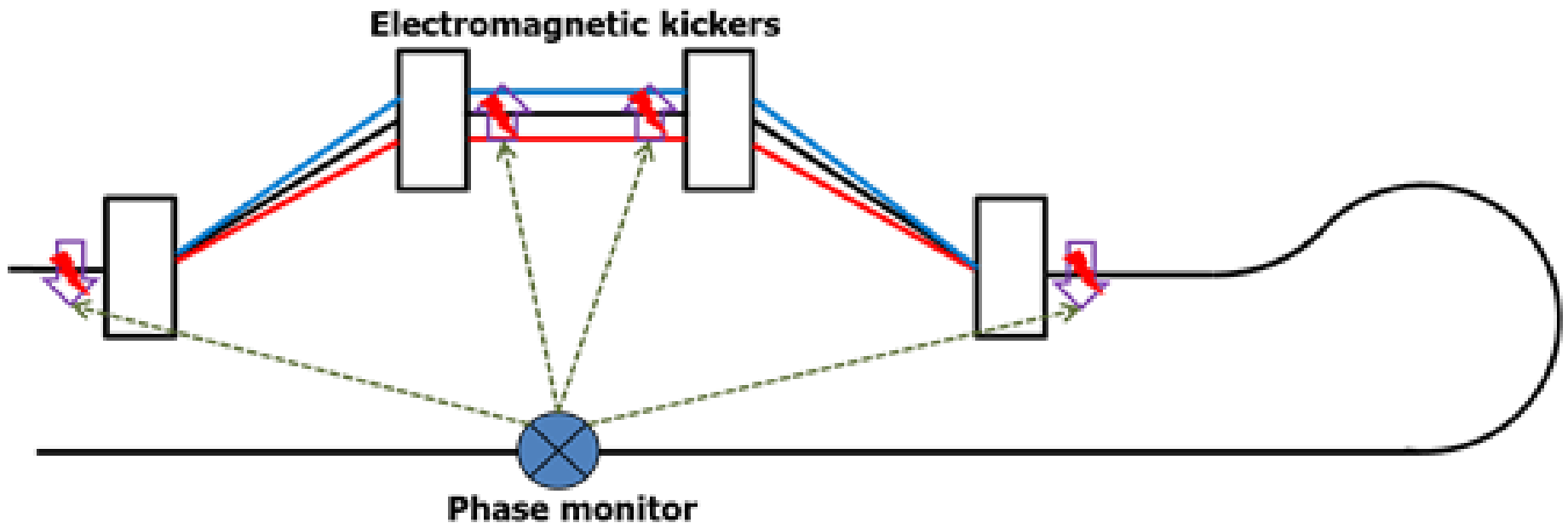
Drive beam phase feed-forward

Phase feed-forward design in CDR

Drive beam phase feed-forward

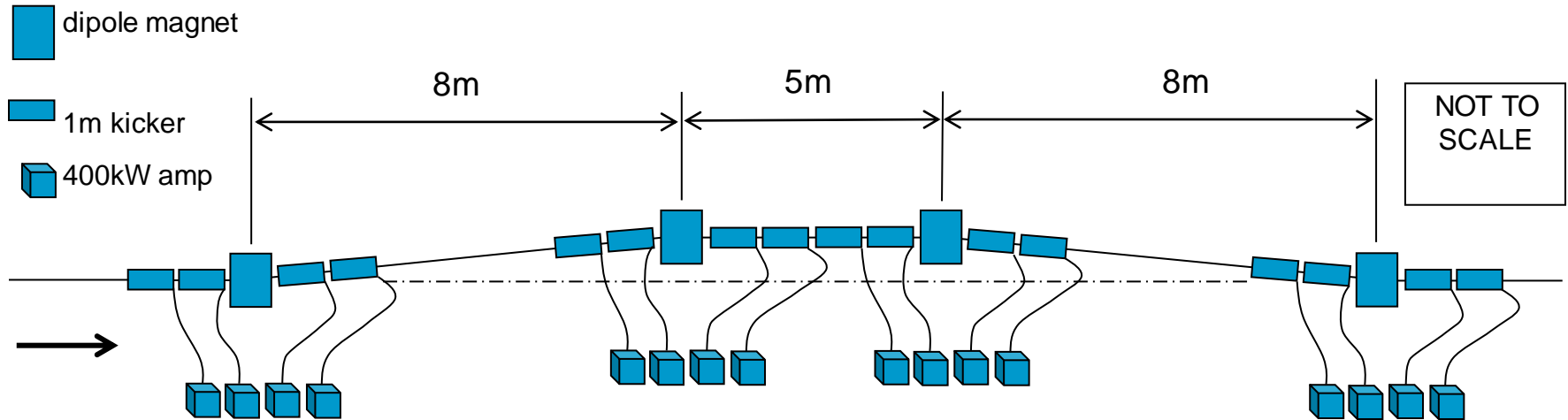


Drive beam phase feed-forward



Skowronski

System concept



- **+/- 375 urad kick at each bend**
- **0.5% energy spread, 1m dispersion -> 5mm rms**
- **beam pipe diameter >> 50mm**
- **4 kickers at each bend**
- **> 400kW peak power amplifier to each kicker**

IPAC papers

A. Gerbershagen et al:

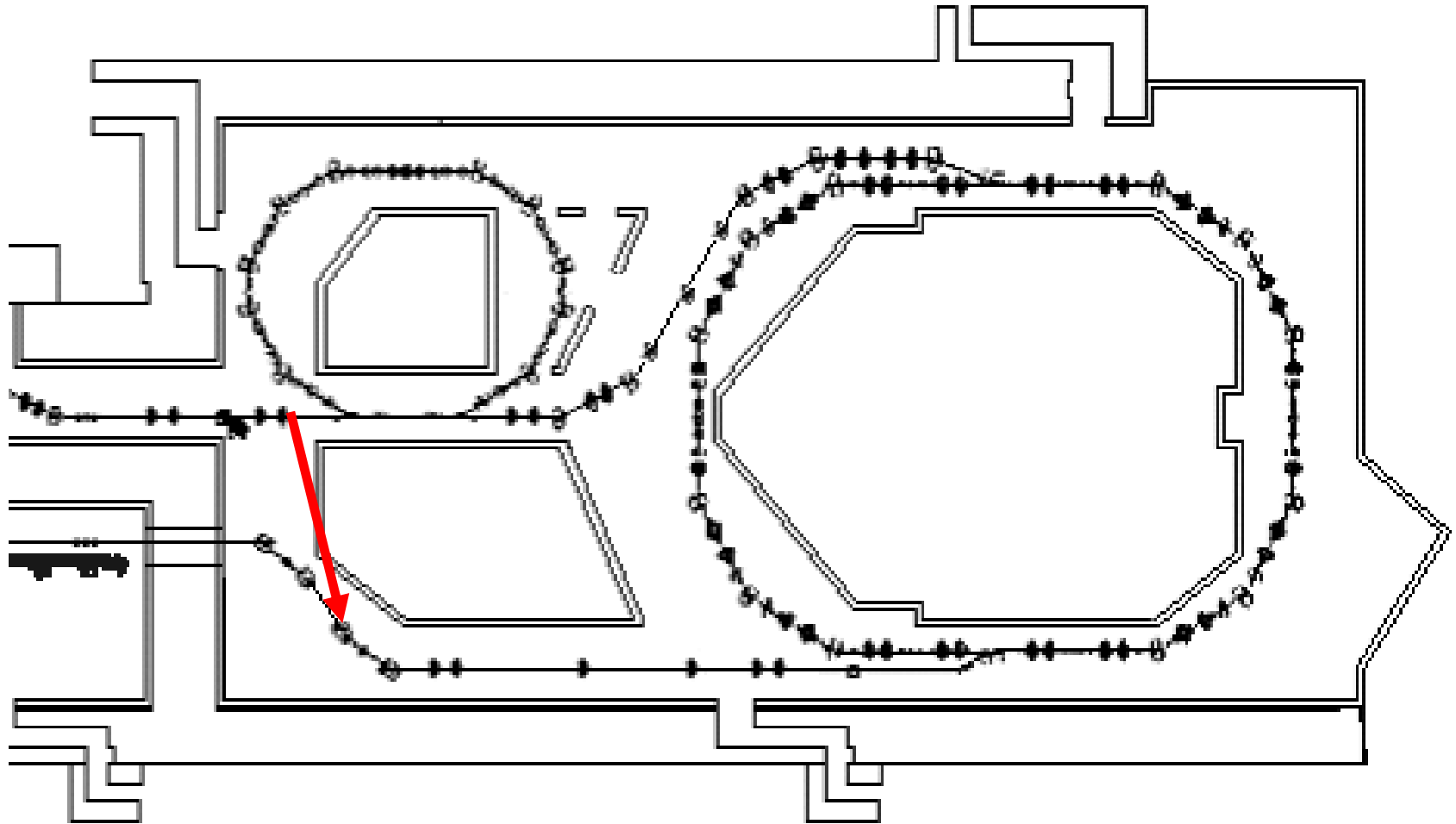
2012:

‘Performance simulations of a phase stabilisation system prototype for CTF3’

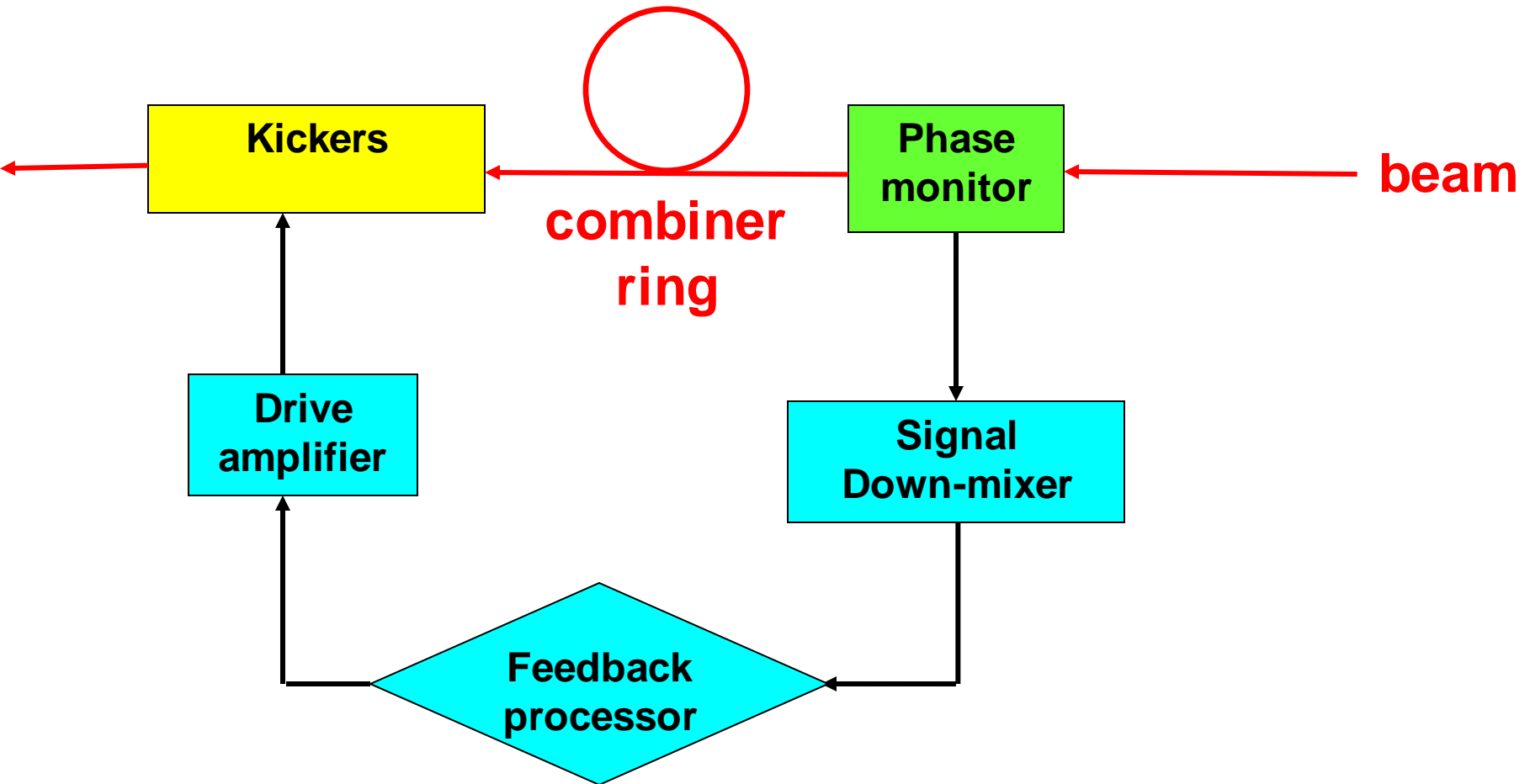
2011:

‘Simulation of Phase Stability at the Flat Top of the CLIC Drive Beam’

CTF3 phase FF prototype



CTF3 phase FF loop layout



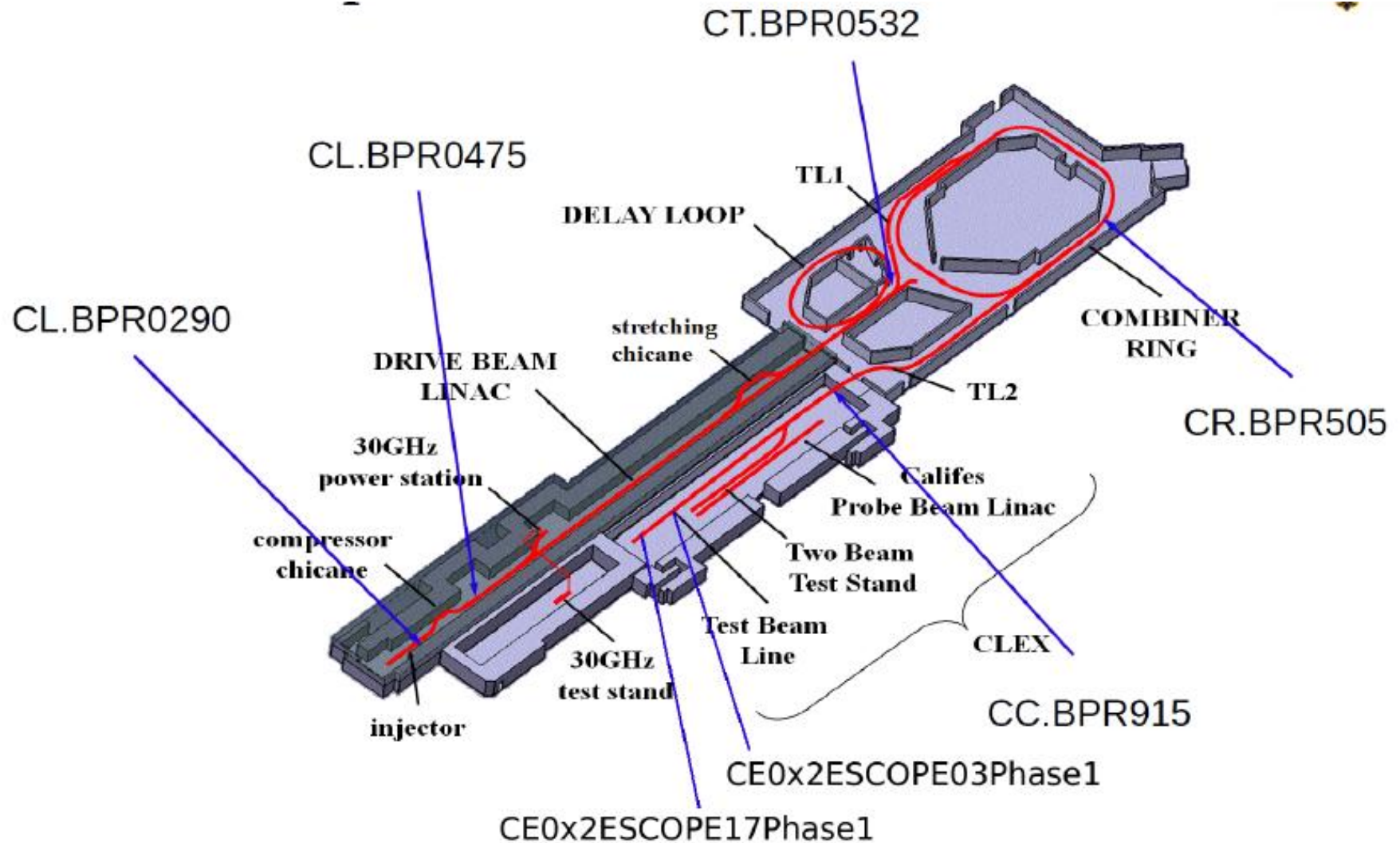
CTF3 phase FF prototype

- **Phase monitor (Frascati)**
 - **Signal down-mixer (CERN)**
 - **Feedback processor + firmware (JAI Oxford)**
 - **Drive amplifier (JAI Oxford)**
 - **Kickers (Frascati)**
- 1 mrad kick
- 1.2 mm path length change
- 17 degrees at 12 GHz

Schedule

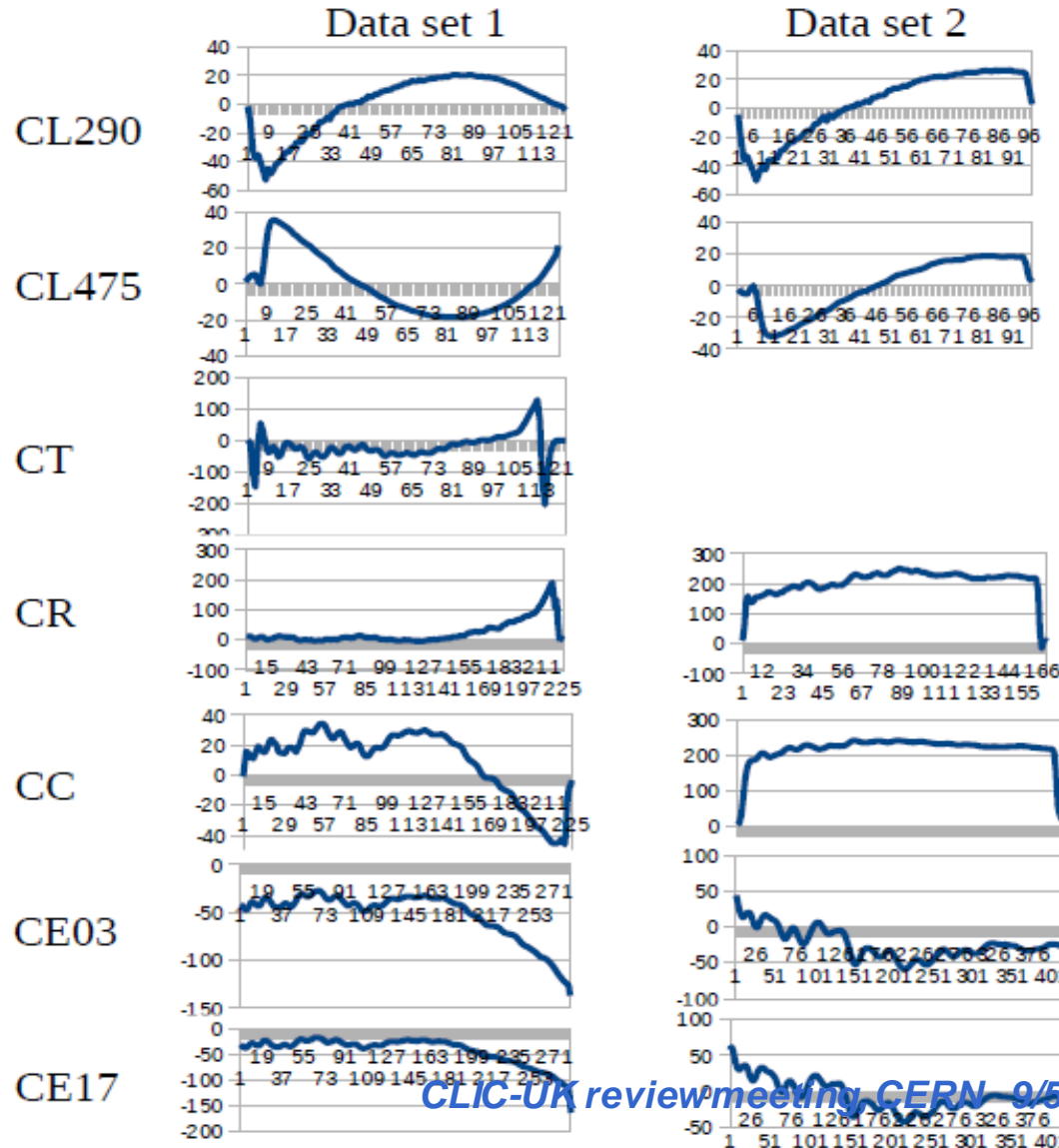
- **Phase monitor installation: summer 2012**
 - get experience with phase monitor r/o
 - digitisation of signals
 - develop + test firmware
- **Kicker installation: winter 2012/3**
- **Amplifier ready: winter 2012/3**
 - test kickers: spring 2013
 - system tests: spring/summer 2013

Existing phase monitors

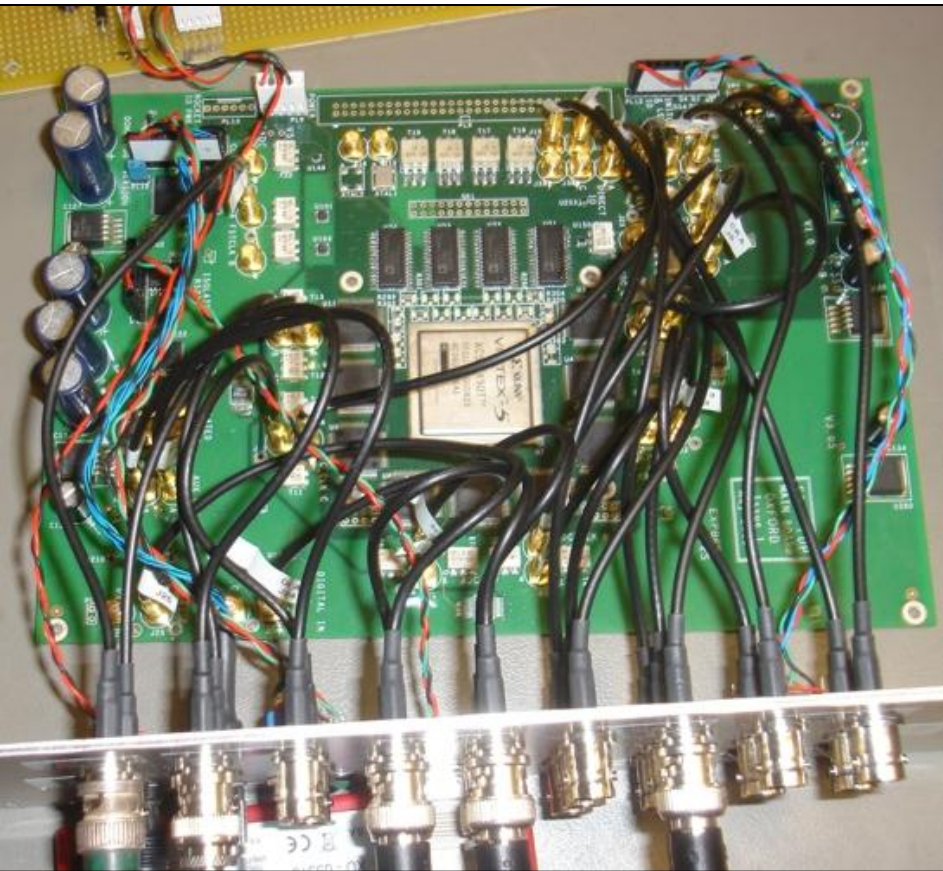


Existing phase data

- Short phase data runs in December 2011
- Gave us a look at the problem
- Interesting effects!
- More beamtime needed when possible



Digitisation + FB



FONT5 digital FB board

Xilinx Virtex5 FPGA

**9 ADC input channels
(TI ADS5474)**

**4 DAC output channels
(AD9744)**

**Plan to clock at 250 MHz
phase-locked to beam**

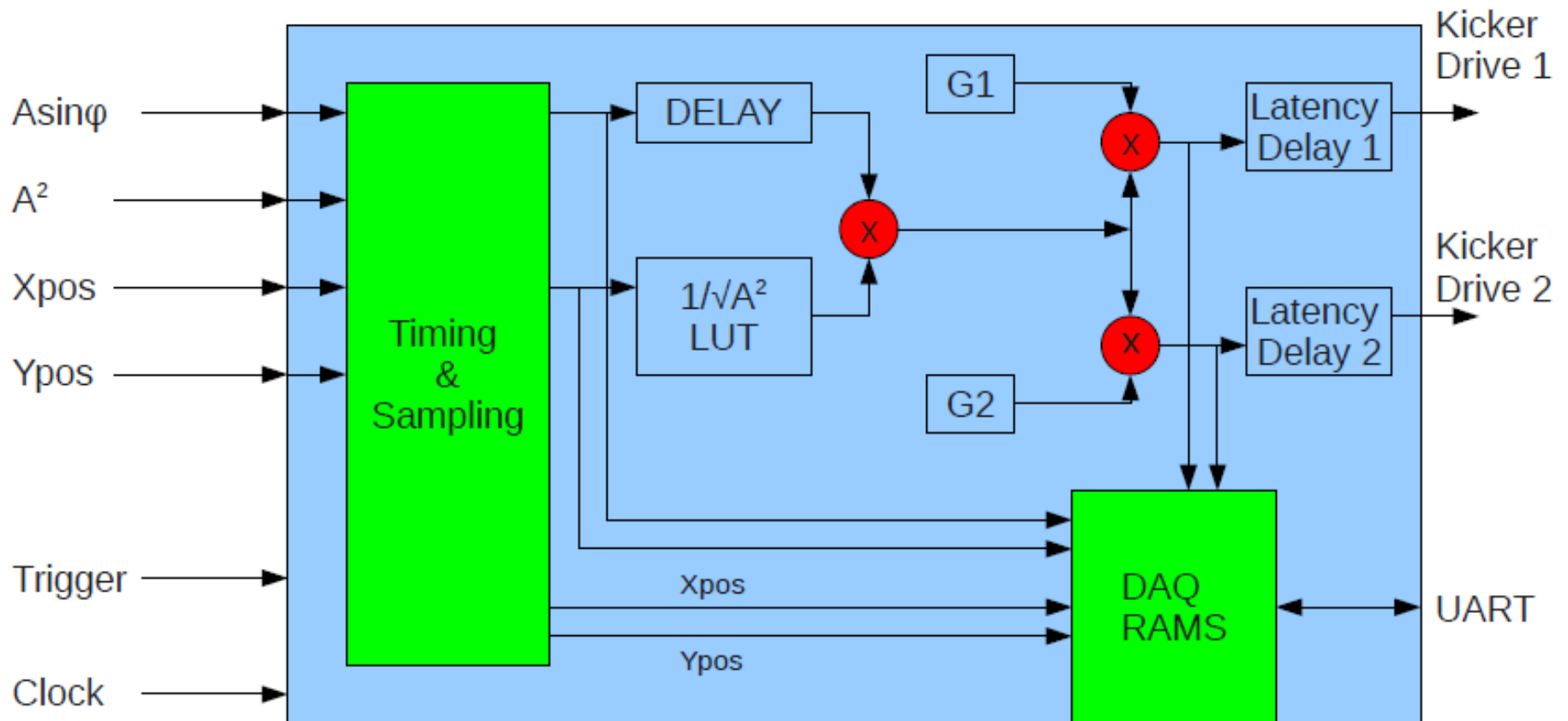
Need to fabricate 2 more boards for CTF3

Digitisation + FB

- **Digitise $A \cdot \sin(\phi)$, A^2 , $x + y$ position ...**
- **Reuse as much of existing firmware as possible**
- **Use 250 MHz clock (phased to beam)**
- **280 samples per pulse on uncombined beam, 35 for combined**
- **Triggering: free running or hold off from pre-trigger?**
- **Standalone DAQ (Labview)**
- **Data transfer to CTF3 controls system**

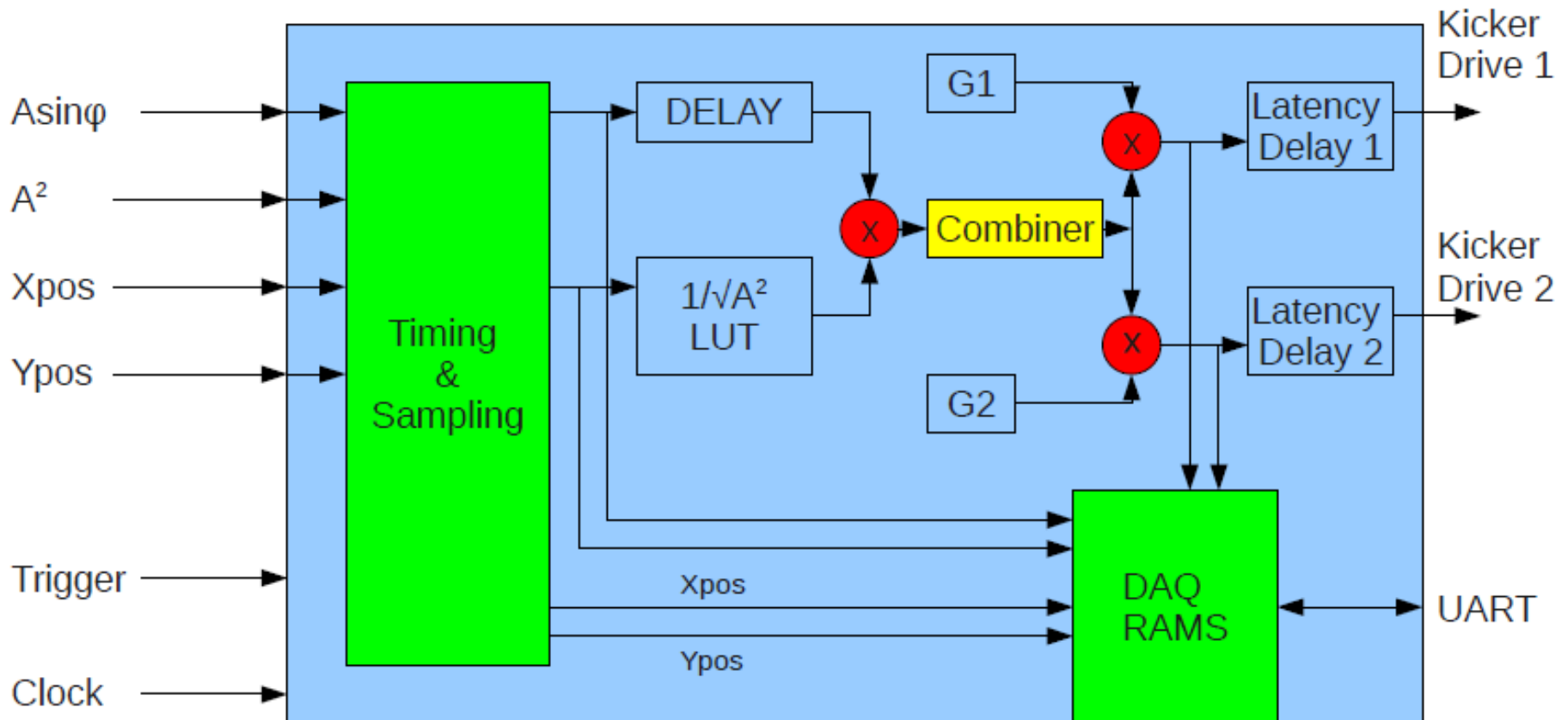
Digitisation + FB

Basic firmware (uncombined beam)



Digitisation + FB

Basic firmware (any beam)



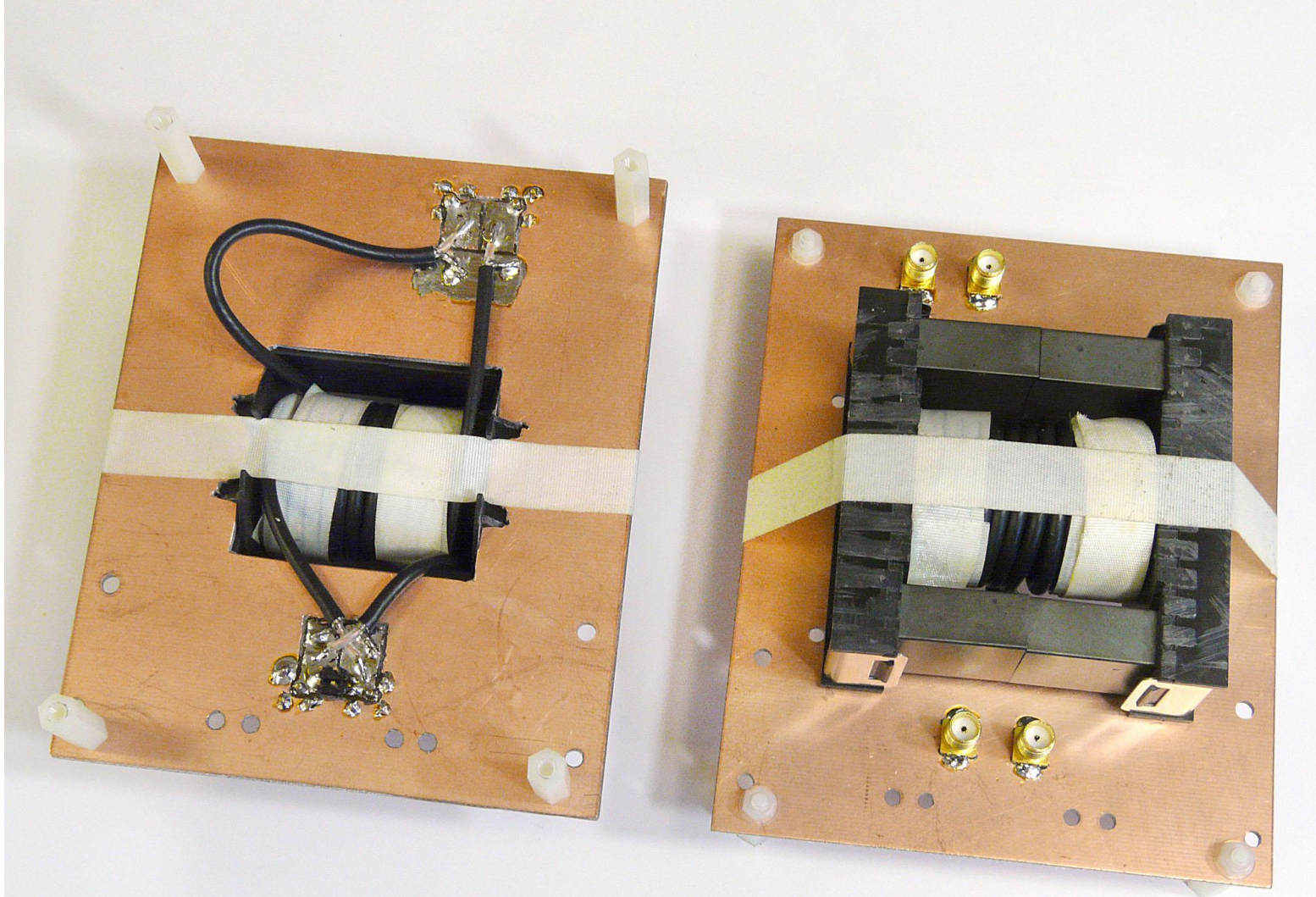
FF amplifier status

- Extensive discussions, design work, component specification and product searching
- Proceeding with fabricating a first-phase CTF3 amplifier
- Target is +/- 17 degrees (12 GHz) dynamic range
- Pulse length up to 1.2us (uncombined beam)
- Bandwidth > 50MHz
- Separate 'slow' FB correction system – see later
- Ordered all critical and long lead-time components (SiC + Si FETs received)

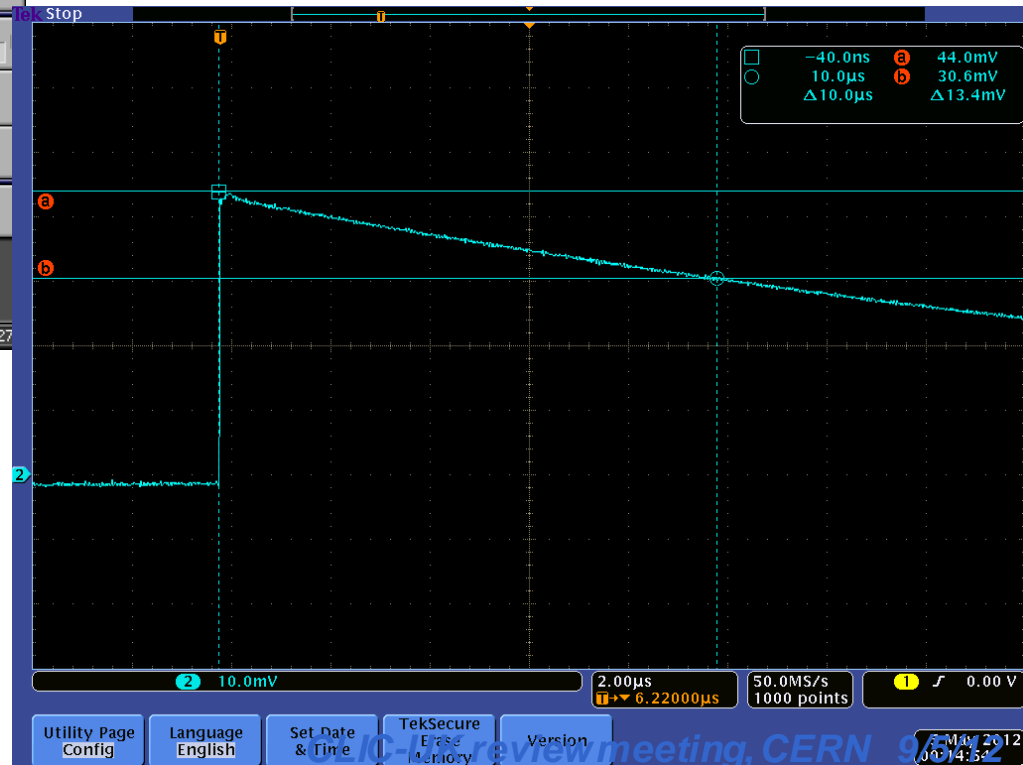
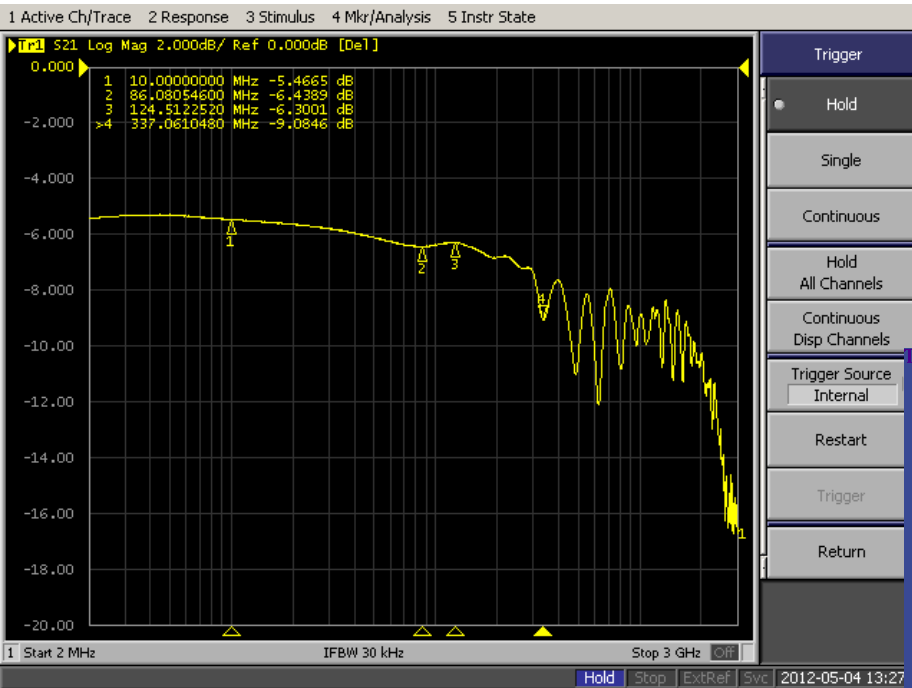
Amplifier design

- **Comprises 4 parallel modules**
each with output transformer and 600V power converter in 220mm deep IEC297 module, 12HP (61mm) wide
- **These plug into 3U (133mm) high sub-rack, which houses output power combiner/transformer**
- **Drive and control module**
- **External DC supply, 50W; no cooling needed**

Prototype output transformer



Output transformer response



Amplifier output stage

- Each module has pair of 1200V Cree SiC FETs, driven by pair of LV IxysRF Si FETs in 'cascode' configuration
 - nominal peak power 18 kW (up to 20kW)
 - o/p bandwidth >50MHz (expect 60MHz)
- Combined output
 - nominal 65kW (up to 75kW)
 - +/-1270V on kicker strips (diff. 100 Ohm)
 - +/- 0.97 mrad or +/- 17 degrees at 12GHz
 - droop < 10% over 1.2us pulse

Slow corrections (FB)

- **‘Static’ shape corrections**
- **Slow amplitude variations on seconds timescale**
- **Cannot be handled with full b/w at large amplitude**
- **Superimpose ‘electrostatic’ correction on strips**
- **Assuming HN connector limited to 5kV, use bipolar DC supply of ± 5 kV**
 - ± 1.9 mrad (electrostatic only)
 - ± 34 degrees (12 GHz)
- **Ultravolt 5HVA24-BP1 ‘high voltage amplifiers’ x4**
 - full swing in 150ms

Summary on phase FF

- Got some data with existing phase monitors
→ more needed
 - Proceeding with first CTF3 prototype design
→ all critical components in hand
 - Scheme for additional 'slow' FB correction
→ suitable amplifiers identified
 - Will use FONT5 FB board → need to fabricate x2
 - Firmware design progressing well
 - First pass at rack locations, cables, controls ...
- Detailed technical discussion Thursday 16.00