CTF3 Drive Beam Feed Forward Amplifier - Status

Amplifier status

- **Extensive discussions, design work, component specification and product searching**
- **Proceeding with fabricating a first-phase CTF3 amplifier**
  - **Aims to meet CTF3 requirements, second phase may be unnecessary.**
- **Target is +- 17 degrees (12 GHz) dynamic range**
- **Pulse length up to 1.2us (uncombined beam)**
- **Bandwidth > 50MHz**
- **Separate ‘slow’ FB correction system – see later**
- **Ordered all critical and long lead-time components (SiC + Si FETs received)**

System Configuration

- **Comprises 4 parallel modules**

  each with output transformer and 600V power converter in 220mm deep IEC297 module,

  12HP (61mm) wide
- **These plug into 3U (133mm) high sub-rack, which houses output power combiner/transformer**
- **Drive and control module**
- **External DC supply, 50W; no cooling needed**

Amplifier Design 1

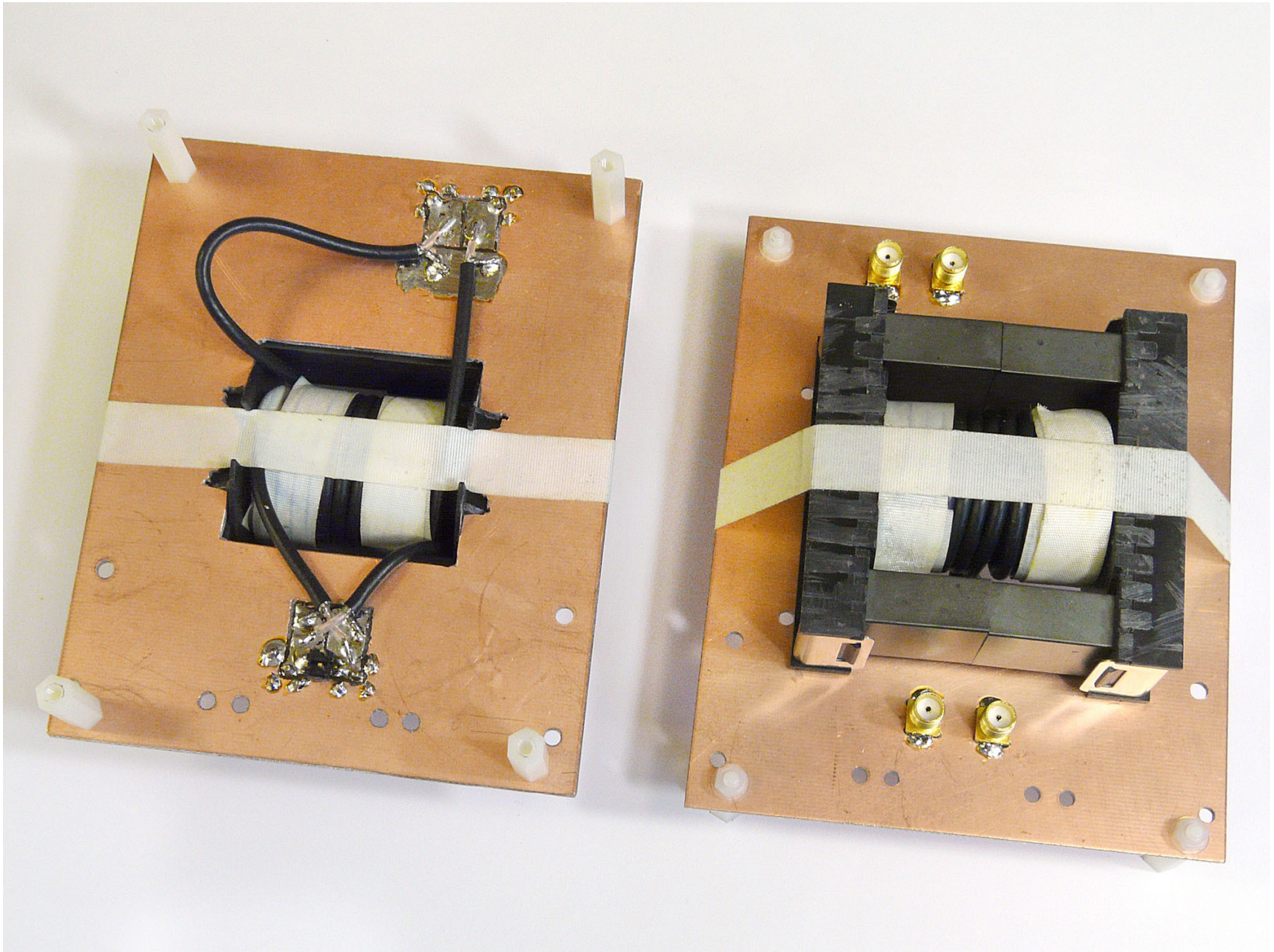
Output Stage

- Each module has pair of 1200V Cree SiC FETs, driven by pair of LV IxysRF Si FETs in ‘cascode’ configuration
- nominal peak power 18 kW (up to 20kW)
- o/p bandwidth >50MHz (expect 60MHZ)
  - Slew rate limited for large changes (see later)

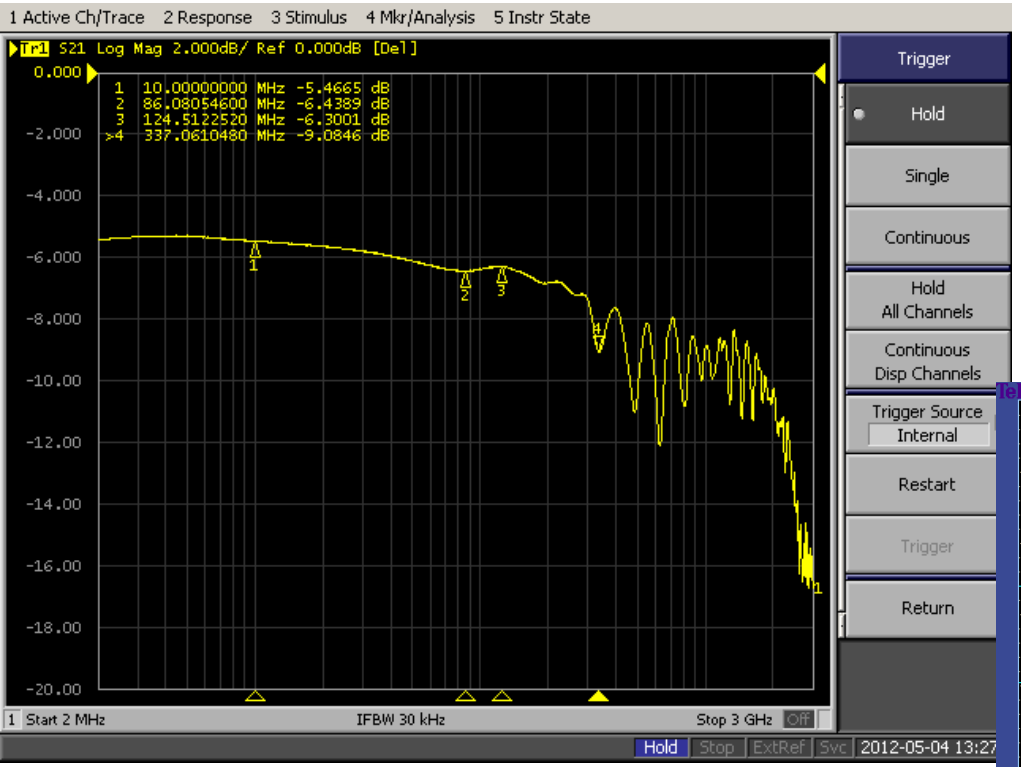
Transformers

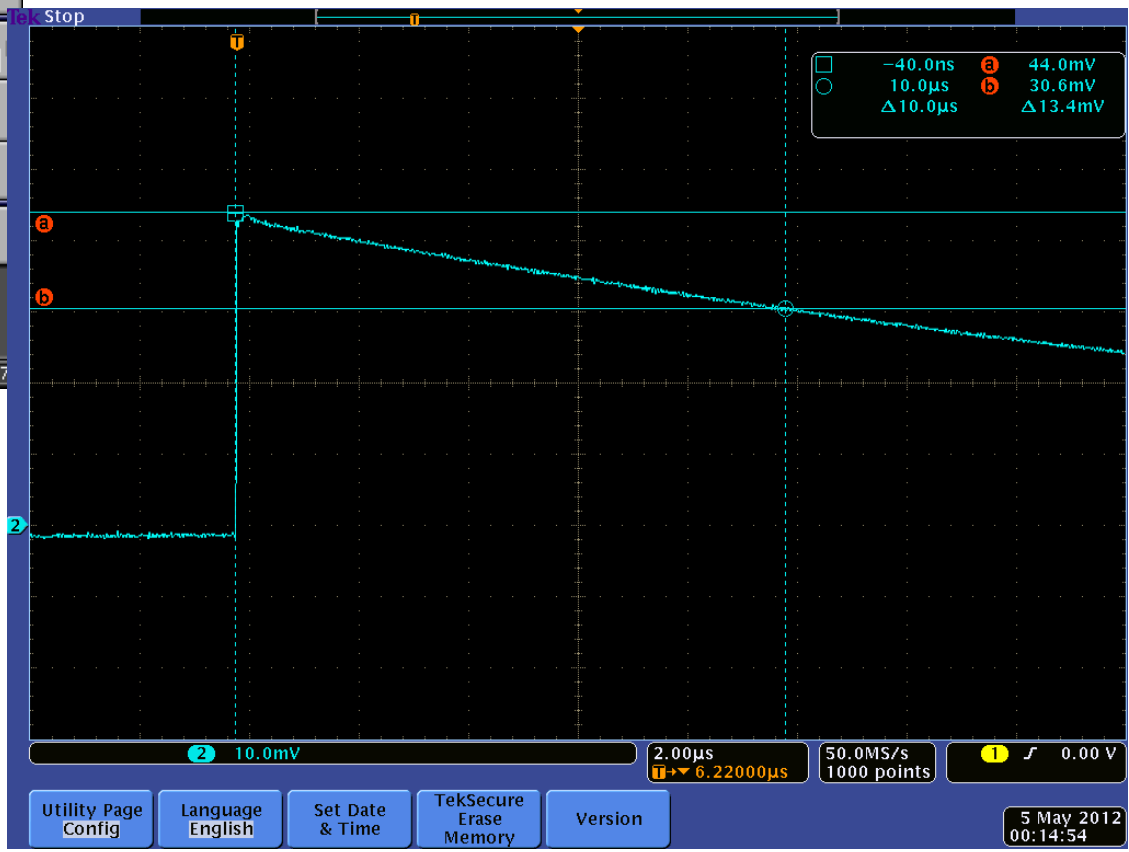
- Second most critical part – two versions calculated
- Expected to support unrestricted operation to the full 1.2 us but short-fall possible
  - At least 600 ns with no limitation but 1.2 us usable
- High frequency response ok; low frequency response also adequate
  - Droop <10% over full 1.2 us duration

Prototype output transformer



Output transformer response





Amplifier Design 2

Drive

- **Nominal output power per module 18 kW (15-20 kW)**
- **Combined output: 65 kW nominal (55 – 75 kW)**
- **+/- 1270 V (into 100 ohms diff) on each side**
- **+/- 0.97 mrad (+/- 19.5 degrees @ 12 GHz)**

Speed

- **At least 50 MHz (target 60 MHz)**
- **Slew rate limited for large corrections – full power not available for at full bandwidth**
  - **Should be fine for small, rapid variations seen in previous phase data**
  - **Potential problem at start of pulse – from zero to large initial phase error. Can correct for this in firmware (see later)**

Option for slow correction

- **Can not handle slow 80-100 degree variations across the full uncombined pulse, nor slow fluctuations in mean phase on pulse-to-pulse timescales**
- **Superimpose ‘electrostatic’ correction on strips**
  - **Blocking capacitors to block DC bias from fast amplifier and terminating resistors**
- **Assuming HN connector limited to 5kV, use bipolar DC supply of +-5 kV**

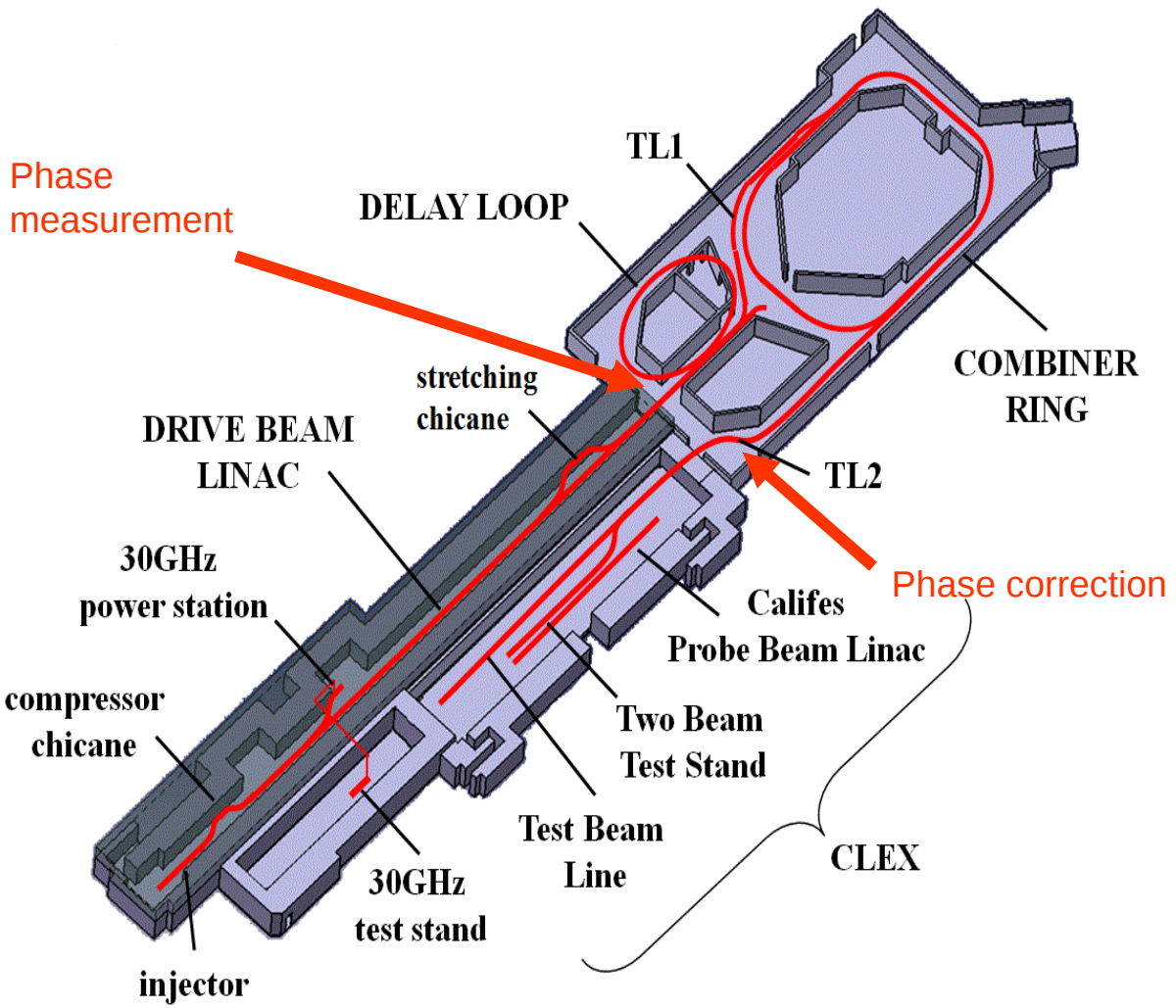
  → +-1.9 mrad (electrostatic only)

  → +- 37 degrees (12 GHz)
- **Ultravolt 5HVA24-BP1 ‘high voltage amplifiers’ x4**

  → full swing in 150ms

CTF3 phase FF firmware

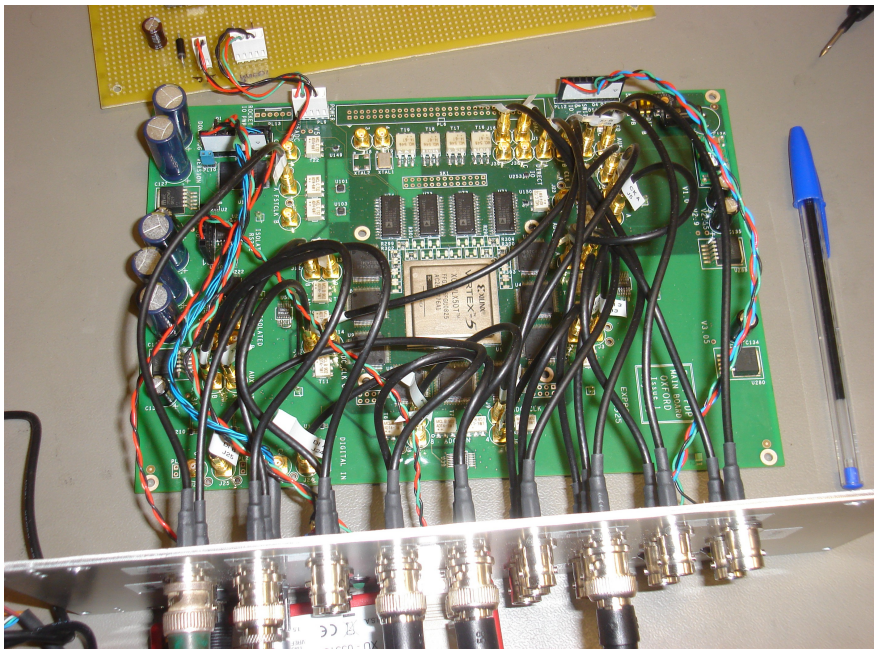
CTF3 phase feed-forward



- For uncombined beam, simple 1-1 correspondence between phase measurement and correction
- For combined beam, measurements from eight sub-pulses will be folded together and averaged to take account of effect of combination scheme at correction point. Each correction is average of appropriate samples from the 8 sub-pulses.

Reminder: FONT5 board

- Xilinx Virtex5 FPGA (XC5VLX50T)- (max clock 550 MHz)
- 9 input channels (with three independent clocks), 4 DAC channels (2 patched to front panel)
- 14-bit (13 effective bits) ADCs/DACs:
  - ADCs: ADS5474 (max clock 400 MHz)
  - DACs: AD9744 (max clock 210 MHz)
- Fast clock comparator for ext clock and onboard 40 Mhz oscillator
- Serial output via RS232



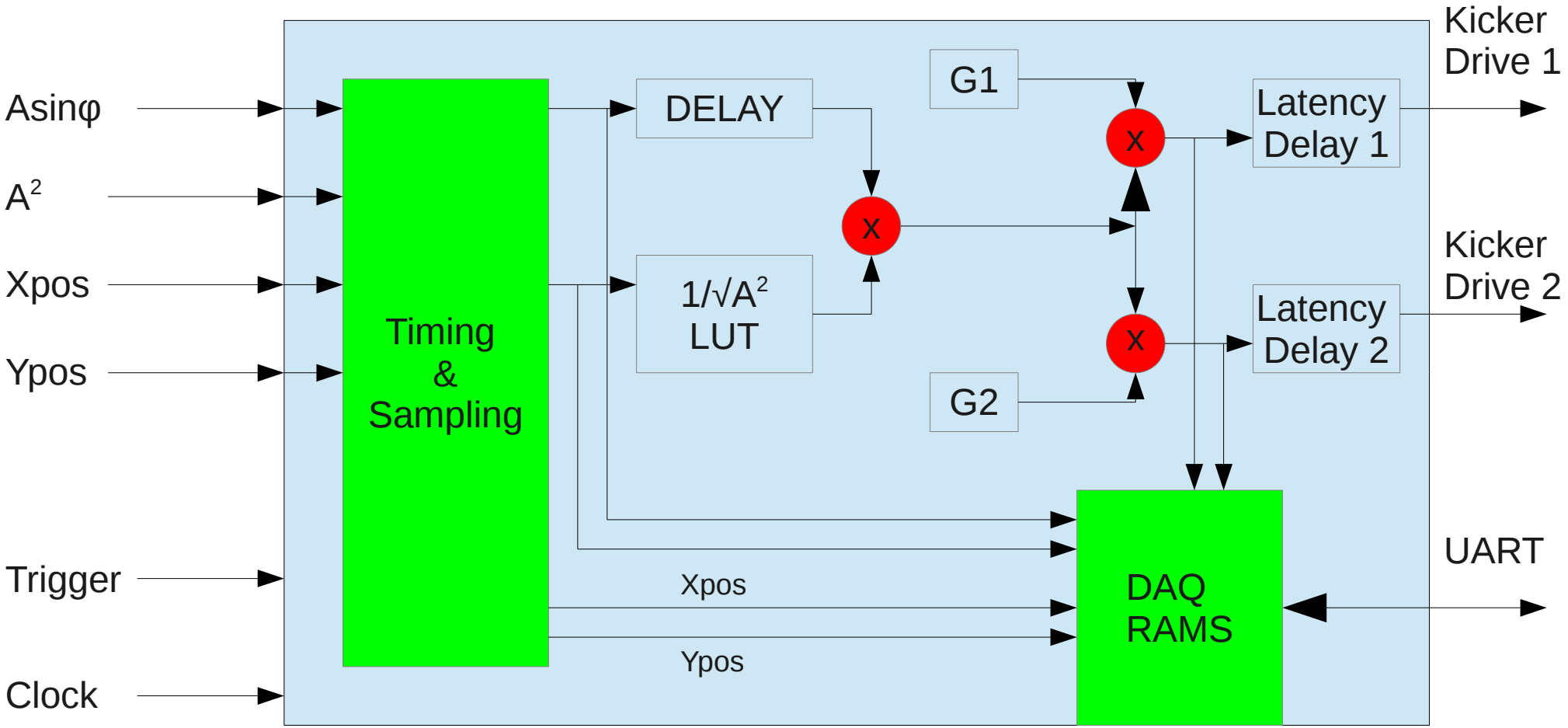
General considerations

- Will need to digitise Asin(phi) and A**2 signal + also perhaps X and Y positions
- Re-use as much of the sampling, DAQ, UART firmware as possible from FONT5 system at ATF
  - Simplifications: no ring clock, no need for independent sampling clocks
- System clock - 250 MHz readily available
  - 280 samples per pulse on uncombined beam, 35 for combined
  - Will be baseline clock speed

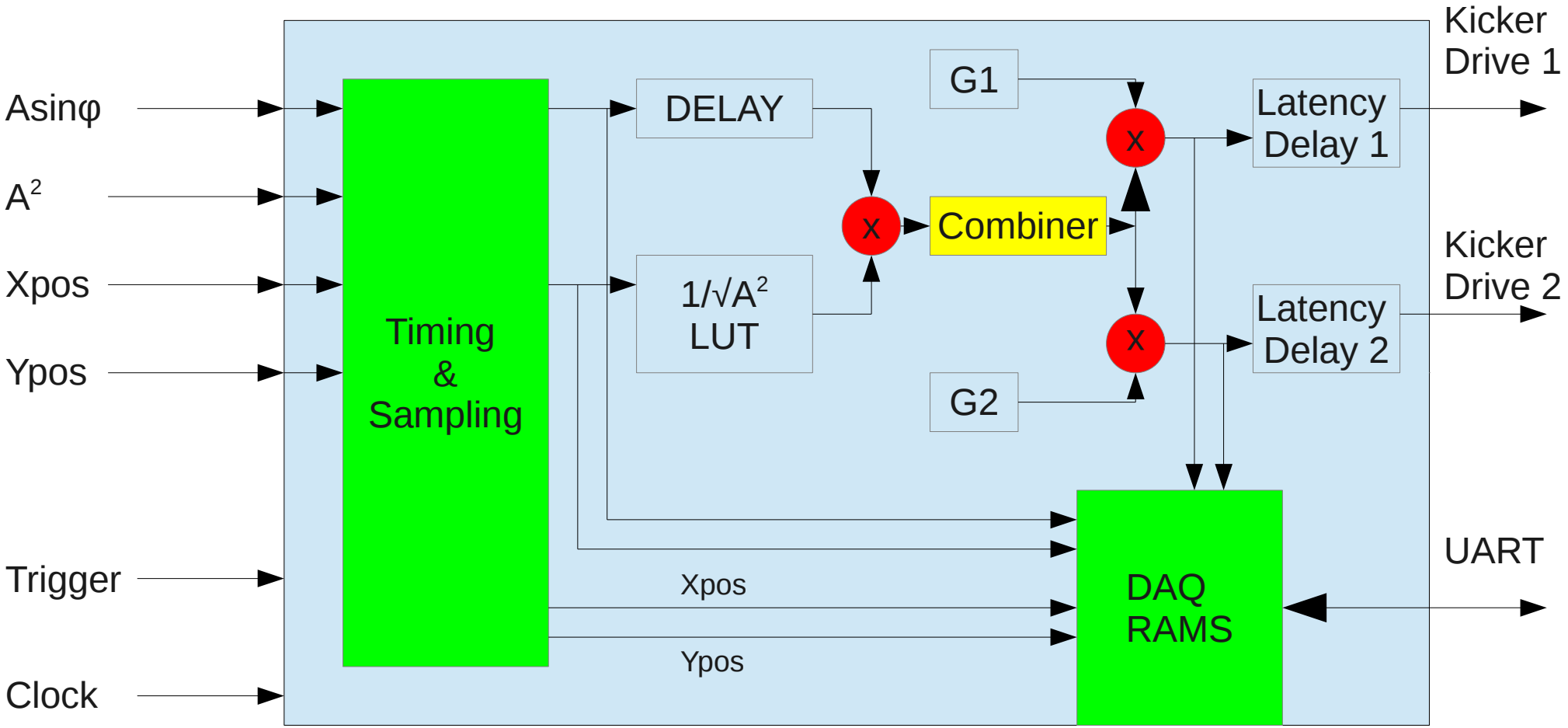
General considerations 2

- Triggering options
  - 1) free-running – start of pulse determined by charge thresholding
    - Needs stable charge
  - 2) Hold off from trigger
    - Needs stable trigger wrt pulse
  - Will probably support both options, Option 2 default.
- In terms of DAQ - flexibility may be required in number of samples recorded and when
- Assume time structure of pulse will not change
  - Only important for combined beam, but set by the lengths of the DL and CR anyway.

Basic firmware (uncombined beam)

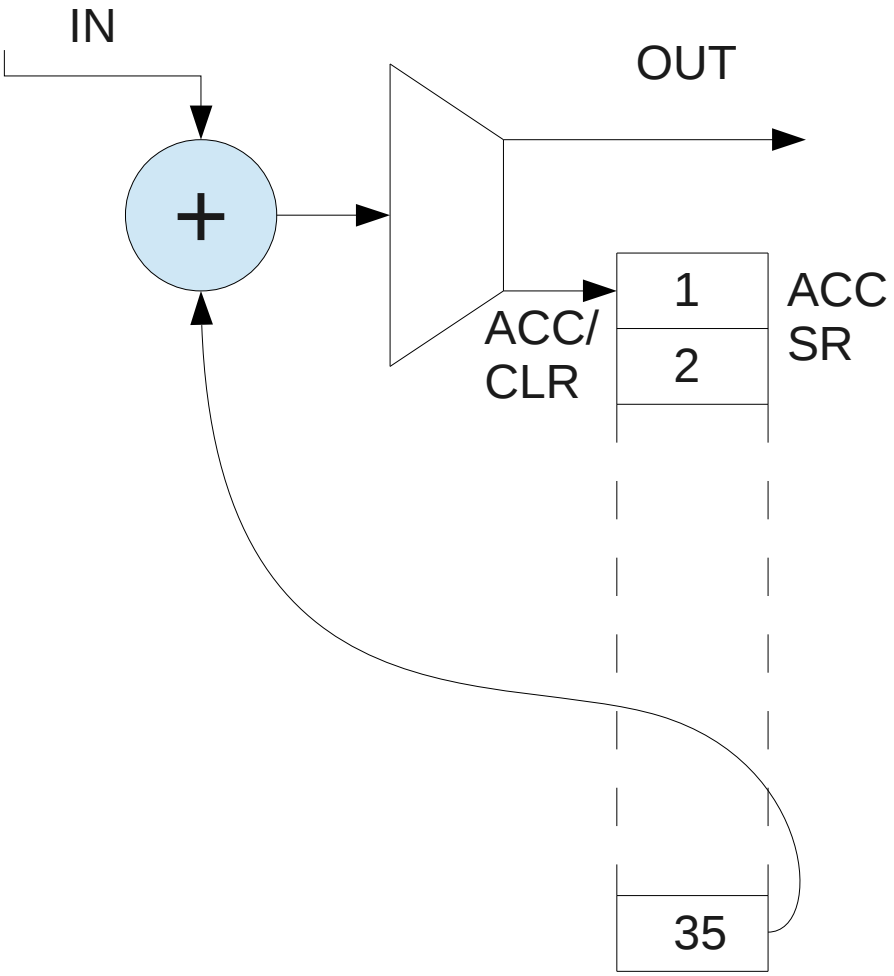


Basic firmware (any beam)

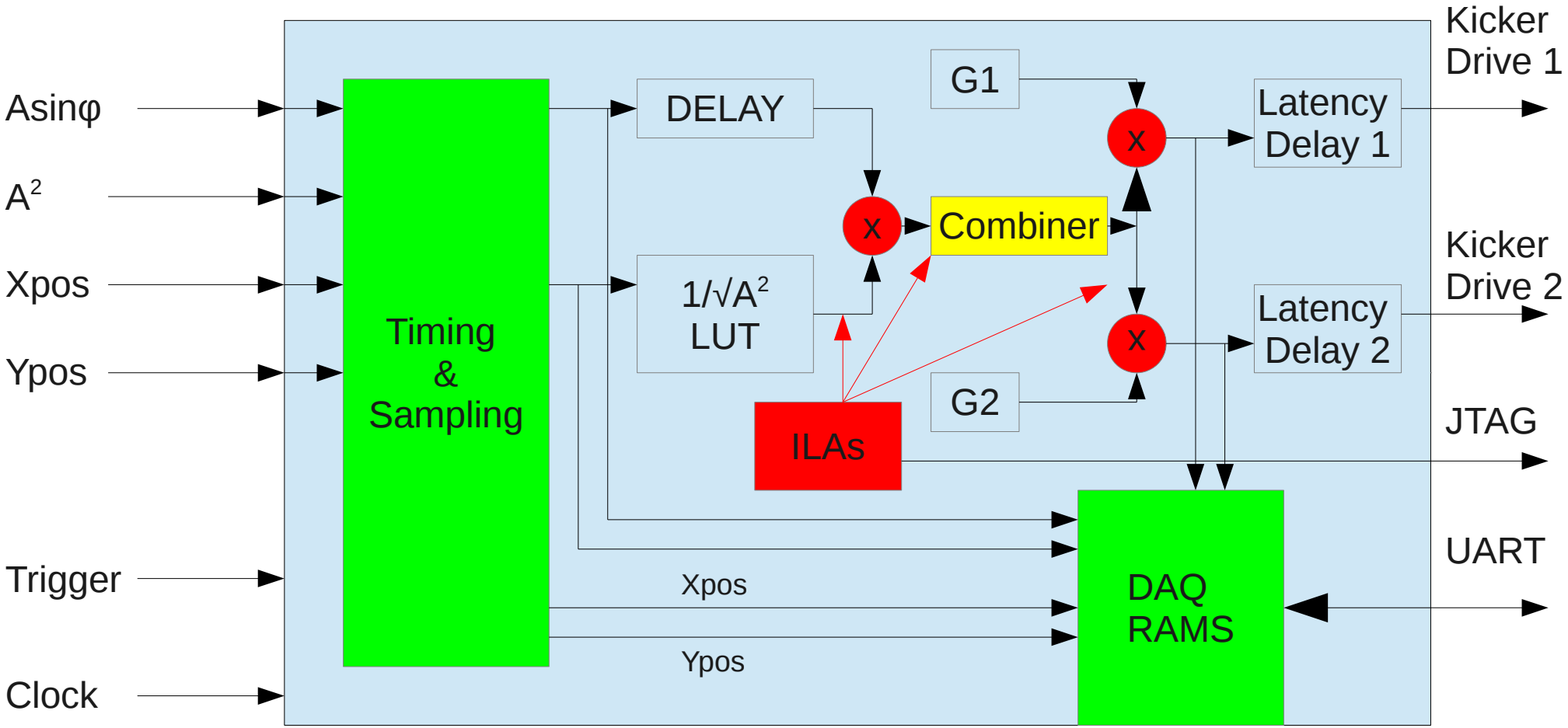


Combiner Module

- Simple 35-deep SR (assuming 250 MHz clock) + accumulator
  - Will work for combination factor 1 (uncombined), 2 (DL only), and 8 (DL +CR). CF 4 unphysical?
  - Output right shifted by appropriate amount
  - Latency delay same for each mode
  - For CF=1, accumulator bypassed, for CF=2 run through SR once, for CF=8 run through 7 times



Basic firmware (any beam)



Additional Options

- Slew rate compensation
  - For small amplitude phase errors response flat to 50 MHz, for larger amplitude errors slew rate limited
  - Only expected to be an issue at start of pulse – slew from zero to initial phase error
  - 2 options:
    - 1) For uncombined beam, put out first correction signal ~30 ns before beam arrives, provided enough range of 'latency delay'
    - 2) For combined beam, can put out average corrections early (e.g. after 6 times through SRs for CF=8)
      - Only really needed if not enough delay in option 1.,
    - Will plan to do both
- Weighted averaged based on charge
- Averaging of phase measurements in FPGA (uncombined beam)
  - Powers of two, depending on range of 'latency delay'

DAQ

- Imagine we will use standalone DAQ software in eg LabVIEW
  - Build on experience with DAQ at ATF
  - Can forward data and allow remote setting of variables etc through database, eg. EPICS or whatever used at CTF
  - Requires PC local to FF controller for RS232 connection and JTAG for remote reconfiguration/ test and debugging

Plan

- Start with stripped back firmware (done for DR monitoring F/W a few years ago)
- Have modified 9 channel digitisation and DAQ version ready for monitoring three PhMs at end of linac
  - Make checks of signals, resolution, correlations etc
- Feedforward firmware to follow shortly after
  - Combiner module will be done last but will probably not take any more time than uncombined F/W