# High Resolution Pixel Technologies Developed for an ILC Micro-Vertex Detector

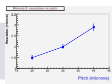
**Marc Winter** (IPHC-Strasbourg)

**contributions:** V.Re (CMOS sensors / INFN-Pavia), L.Andricek (DEPFET / MPI-Munich), M.Demarteau (3D sensors / FNAL-Chicago)

▷ **More information on ILC Web site:** **http://www.linearcollider.org/cms/**

## OUTLINE

- **Requirements for a Vertex Detector at ILC**
  - *Constraints from physics goals*
    - *Constraints and Benefits from running conditions*
      - *Example of vertex detector geometry*
- **Vertex detector technologies easiest to transpose to CLIC running**
  - *CMOS sensors (1st & 2nd generation)*
  - *DEPFETS*
  - *3D integrated sensors*
- **Conclusion – Perspectives**




# Main Requirements

## for the ILC Vertex Detector :

- Physics goals
- Running conditions

# Constraints from the Physics Goals

- **Overall objective: identify $\sim$ all flavours involved in most final states**

  **Ex: $e^+e^- \longrightarrow ZH$ $\Rrightarrow$ measure Br ($H \longrightarrow c\bar{c}, \tau^+\tau^-, b\bar{b}, gg, ...$)**

- **In practice:**
  - ▷ *tag $c$ and $\tau$ jets with unprecedented efficiency & purity ($b$ tagging much less challenging)*
  - ▷ *reconstruct very efficiently Vx1 $\longrightarrow$ Vx2 $\longrightarrow$ Vx3 $\longrightarrow$ ....*
  - ▷ *reconstruct vertex flavour and electrical charge ...*
  - ▷ *cope with high jet multiplicity final states containing numerous $b, c, \tau$ jets*
  - ▷ *minimise secondary interactions (missleading particle flow reconstruction)*
  - ▷ *etc.*

- $\sigma_{IP} = a \oplus b/p \cdot \sin^{3/2}\theta$ **with $a < 5\ \mu m$ and $b < 10\ \mu m$**

  ▷ **limits on $a$ and $b$ are still "very educated guesses"** ▷ **SLD: $a$ = 8 $\mu m$ and $b$ = 33 $\mu m$**

  • $\sigma_{sp} \lesssim 3\mu m$ • **$R_{in} \sim$ 1–2 cm** • **$R_{out} \sim 4 \cdot R_{in}$** • **VD layer $\sim$ 0.1–0.2 % $X_0$** • **beam pipe $\sim$ 0.1 % $X_0$**

- *Constraint on $\sigma_{IP}$ satisfies simultaneoulsy requirement on 2-hit separation in inner most layer ($\sim$ 30 – 40 $\mu m$)*

- **Overall objective: come as close as possible to IP $\longrightarrow$ minimise $\mathbf{a}$ and $\mathbf{b}$ ($\propto \mathbf{R_{in}}$)**

  $\Rrightarrow$ **beam background induced by high luminosity :**

  *Beamstrahlung $\mathbf{e^{\pm}}$ $\Rrightarrow$ inner layer constraints prevent $\mathbf{a}$ & $\mathbf{b}$ to be well below their upper bounds*

  $\hookrightarrow$ *Inner most layer: BG generates O($10^7$) hits/s while Physics generates O($10^2$) hits/s*

- **In practice:**

  ▷ *experimental magnetic field should be as high as possible ($\sim$ 3–5 T) $\longrightarrow$ sweep away most $\mathbf{e^{\pm}_{BS}}$*

  ▷ *$\mathbf{e^{\pm}_{BS}}$ rate still $\lesssim$ 5 hits/cm$^2$/BX at R=15 mm ($\sqrt{s}$ = 500 GeV, 4 T) $\longrightarrow$ O($10^3$) pixels /cm$^2$/10 $\mu s$*

  ▷ *foster high read-out speed in inner layers against occupancy $\lesssim$ few tens of $\mu\mathbf{s}$*

  ▷ *rad. level not negligible at $T_{\mathbf{room}}$ (mat. budget ?): • $\sim$ 50 kRad/yr • $6 \cdot 10^{11} e^{\pm}_{10\ MeV} \approx 2 \cdot 10^{10} n_{eq}$/cm$^2$/yr*

  ▷ *prediction accuracy $\Rrightarrow$ prepare for 3 ? 5 ? times more BG $\longrightarrow$ • $\sim$ 500 kRad/3 yr • $\sim 2 \cdot 10^{11} n_{eq}$/cm$^2$/3 yr*

  ◇ *neutron dose integrated over 3 years much smaller : $\lesssim 3 \cdot 10^{10}$ $n_{eq}$/cm$^2$ (safety factor of 10)*

- **Power dissipation : avoid increasing mat. budget & complexity with heavy cooling $\Rrightarrow$ air flow**

  ◇ *exploit beam time structure: $\sim$ 1 ms train ($\sim$ 3000 buckets) every $\sim$ 200 ms $\Rrightarrow$ duty cycle $\sim$ 1/200*

  $\Rrightarrow$ *switching off the sensors between trains may allow power reduction by factor of $\sim$ 100*

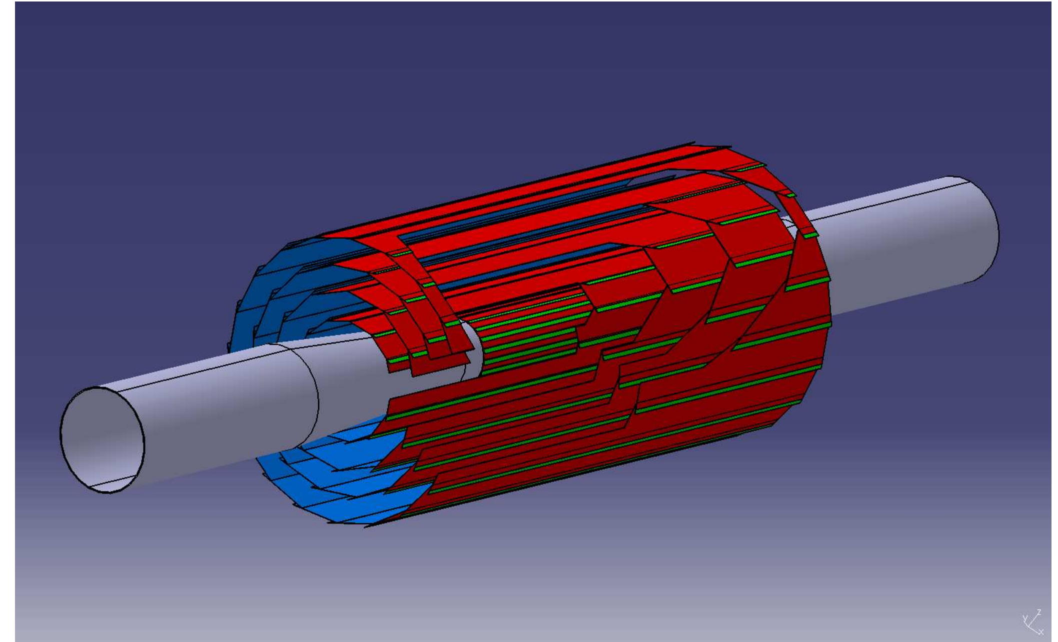
- **EMI : fear that beam delivery elements may be source of very short $\lambda$ EM field**

  ◇ *some sensor architectures developed (variants of CCD & CMOS sensors) foresee r.o. delayed after end of train*

  $\hookrightarrow$ *not transposable to CLIC running conditions $\Rrightarrow$ not reviewed in this report*

- *ILD geometry: $\geq$ 5 cylind. layers (R = 15–60 mm), $\|cos\theta\| \leq$ 0.90 – 0.96* ▷ *SiD: shorter barrel & fw/bw disks*
- *L0 and L1 : optimised against occupancy*
- *L2, L3 and L4 : optimised against power dissipation*
- *Pixel pitch varied from $\sim$ 20 $\mu m$ (L0–L1) to $\gtrsim$ 30 $\mu m$ (L2–L4) $\rightarrowtail$ minimise $P_{diss}$*

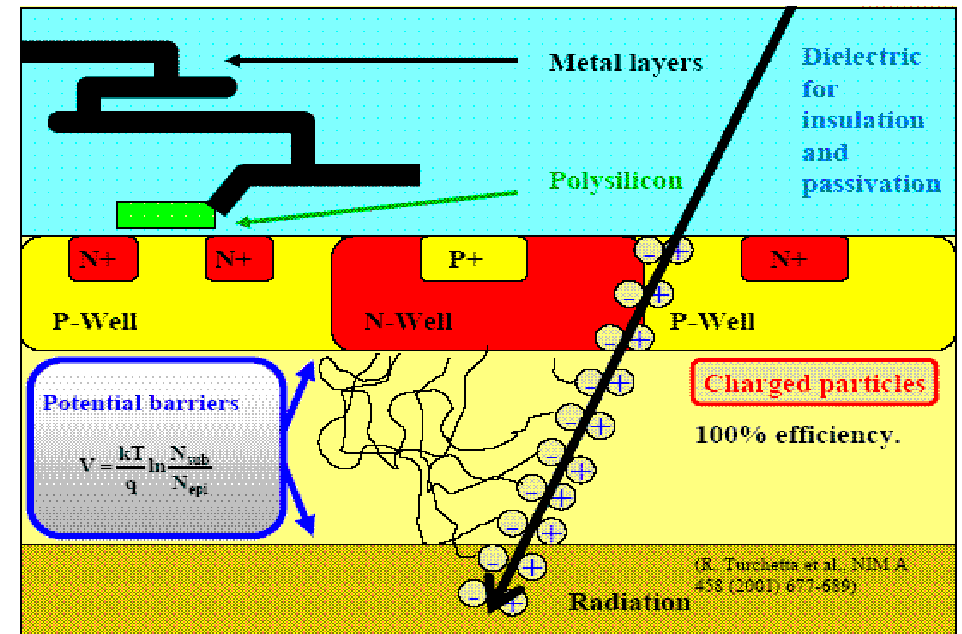
| Layer | Radius (mm) | Pitch ($\mu m$) | $t_{r.o.}$ ($\mu s$) | $N_{lad}$ | $N_{pix}$ ($10^6$) | $P_{diss}^{inst}$ (W) | $P_{diss}^{mean}$ (W) |
|---|---|---|---|---|---|---|---|
| L0 | 15 | 20 | 25 | 20 | 25 | $<$100 | $<$5 |
| L1 | $\leq$ 25 | 25 | 50 | $\leq$26 | $\leq$ 65 | $<$130 | $<$7 |
| L2 | 37 | 33 | $\sim$100 | 24 | 50 | $<$90 | $<$5 |
| L3 | 48 | 33 | $\sim$100 | 32 | 80 | $<$120 | $<$6 |
| L4 | 60 | 33 | $\sim$100 | 40 | 150 | $<$125 | $<$8 |
| Total | | | | 142 | **330** | $<$600 | **3–30** |



- *Ultra thin layers: $\lesssim$ 0.2 % $X_0$/layer (extrapolated from STAR-HFT; $\lesssim$ 40 $\mu m$ thin sensors)*
- *Very low $P_{diss}^{mean}$ : $<<$ 100 W (exact value depends on duty cycle)*
- *Fake hit rate $\lesssim 10^{-5}$ $\rightarrowtail$ whole detector $\cong$ close to 1 GB/s (mainly from $e^{\pm}_{BS}$)*

# PIXEL TECHNOLOGIES DEVELOPED

## for the ILC Vertex Detector :




- **p-type low-resistivity Si hosting n-type "charge collectors"**
  - *signal created in epitaxial layer (low doping):*

    $Q \sim 80$ *e-h* / $\mu m \mapsto$ *signal* $\lesssim 1000\ e^-$
  - *charge sensing through n-well/p-epi junction*
  - *excess carriers propagate (thermally) to diode with help of reflection on boundaries with p-well and substrate (high doping)*

- **Specific advantages of CMOS sensors:**

◇ *Signal processing* $\mu$*circuits integrated on sensor substrate (system-on-chip)* $\mapsto$ *compact, flexible*

◇ *Sensitive volume (*$\sim$ *epitaxial layer) is* $\sim$ *10–15* $\mu m$ *thick* $\longrightarrow$ *thinning to* $\sim$ *30–40* $\mu m$ *permitted*

◇ *Standard, massive production, fabrication technology* $\longrightarrow$ *cheap, fast turn-over*

◇ *Room temperature operation*

◇ Attractive balance between granularity, mat. budget, rad. tolerance, r.o. speed and power dissipation

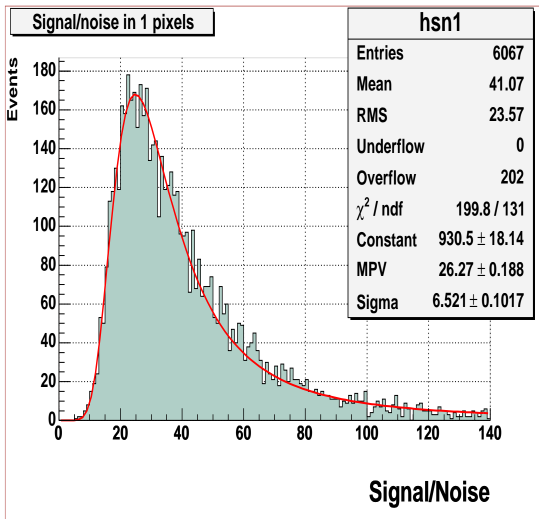
⋈ *Very thin sensitive volume* $\rightarrowtail$ *impact on signal magnitude (mV !)*

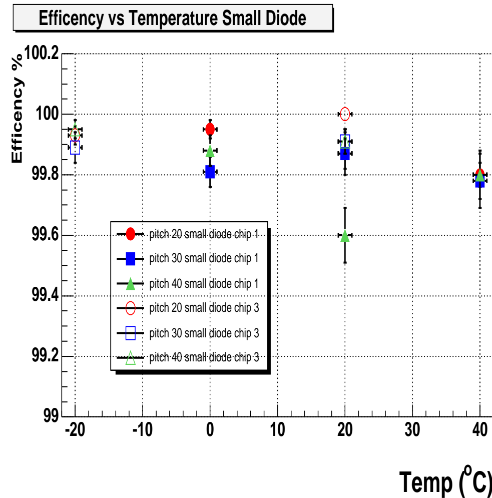
⋈ *Sensitive volume almost undepleted* $\rightarrowtail$ *impact on radiation tolerance & speed*

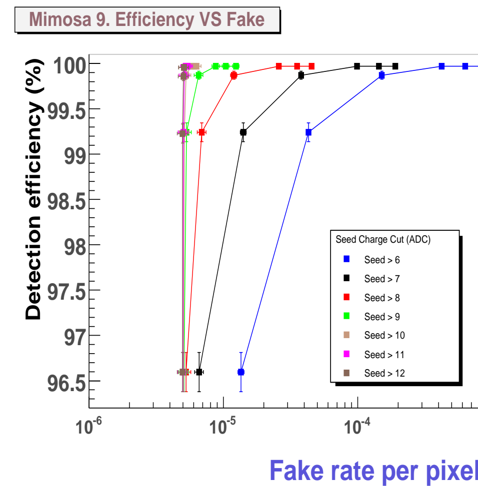
⋈ *Commercial fabrication (parameters)* $\rightarrowtail$ *impact on sensing performances & radiation tolerance*

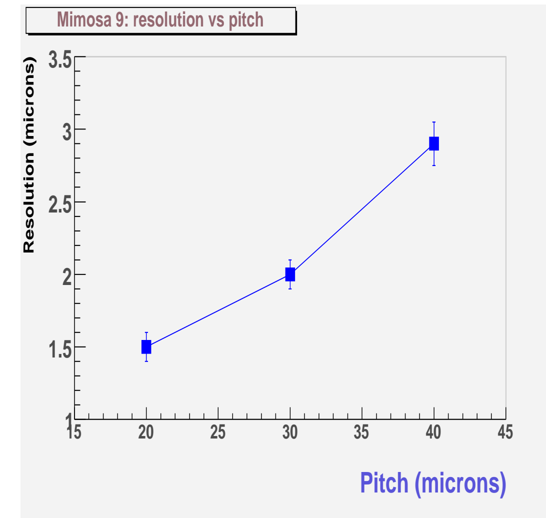
**Numerous MIMOSA chips tested on H.E. beams (SPS, DESY)** $\mapsto$ **well established perfo. (analog output):**

- *Best performing technology: AMS 0.35 $\mu m$ OPTO ($\sim$ 11–15 $\mu m$ epitaxy)*
- *N $\sim$ 10 $e^-$ $\mapsto$ S/N $\gtrsim$ 20–30 (MPV) $\Rrightarrow$ $\epsilon_{det}$ $\sim$ 99.5–99.9 % for fake rate $\lesssim$ $10^{-5}$*
- *$T_{oper.}$ $\gtrsim$ 40 $^\circ$C*
- *Spatial resolution exploits charge sharing between pixels: $\sigma_{\mathbf{sp}}$ $\sim$ 1 – 1.5 – 2 – 3 $\mu m$ for 10 – 20 – 30 – 40 $\mu m$ pitch*
- *Radiation tolerance: $\gtrsim$ 1 MRad (10 keV X-Ray) ; O($10^{13}$) $e^{\pm}$ (10 MeV) ; $\lesssim$ O($10^{13}$) $n_{eq}$/cm$^2$*
- *Technology without epitaxy also performing well : very high S/N but large clusters (hit separation $\searrow$)*
- *Macroscopic sensors : MIMOSA-5 ($\sim$ 3.5 cm$^2$ ; 1 Mpix); MIMOSA-20 (1x2 cm$^2$ ; 200 kpix); MIMOSA-17 (.8x.8 cm$^2$ ; 65 kpix)*
- *Several 0.3–3 cm$^2$ sensors thinned successfuly to $\lesssim$ 50 $\mu m$*
- *Sensors adapted to applications with $\lesssim$ $10^3$ frames/s: B.T. of EUDET (FP6), TAPI (Strasbourg), of LBNL; STAR telescope*



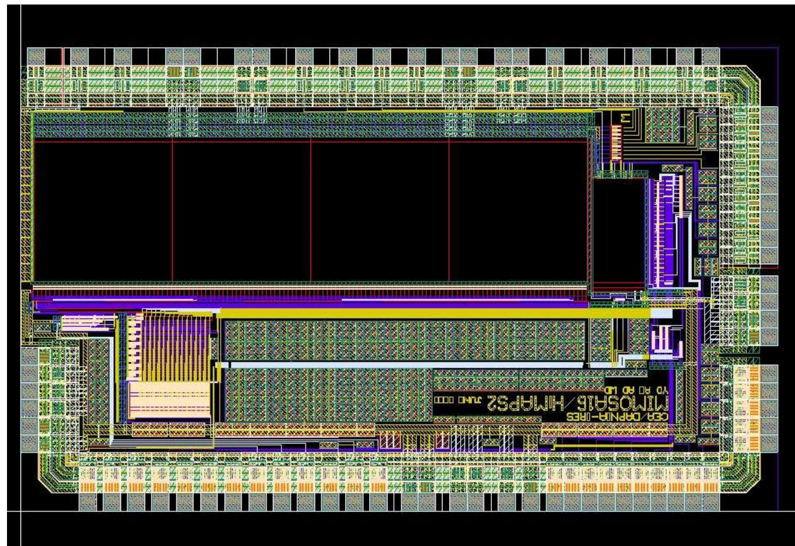



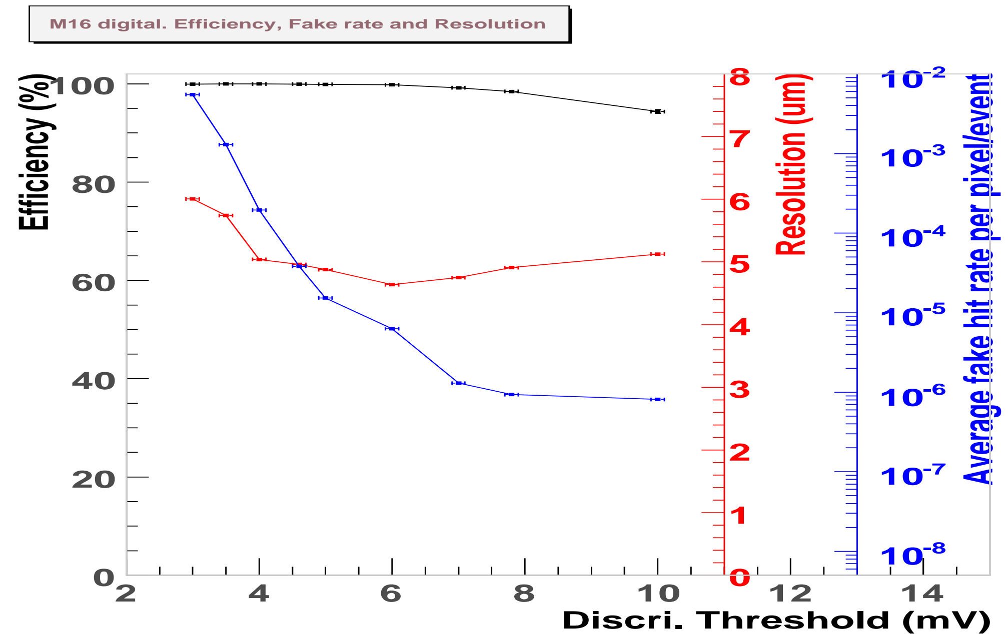



- **Integrated signal processing mandatory if r.o. freq. $\sim 10^4$ - $10^5$ frames/s** *(STAR-HFT, ILC-VD, CBM-MVD)*

- **Status of MIMOSA sensors** *(column // archi. with in-pixel CDS & mixed+digital $\mu$circuits at edge of sensitive area):*
  - *sensor with 24 // col. of 128 pixels (25 $\mu m$ pitch) ended with integ. discri. operationnal (tests at SPS)*



MIMOSA-16




- *Next steps $\longrightarrow$ integrate sparsification and ADC:*
  - *Intregrated $\emptyset$ $\longrightarrow$ real scale sensors for EUDET telescope (2008), STAR-HFT (2009), CBM-MVD (201X)*
  - *Integrated 4-5 bit ADC replacing discriminators $\longrightarrow$ prototype for ILC-VD (2008/09)*

- *Architecture difficult to adapt to r.o. freq. $>$ 100 kframes/s $\Rrightarrow$ call for more functionnalities inside pixel*

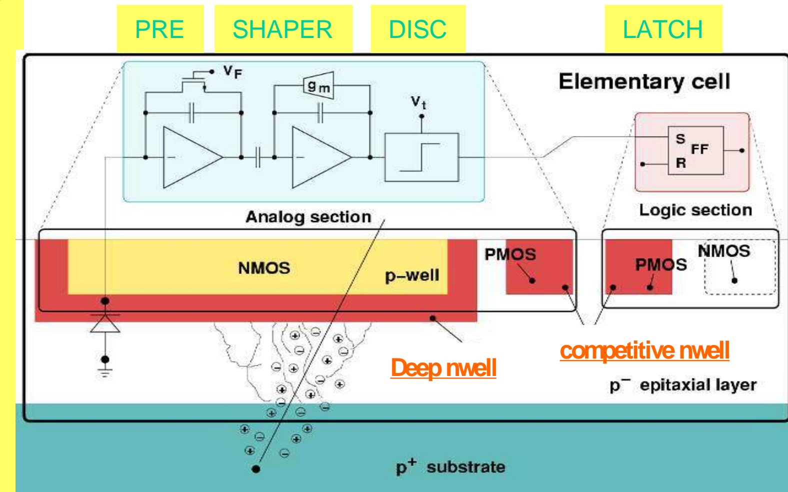
# Next Generation of CMOS Sensors (1/2)

## Deep NWell 130nm CMOS MAPS

- Rad-hard MAPS with data sparsification and high rate capability (self-triggering pixel design, in-pixel comparator, in-pixel time stamping and sparsification logic)
  - Deep N-Well (DNW) as collecting electrode
  - Classical pixel analog processing with charge-sensitive preamplifier

    Gain independent of the sensor capacitance collecting electrode can be extended and include NMOS of the analog section
  - Area of the "competitive" nwells housing PMOSFETs inside the pixel kept to a minimum. Fill factor = DNW/total n-well area ~90% in the prototype test structures
- **Pros:** With 100-nm scale CMOS, integration of advanced analog and digital functions at the pixel level (as in hybrid pixels), rad-hard electronics
- **Cons:** possible limitations in pixel pitch (go to more scaled CMOS, but higher cost, only binary readout) and detection efficiency (pixel layout critical, deep P-well option?)

SLIM5, ILC – INFN & Italian Universities




- 2004-2006: Proof of principle achieved with the first prototypes in a 130 nm triple well CMOS process
- 2007-2009: Full size MAPS sensors and detector modules, beam tests

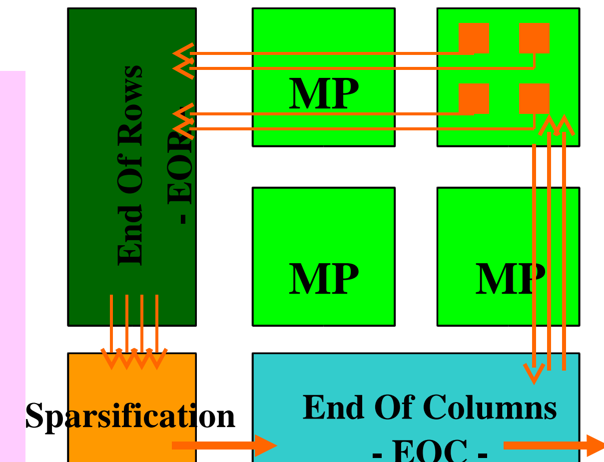
## Experimental results and future plans

- Performed successful tests of small (8x8) structures (full analog section and sequential binary readout, 50 μm and 25 μm pitch) with radiation sources and of small prototypes with sparsified data-driven readout architecture

- Next steps (4Q 2007- 1Q 2008): submission of larger devices (32x128, 256x256) with full time stamping and sparsification logic. Different readout architectures and pixel pitches are being optimized for operation at a Super B–Factory (large background, equivalent to a continuous beam operation) and at ILC.

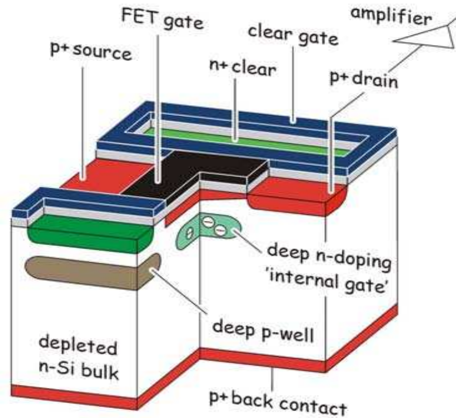
### Architecture for MAPS with LVL1 trigger capabilities

- Matrix subdivided in MacroPixel (MP=4x4) with point to point connection to the End Of Column
- Token pass logic scans for hits in the EOCs (stored list of hit MPs and relative timestamp) to start the redout of the corresponding MP.
- Pixel data from each read out MP are sent to the End Of Row and to the sparsification logic.
- Data output interface formats the output of the sparsification, associates the TS and sends data to output lines



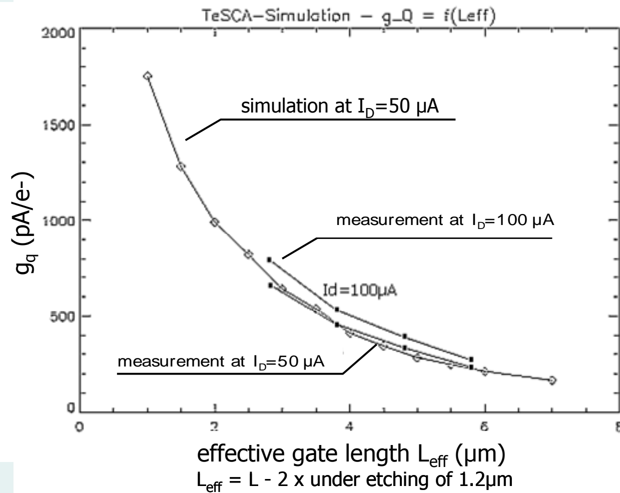

- Present R&D effort: improve S/N and threshold dispersion, reduce power dissipation, avoid digital-to-analog interferences (use shields), optimize sensor geometry for charge collection efficiency and pixel pitch for spatial resolution

# DEPFET Pixel Cell




Depleted P-channel FET

- fully depleted sensitive volume
  - fast signal rise time (~ns), small cluster szie
- internal amplification
  - large signal, even for thin devices
  - charge-to-current conversion:
    $g_q = dI_d/dq$ = 0.4 nA/electron (latest production)
    scales with gate length
- Charge collection in "off" state, read out on demand
  - potentially low power device




effective gate length $L_{eff}$ (µm)
$L_{eff}$ = L - 2 x under etching of 1.2µm

- special technology, currently only available at the MPI Semiconductor Laboratory (MPI HLL)
- future developments:
  - reduce feature size → improve $g_q$
  - improve technology for large wafer scale ($\Phi$=150mm) sensors
  - main applications:
    - X-ray Astronomy (XEUS, BepiColumbo, SimbolX)
    - candidate for the VXD at ILC and for the XFEL ….

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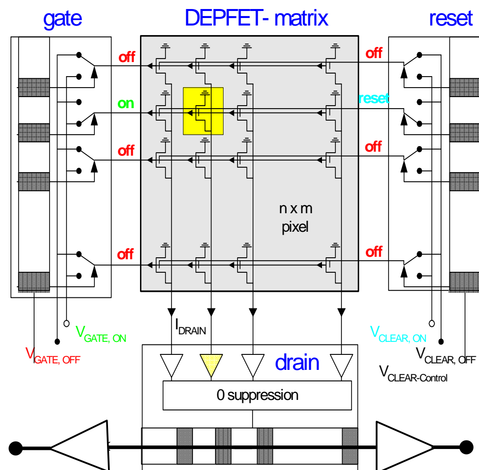
# DEPFET Array - different ways for read-out




**1. Row wise read-out ("rolling shutter") → Concept for the ILC VXD**

- select row with external gate, read current, clear DEPFET, read current again → the difference is the signal (row wise CDS)

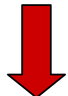
Advantage

- Low power consumption!
- No advanced interconnection technologies needed

Disadvantage

- two different types of auxiliary ASICs needed
- limited frame rate

Design goal at the ILC: 50ns row rate (sample-clear-sample)



**2. Hybrid-pixel-like approach: one amp. (and ADC?) per pixel**

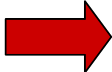
Advantage

- fast! (~ns), frame rate comparable with hybrid pixels

Disadvantage

- challenging interconnection between sensor and r/o chip
- high power consumption

Foreseen the focal plane at the XFEL



**3. Combination of those two**

- subdivide large arrays into smaller units
- challenging interconnection (→"3D")

→ find optimum for a specific application balancing the pros and cons

under consideration for the ILC VXD

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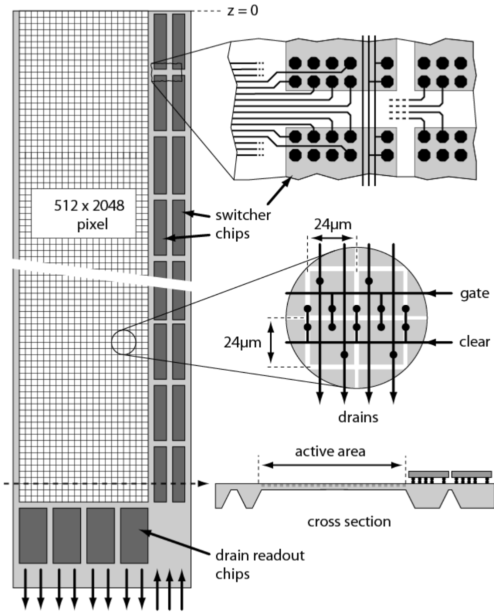
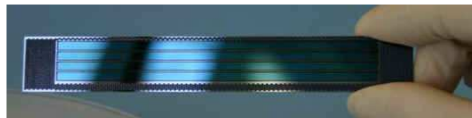
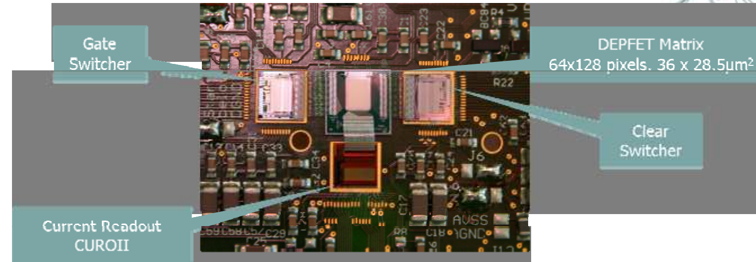
# ILC: Ladder Concept and Prototype System




ILC VXD first layer ladder



Thinning technology established!




**Prototype system achievements:**

- thick (!) DEPFETs (450µm), CURO and Switcher
- test beam @ CERN:
  - S/N≈110 @ 450 µm ←→ goal S/N ≈ 20-40 @ 50 µm
  - sample-clear-sample 320 ns ←→ goal 50 ns
  - s.p. res. 1.3 µm @ 450 µm ←→ goal ≈ 4 µm @ 50 µm
- radiation tolerance tested with single pixel structures up to 1 Mrad and ~$10^{12}$ $n_{eq}/cm^2$

**Next steps - very(!) briefly:**

- Develop new r/o ASIC with in-pixel ADC, improve noise and speed
- Production of thin wafer scale DEPFET arrays (2009)
- interconnection technology ("3D", fine pitch bump bonding..)

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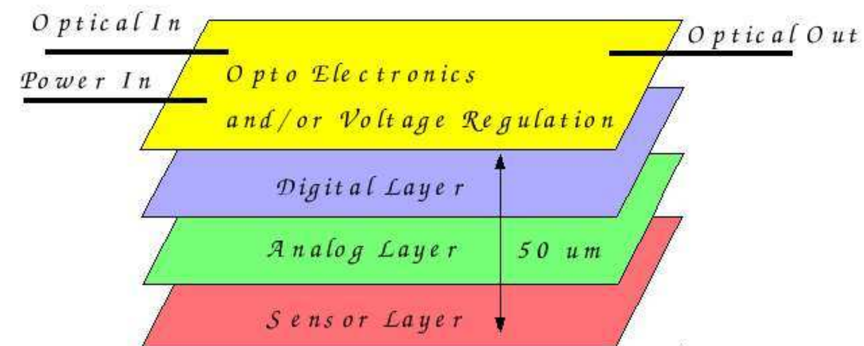
# Vertical Integration – 3D

- A 3D device is a chip comprised of 2 or more layers of semiconductor devices which have been thinned, bonded, and interconnected to form a monolithic circuit

- Advantages of 3D
  - Increased circuit density due to multiple tiers of electronics
  - Fully active sensor area
  - Independent control of substrate materials for each of the tiers
    - Process optimization for each layer
  - Ability to mate various technologies in a monolithic assembly




- Technology driven by industry
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power, crosstalk

- Critical issue are:
  - Layer thinning to < 10 µm
  - Precision alignment (< 1 µm)
  - Bonding of the layers
  - Through-wafer via formation

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# Vertical Integration – 3D

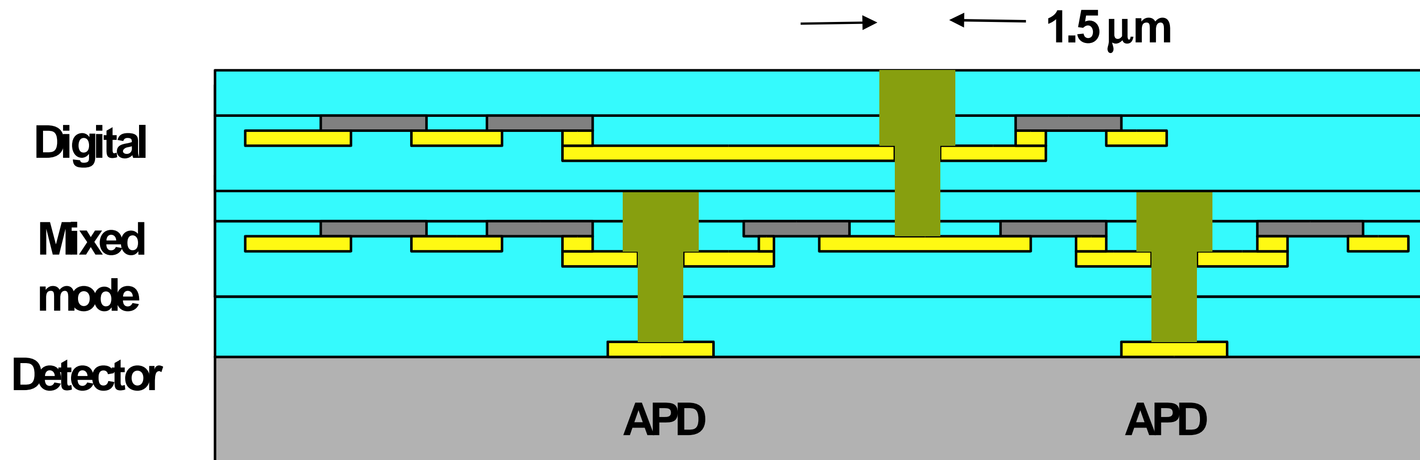
- Disadvantages of 3D
  - Relatively new technology with perhaps relatively long development cycle
  - Process is not cheap
  - Process not commercially available yet
  - Slow turn-around

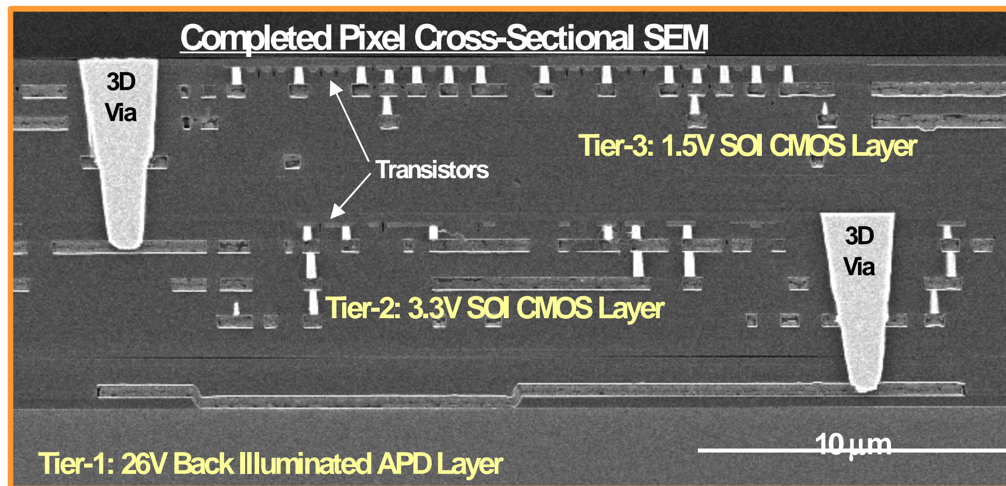
- Current efforts in 3D
  - To the best of our knowledge, so far only Fermilab pursuing the 3D technology
  - Fermilab has submitted a design for a 3D demonstrator chip for the ILC with MIT-Lincoln Laboratory on a 3D Multi-Project Wafer run with 3 tiers available:
    VIP (Vertical Integrated Pixel) – Chip
  - Design:
    - 20x20 $\mu m^2$ pixels
    - Layout for 64 x 64 array, but design for 1000 x 1000 array (readout speed etc.)
    - Analog and binary readout information
    - 5-bit time stamping of pixel hit
    - Data sparsification
  - Design submitted October 15, 2006
  - 3D chip due back at Fermilab at the end of October 2007
  - Unfortunately no test results available as of yet

*Slide 3*

# Proof of Principle

- MIT-LL has developed a laser radar imager based on three-dimensional integration of Geiger-mode avalanche photodiodes with two SOI timing-circuit layers

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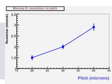
# Status and Plans

- VIP chip to be received any day; vigorous test program planned
  - Circuitry test of individual tiers
  - Vertical Interconnections
  - Functionality of chip
  - Irradiation measurements
- Chip to be bonded to "edgeless" silicon sensor, 20 micron pitch
  - Since the bonding with the sensor is not included in the 3D process, establishing reliable bonding currently bonding "System Test" of full structure of sensor plus readout chip

- Considering as next step a two-tier sensor+readout device
  - One wafer; on one side of the wafer is the detector on the other half of the wafer is the readout circuitry (mirror imaged)
    - Process would then only call for one bonding step
  - The wafer would be diced and folded over for 3D bonding
    - Estimated cost $400k - $500k




# SUMMARY

- **Numerous types of sensors and architectures are currently being developed for the ILC vertex detector:**
  $\hookrightarrow$ *many exploit ILC features* $\Rrightarrow$ *not suited to CLIC : difft beam time structure, occupancy, rad. level*

- **The most advanced sensor architectures developed for ILC-500 may not offer the necessary outreach for CLIC running conditions** *(e.g. CCDs, MIMOSA sensors, DEPFETs ?) :*
  $\hookrightarrow$ *R&D for CLIC VD should focus on 2nd generation techno. foreseen for ILC upgrades (e.g.* $\sqrt{s} \sim$ *1 TeV)*

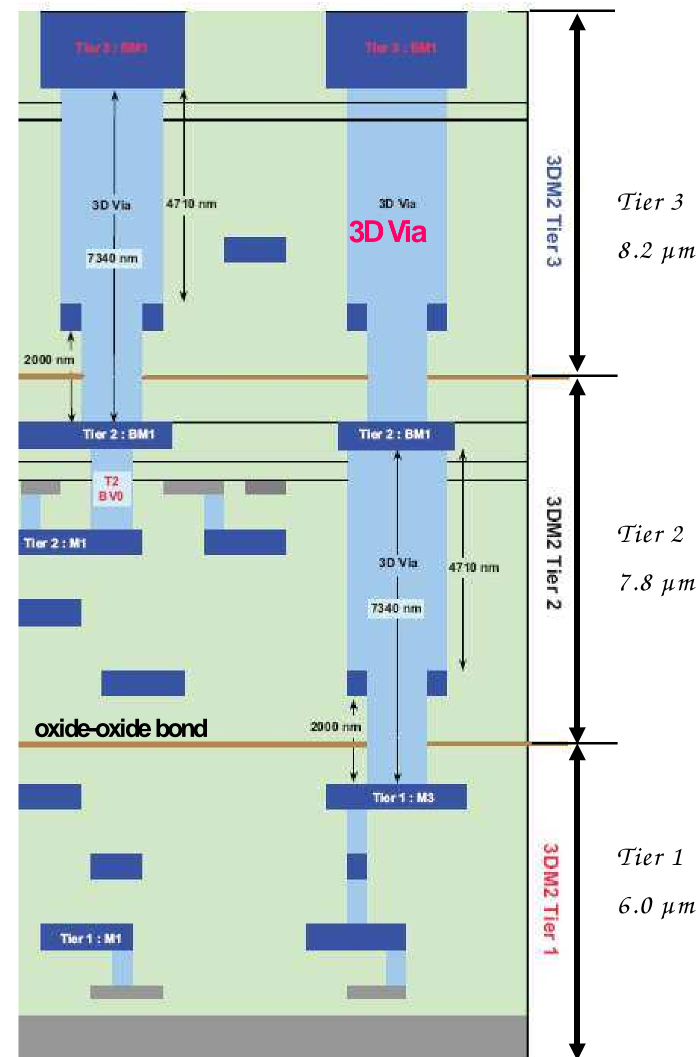
- **General trend : exploit 3D (vertical) Integration Technologies**
  $\hookrightarrow$ *SoI or existing technologies (CMOS sensors, DEPFETs) obviously going to take big advantage of 3DIT*

- **Common ILC - CLIC R&D ?**
  - *explore overlaping objectives* $\rightarrowtail$ *ex: fully integ. sensor architectures & (3D) fab. technologies*
  - *assess CLIC physics and running requirements : CLIC-500 (*$\sim$ *ILC-500 ?) vs CLIC-3000 (*$\gg$ *ILC-1000) ?*
  - *integration issues* $\equiv$ *natural ILC-CLIC field of synergy :*
    - *new (composite) materials*
    - $T_{room}$ *operation*
    - *data flow*
    - *3DIT (mech. support, ...)*

# BACK-UP SLIDES

# Development of a 3D Demonstrator Chip

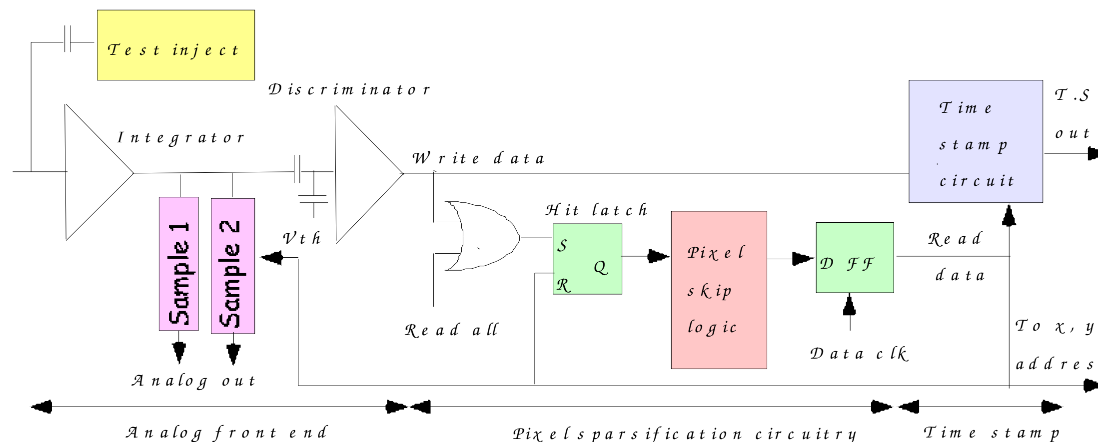
- MIT Lincoln Laboratories (MIT-LL) has developed the technology that enables 3D integration
  - Demonstrated the 3D technology through fabrication of imaging devices
  - Has infrastructure to allow for 3D Multi-Project Run fabrication
- We were invited to participate in the MIT-LL three-tier multi-project run
  - 3D design to be laid out in MIT-LL 0.18 μm SOI process
    - SOI provides additional advantages: BOX, full isolation, direct via formation, enhanced low-power operation
  - 3 levels of metal in each layer
- Submission deadline was Oct. 15, 2006
- Requested wafer space of ~ 2.5 x 2.5 mm²
- Pixel size 20 x 20 μm; 64 x 64 pixel array
- No integrated sensor
- Chip has been submitted !




Slide 6

# Architecture of Demonstrator Chip

- **Design:**
  - Provide analog and binary readout information
  - Time stamping of pixel hit for ILC environment
    - Divide bunch train into 32 time slices; each hit pixel can store one time stamp equivalent to 5 bits of time information
  - Sparsification to reduce data rate
    - Use token passing scheme with look-ahead to reduce data output
      - During acquisition, a hit sets a latch
      - Sparse readout performed row by row with x- and y-address stored at end of row and column
  - Chip divided into 3 tiers
    - Pixels as small as possible but with significant functionality.
    - Design for 1000 x 1000 array but layout only for 64 x 64 array.




**Schematic pixel cell block diagram**

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# Pixel Readout Scheme

- Pixel being read points to the x address and y address stored on the perimeter.
- At same time, time stamp information and analog pulse height is read out
- During pixel readout, token scans ahead for the next hit pixel (200 ps/cell)

Assume 1000 x 1000 array
X and Y addresses are 10 bits each

Digital Data Mux X,Y,Time
X
Y
Time
Serial Data out (30 bits/hit)
Y address bus
Analog outputs
Start Readout Token
10
1
5
X=1
T1 buf
X=2
T2 buf
X=1000
T1
T2
cell 1:1
cell 2:1
cell 1000:1
Y=1
Token to row Y=2
cell 1:2
cell 2:2
cell 1000:2
Y=2
Token to row Y=3
cell 1:3
cell 2:3
cell 1000:3
Y=3

Note: All the Y address registers can be replaced by one counter that is incremented by the last column token.

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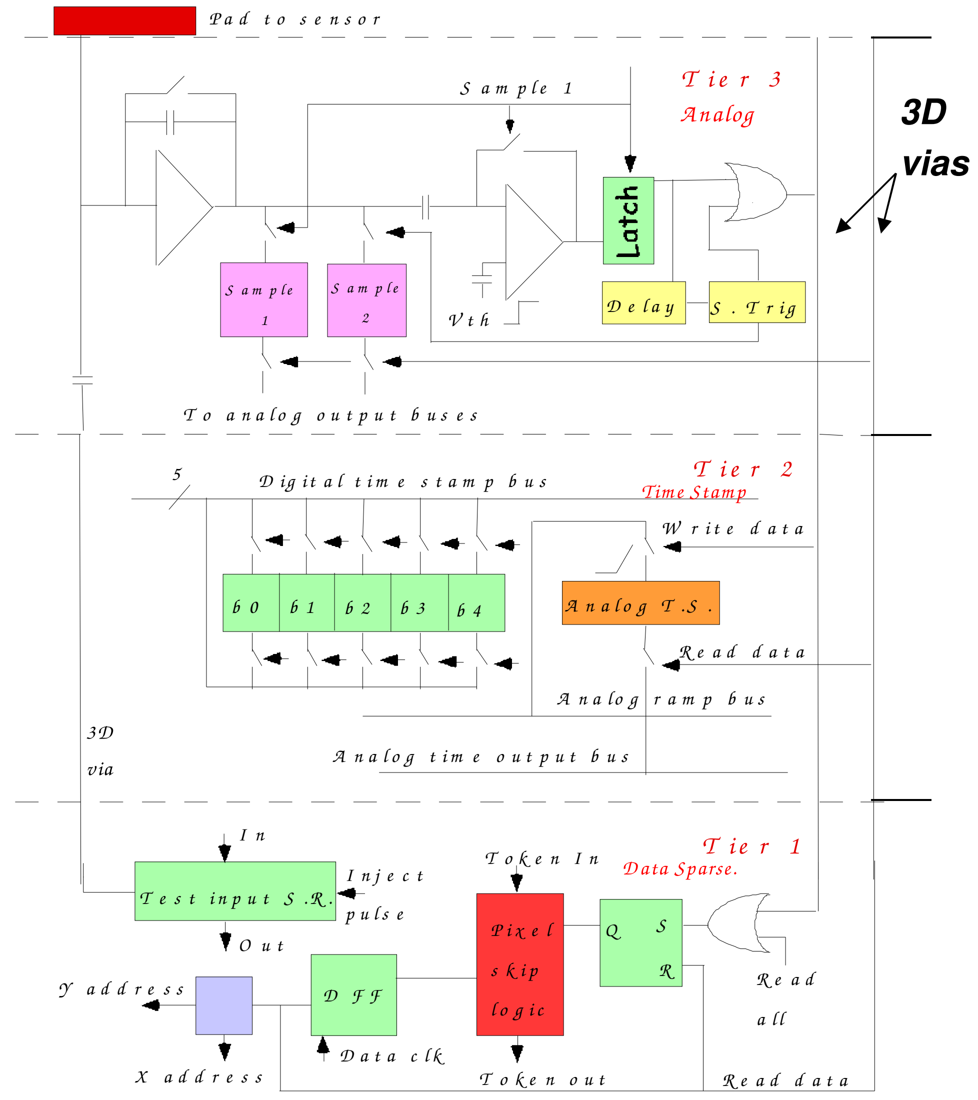
# 3D Three Tier Pixel Layout

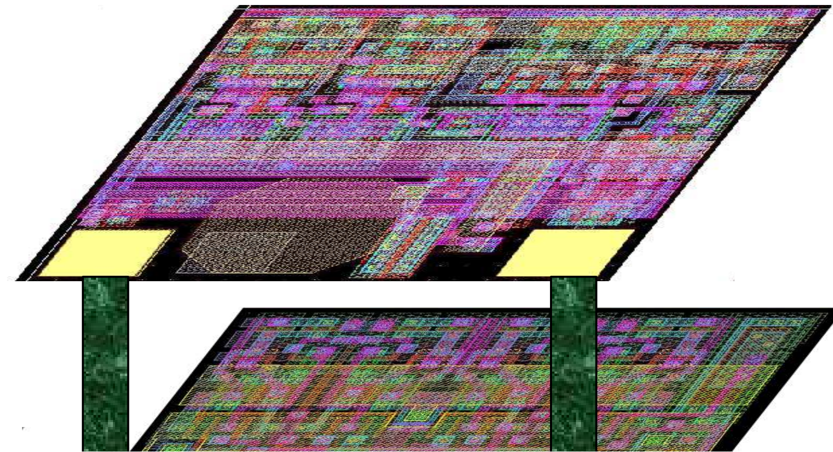
- Readout speed for an ILC environment
- Assume 1k x 1k array with 20 x 20 $\mu m^2$ pixels
  - First pixel in each row always read out
    - Adds 1000 cells, small increase in data volume
  - Time to scan 1 row:
    200 ps x 1000 = 200 ns
  - Time to readout cell
    30 bits x 20 ns/bit = 600 ns
  - Plenty of time to find next hit pixel during readout
- Assume maximum number of hits/chip of 250 hits/mm²
  - For a 1000 x 1000 array of 20 $\mu$m pixels, 100k hits/chip
  - For 50 MHz readout clock and 30 bits/hit, readout time:
    100,000 hits x 30 bits/hit x
    20 ns/bit = 60 msec.

- Readout time is far less than the ILC allowed 200 msec. Thus the readout clock can be even slower or several chips can be put on the same bus. Readout time is even less for smaller chips

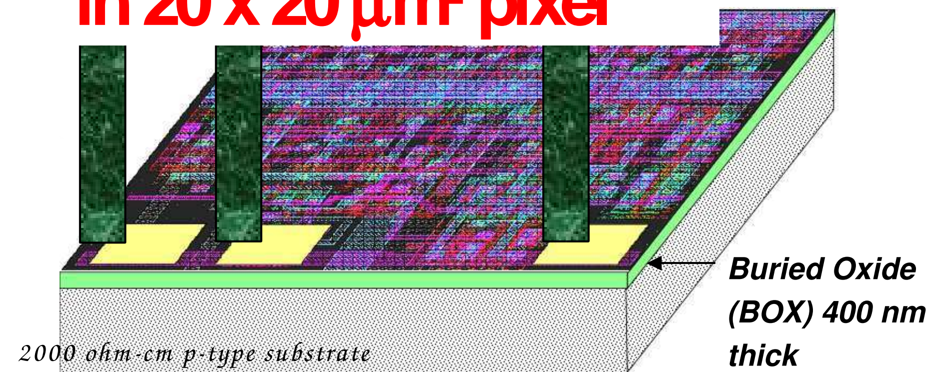


# 3D Stack

- Form 2 vias, 1.5 x 7.3 µm, through tier 3 to tier 2
- Tier 3
  - Integrator, DCS plus readout
  - Discriminator
  - 2 vias
  - 38 transistors
- Bond Tier 3 to Tier 2
- Form 3 vias, 1.5 x 7.3 µm, through Tier 2 to Tier 1
- Tier 2
  - 5 bit digital time stamp
  - Analog time stamp (ts)
    - Either analog or digital ts
  - 3 vias
  - 72 transistors
- Bond Tier 2 to Tier 1
- Tier 1
  - OR for READ ALL cells
  - Pixel skip logic for token passing
  - 3 vias
  - 65 transistors



175 Transistors in 20 x 20 $\mu m^2$ pixel

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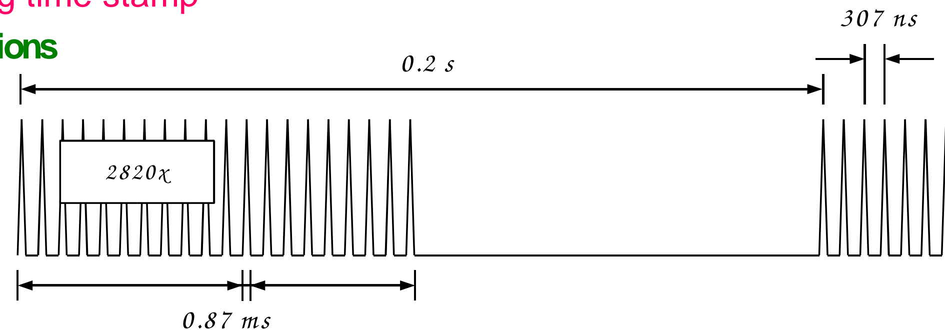
# ILC Pixel Detectors

- ILC requirements push the limits for low mass, low power and high resolution
  - Event characteristics require excellent b-identification capabilities through secondary and tertiary vertex finding and jet charge measurement
  - High occupancy environment due to machine and IP backgrounds
- Vertex detector requirements
  - Very low mass: 0.1% $X_0$ per layer (equivalent of 100 μm of Si)
    - Low mass requires no active cooling, hence low power
  - High resolution: impact parameter resolution of ~ 5 μm
    - Requires smaller pixels which increases the readout circuit density
  - Good and robust pattern recognition, integrated design
    - Low occupancies, bunch crossing time stamp
  - Modest radiation tolerance for ILC applications




- ILC beam structure
  - 2820 crossings in a 1 ms bunch train
  - 5 bunch trains per second
- ILC Maximum hit occupancy
  - Assumed to be 0.03 particles/crossing/mm²
  - Assume 3 pixels hit/particle (obviously this depends somewhat on pixel size, hit location, and charge spreading)
  - Hit rate = 0.03 part./bx/mm² x 3 hits/part. x 2820 bx/train gives 252 hits/train/mm²

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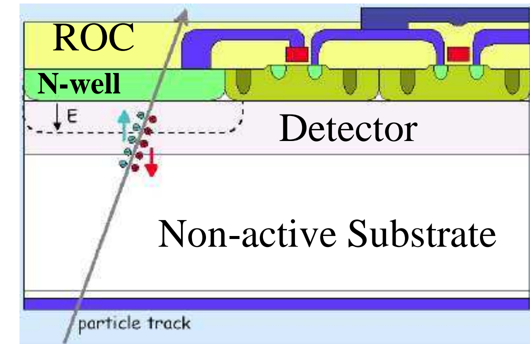
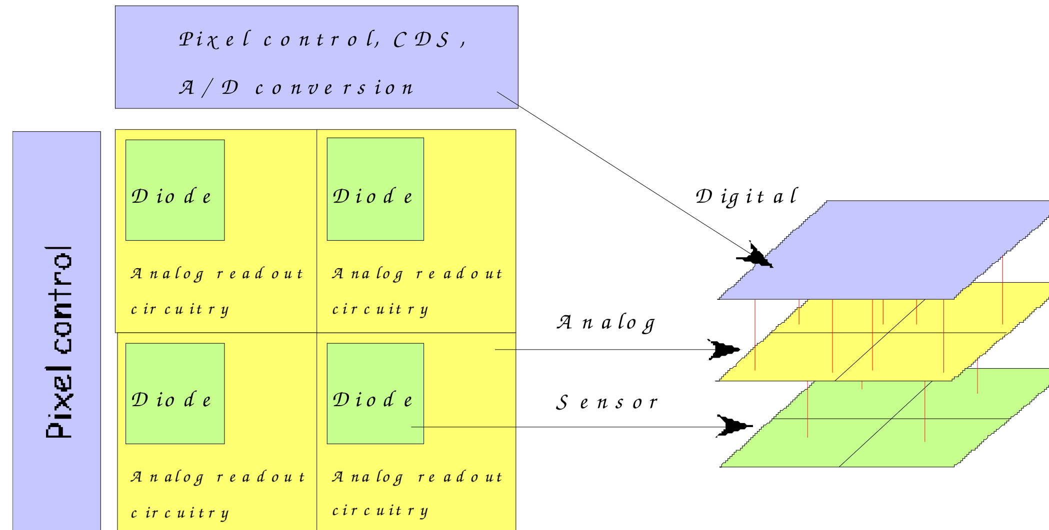
# 3D versus Monolithic Active Pixels

- A MAPS device is a silicon structure where the detector and the primary readout electronics are all processed on the same substrate
- Advantages of 3D devices:
  - Significantly higher functionality in a pixel cell using current feature sizes
  - NMOS and PMOS transistors
  - Processing of each layer can be optimized
  - 100% active, minimal perimeter area requirements




MAPS Principle




Conventional MAPS 4 Pixel Layout

3D 4 Pixel Layout

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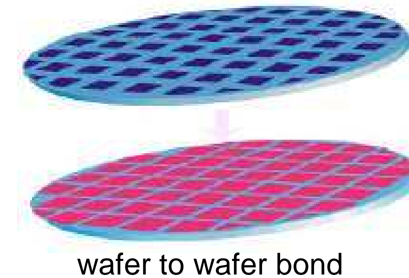
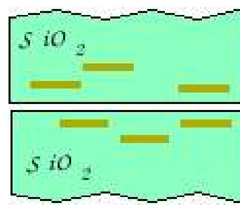
# 3D Process

- Wafer thinning
  - Thinning of individual tiers may be done before or after bonding to another tier.
  - Thinning is generally done by grinding and lapping followed by etching (plasma or wet) and CMP (chemical mechanical polishing)

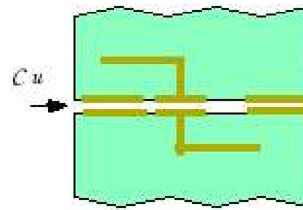


wafer to wafer bond

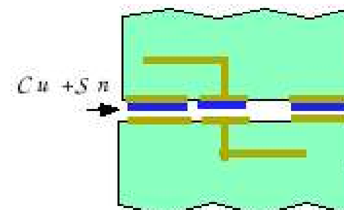
- Wafer bonding
  - Bonding approach
    - wafer to wafer bonding
    - die to wafer bonding
  - Bonding techniques



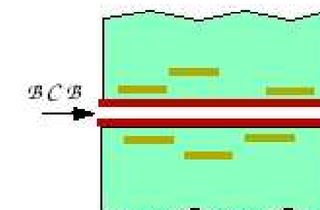

Direct silicon bonding




Copper to copper bonding




Copper-tin eutectic bonding




Adhesive (BCB) bonding

- Electrical connectivity
  - Pad contacts in bonding process
  - Through wafer via formation

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