## +

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SRS development: Hans Muller, Sorin





Marcin Byszewski On behalf of the MAMMA collaboration.

## Running Micromegas in ATLAS: status update of DAQ integration and plans

2/10/2012 RD51 Stony Brook



### **Compare data from the test chambers with ATLAS data**

(take these data with no impact on ATLAS data taking)

- 1. Stand-alone, random trigger (until September 2012)
  - Convenient, Track matching not possible
- 2. Trigger from ATLAS, data separate ('parasitic')
  - Offline synchronisation
- 3. Fully integrated with TDAQ in ATLAS partition
  - Most of our event fragments empty

A lot of discussions and support from CTP / TDAQ / run coordination / Sysadmins. Thank you.

## Micromegas test chambers

### Installed Feb 2012, read out in stand-alone random trigger mode

Test chambers description and readout in stand alone mode see Joerg Wotschack's presentation in Run Weekly 24/7/2012 <u>https://indico.cern.ch/conferenceDisplay.py?confId=194946</u>

#### MBTS, side A

- Front of the LAr calorimeter cryo
  - $r \approx 1 m$
  - z = 3.5 m
- One 9x4.5 cm<sup>2</sup>
  - X-V (2 readout gas gaps)



#### Small Wheel, sec. 9, side A, CSC

- r = 1.7 -1.8 m
- Four 9x9 cm<sup>2</sup> chambers
  - X, Y, XY, XUV
  - Only three read out
    - 1 FEC limit
    - Power supply limits and SRU firmware





# MBT chambers (LAr ecal)



## MMs on Small Wheel II





R16, chamber with 2D readout active area: 9 x 9 cm<sup>2</sup>

## +Some typical events displays



J. Wotschack (CERN)

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### + Rates / Occupancy / data size

#### **MBTO**

- Rates:
  - $\approx 20 \text{ kHz/cm}^2 @ \text{L}=10^{33} \text{ cm}^{-2} \text{ s}^{-1}$
  - 7 strips (16 time bins)
- 10kHz readout
  - (100kHz \* 0.1 due to slow readout)
- Up to 10MB/s
  - by varying time window and data reduction mode (36GB/h)
- Total data:

for 10 weeks, 5 days, 10h runs 17 TB of LV1 data

### SW

#### Rate:

- $30 \text{ Hz/cm}^2 \textcircled{0}{L} = 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$
- Majority (90%) of events with uncorrelated hits

# + Current readout: ½ ROD

TECTOR ith 2 hybrids two Arvis theads one Hont cable two Arvis theads two Arvis theads two Arvis theads one Hont cable pigitizer card up to 8 Hont cables

- SRS based ROD:
  - RD51's SRS system <u>https://espace.cern.ch/rd51-wg5/srs/default.aspx</u>
    - APV25 chips (CMS Si tracker) (16+4)
    - HDMI cables (10)
    - SRS FEC (ADC, Ethernet)
- Data to a DAQ PC in USA15



### +SRS – based Readout

- Front end electronics:
  - APV25 chips (CMS tracker, no other choice)
  - HDMI cables (LV, data)
- **ROD** in UX15:
  - SRS FEC digitization, peak finding, zero suppression
  - **DTC** link to SRU
  - SRU-EB, TTC, LV1, DCS, SLINK
- **USA15** 
  - CSC TTC, DATA, DTC fibres
  - **Run Control Application (on RC PC)**

ROD

ROS 

UX 15

DCS(ACR Muon Desk, CSC infrastructure) 

FEC

(ADC/Eth

ernet)



Ctrl

SLINK

SRU

**USA** 15



M. Byszewski (CERN)

APV25

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### + Configuration

- Not in ATLAS partition
  - There is no way of getting LV2/EF information to our ROS (event selection)
  - MM partition fully described in TDAQ OKS database
  - Reading out 10% of LV1 triggers (slow APV data transfer)
  - Pre-selection on SRU possible
    - Send only events with APV data
    - Possibly select on FEC event size
  - Store all read out data
- Switch to SW-only readout
- We could switch back to TDAQ-compliance mode, if we want
  - into fully integrated mode
  - and serve all LV1 if in ATLAS partition



### + Run Modes



- **ATLAS LV1, 10%**
- Data to SLink-ROS-RC PC-HDD
- Offline synchronisation of LV1
- Throttled data transfer to storage (Castor)
- All APV / SW-only runs
- Calibration
  - Off-run
  - Internal / CSC triggers
  - On FEC measurement of ZS pedestals
  - RC PC storage of pedestals (read from FEC)
- APV calibration (rare)
  - Internal triggers
  - ZS in bypass mode
  - SRU in bypass mode to Ethernet port
  - Display / Verify raw APV frames



### + Run Modes



#### Physics

- ATLAS LV1, 10%
- Data to SLink-ROS-RC PC-HDD
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#### Calibration

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- Internal / CSC triggers
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### + Run Modes



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- ATLAS LV1, 10%
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#### Calibration

- Off-run
- Internal / CSC triggers
- On FEC measurement of ZS pedestals
- RC PC storage of pedestals (read from FEC)
- APV calibration (rare runs)
  - Internal triggers
  - FEC ZS in bypass mode (RAW data of one APV)
  - SRU in bypass mode (to Ethernet port)
  - Display / Verify raw APV frames

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# Offline synchronisation

- Before data analysis
- Save all RAW events
  - ATLAS synchronisation at our convenience
  - Max of 16TB of data (SW+MBTS) for 10 weeks of 10h ATLAS runs daily (SW+ MBT0)
  - We will get that space
  - Throttled speed of output to storage will limit data taking
- Dedicated SW-only runs
  - This data will by compared to ATLAS data





- ATLAS compliant ROD based on SRS
  - But run in a different mode
- Readout synchronised with ATLAS triggers
  - There is no way of getting LV2/EF information from TDAQ
- I FEC (MBT0 + SW chambers)
  - Power supply
  - To be switched to SW only
- RC-PC with storage space is being prepared
  - Time to debug

# Next steps: to data analysis

- Run planning to be made (9 weeks)
  - MBT0/SW runs
  - dedicated SW runs (re-cabling 4<sup>th</sup> chamber)
- DAQ commissioning
  - Verify APV settings (raw data)
  - Verify FEC ZS pedestals
  - Stability (not to disturb the Muon shifter's sleep)
  - Write data decoder (ATLAS -> ROOT for EventBrowser)
- Data preparation / Offline Synchronisation
  - Select based on Timestamp + LV1ID (ATLAS and MM)
  - Select events with CSC tracks
  - ATHENA jobs
  - mmDAQ root files feed to RECOmm
- Data analysis
- (Write Manual / Documentation)

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Thank you



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# Micromegas principle

### Parallel-plate chamber

Conversion & drift region (typically a few mm) with moderate electric field of 100–1000 V/cm

Amplification in a narrow (128  $\mu$ m) gap with high electrical field (40–50 kV/cm)

- With drift velocities of 5 cm/µs (or 20 ns/mm) electrons need 100 ns drift time to reach the mesh (for a 5 mm gap)
- By measuring the arrival time of the signals a MM functions like a TPC => Track vectors for inclined tracks





#### SRU

- Virtex 6,
- TTCrx chip,
- 4 SFP ports
- 40 DTC links
- EB, and TTC LVL1 Accept treatment
  - Process first, buffer others
- TTC
  - SRU uses onboard TTCrx chip to receive BC clock, L1A, ECR, BCR and trigger type
  - Connect to CSC TTC partition with unique TTC address
  - Additional user-programmable offset value for BCID
- S-LINK
  - HOLA emulator on Virtex 6 board



Configuration (1): TDAQ

- 1) Fully integrated solution required much more work (MM and TDAQ) without clear advantage for data analysis.
- 2) Parasitic mode
  - LVL1A from CSC TTC crate
  - Sub-detector ID : RPC 0x65 (side A), data channel 0xFF (nonexistent, ignored by decoder)
  - Separate MM partition for ROS local storage
    - Offline synchronization with ATLAS data
- 3) Parasitic with RCD in ATLAS partition
  - Send UDP packages to our ROD (e.g., to set RunNumber)
  - (Always returns with success)

ATL RC RC PC

ROS

# **SLINK** implementation

(M. Della Volpe, R. Giordano, V. Izzo, S. Perrella)

 Event data are transmitted using SLINK to the data aquisition system (formerly HOLA based)

 No need of a seperate HOLA daughter card, due to the implementation of the serialisation logic in the Virtex6 FPGA (GTX transceiver)

 Data transfer to a standard ROS PC tested successfully with both FILAR and ROBIN pci cards. Valid ATLAS frames are received.



Andre Zibell, LMU Munich

# **DTC Links**

(A. Martinez)

- Transmit TTC clock to FEC Cards
- Foreward triggers with fixed latency, synchronous to the clock
- Carry Slow Control commands to FEC and APV chip, ...
- Return detector event data at 640 Mbit/s
- Hot plug ability and automatic resynchronisation

Andre Zibell, LMU Munich