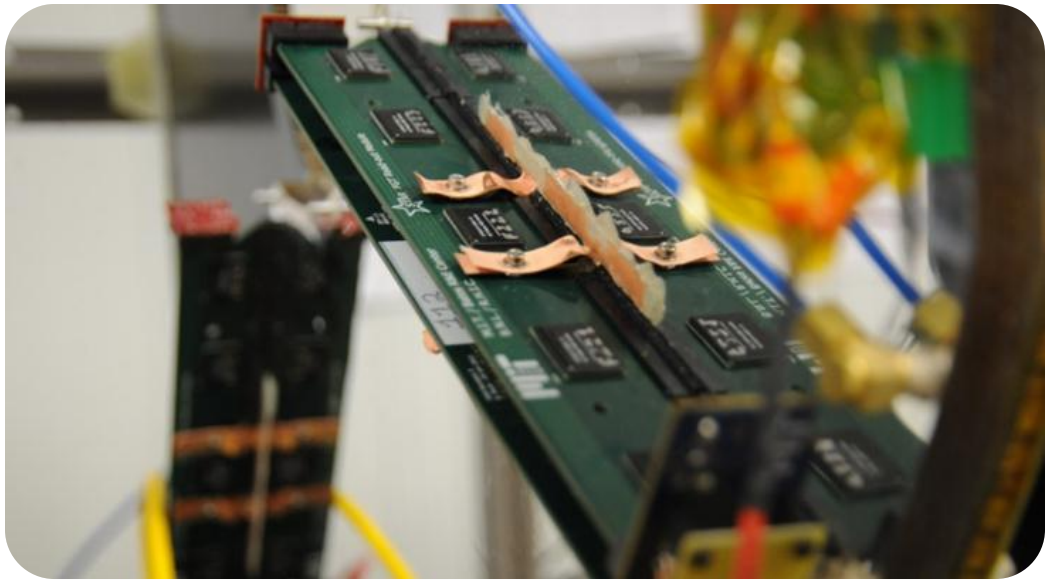
BGA packaging of APV-25 Chip



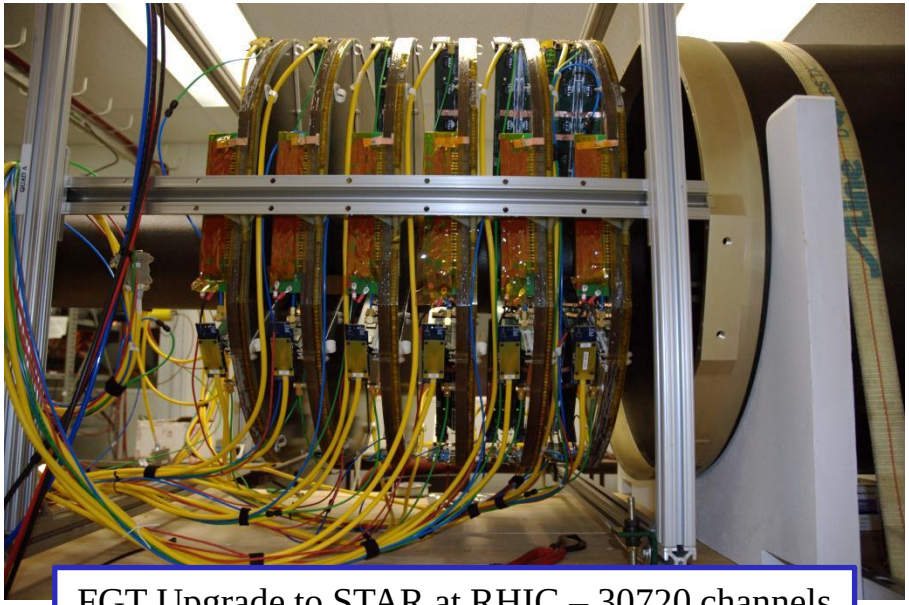
Benjamin Buck

bbuck@mit.edu

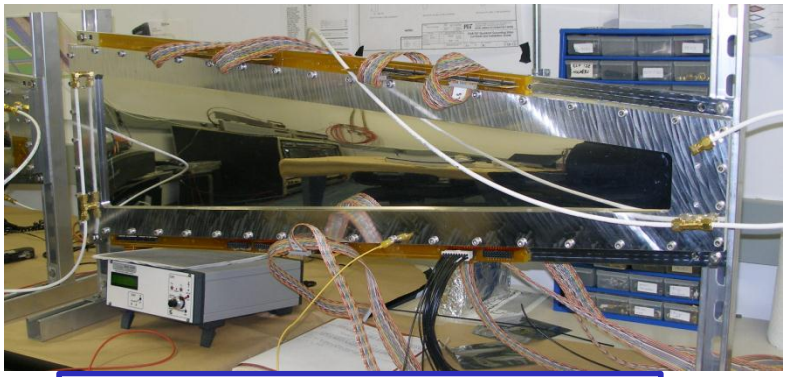
MIT Bates Research and Engineering Center

2 October 2012

Background



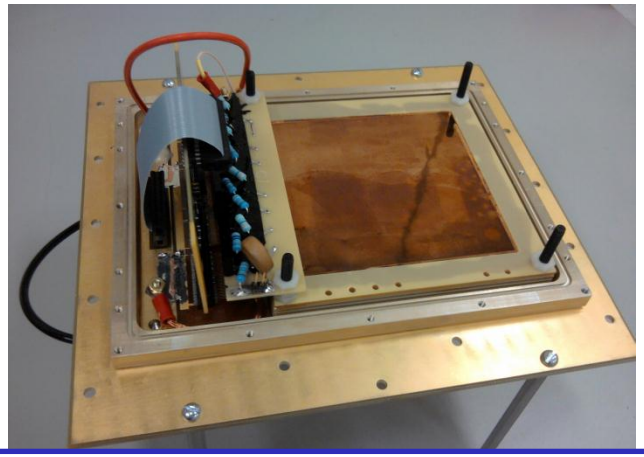
FGT Upgrade to STAR at RHIC – 30720 channels



GEM Tracker for OLYMPUS at DESY – 2984 channels

At Bates R&E center we provide engineering support for various projects.

For several projects there was a need to develop a front end card for triple-GEM readout

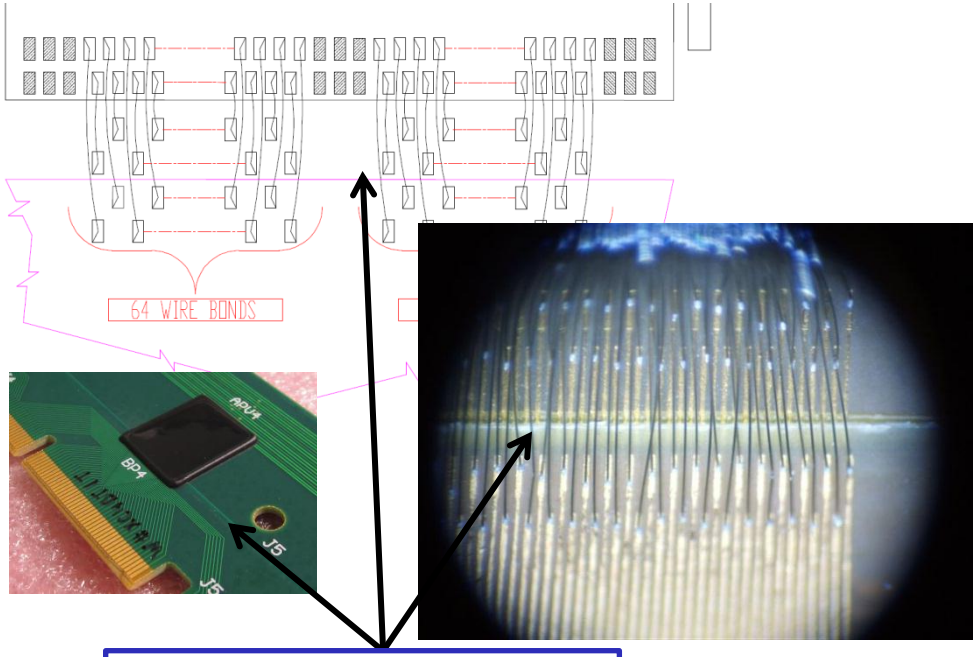


GMT Upgrade to STAR at RHIC – 2048 channels

Chip-on-Board

First FGT Readout Module prototype – APV bonded directly to circuit card

- FGT planned on APV25-S1, had purchased die sufficient for the project.
- Prototype readout boards were expensive and complicated – “Cavity Board” had a step in the design, wire bondable gold finish
- Assembly was also expensive and complicated, involving wire bonding and encapsulation plus hand soldering of passive components
- Assembly permitted no rework



Two boards laminated together

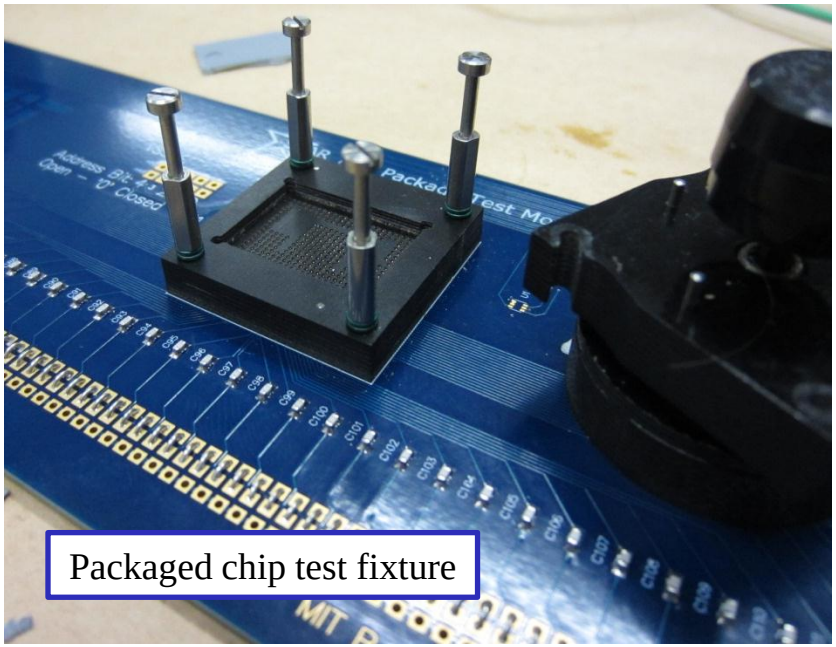
Packaged Chips

Advantages:

- Reduces cost and complexity of front end card manufacturing and assembly
- Permits re-work after assembly
- Significant NREs associated with the design of the package made this costly for FGT's first run, subsequent runs were much more cost effective
- Permits testing die directly before installing on boards
- Other projects can jump on the band-wagon

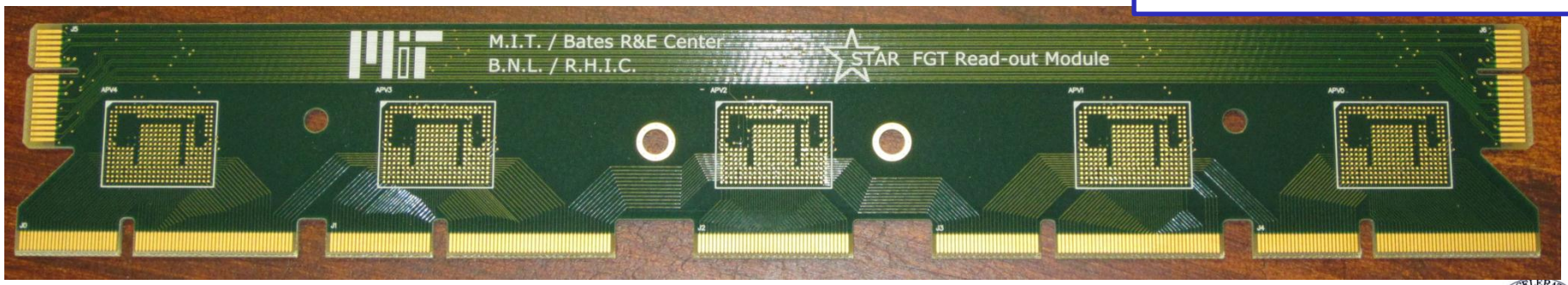
Disadvantages

- More mass
- More capacitance
- Higher costs if re-design is necessary
- More interfaces = more potential for problems



Packaged chip test fixture

FGT Production Readout Board



Cost Comparison

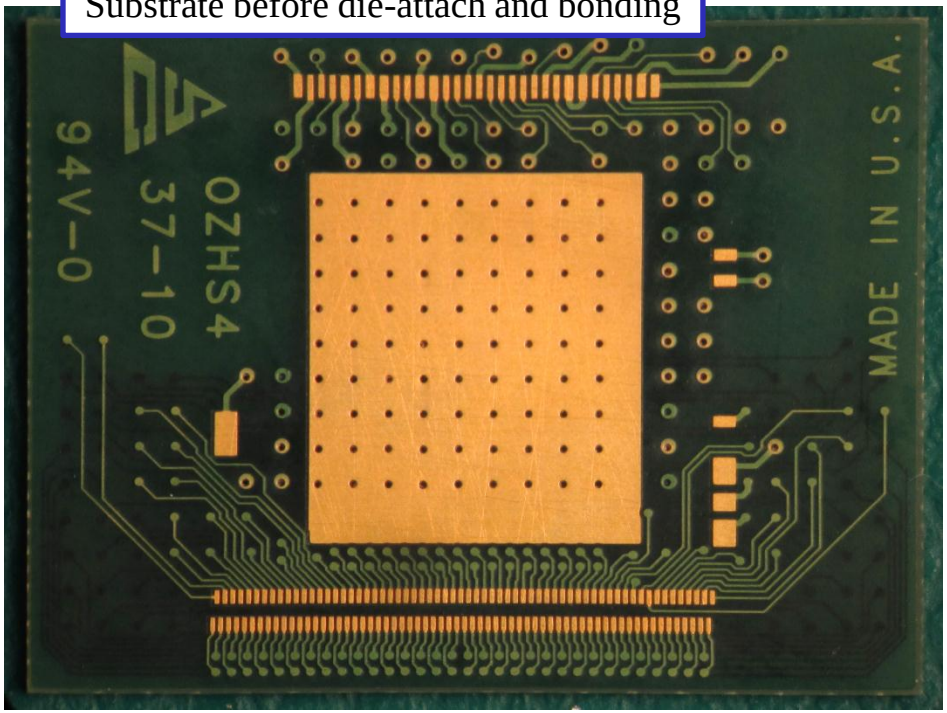
Cost Estimate for producing Chip on Board design

Cost / Unit	NRE	Item	Manufacturer
$ 650.00	$ 1,300.00	Boards	Compunetics
$ 101.00	$ -	Bonding	Corwil
$ 51.00	$ -	Add'l Assembly estimate	Proxy
	$ 65,460.00	**80 Boards**	

Cost Estimate for producing Packaged Chip design

Cost / Unit	NRE	Item	Manufacturer
$ -	$ 16,000.00	BGA Design	Compunetics
$ 30.85	$ 2,500.00	Substrates (600 units)	Sierra
$ 46.31	$ 2,500.00	Substrates (185 units)	Sierra
$ -	$ 5,820.00	Packaging (580 units)	Corwil
$ -	$ 5,085.00	Packaging (101-200 units)	Corwil
$ 68.29	$ 355.00	Boards	Sierra
$ -	$ 1,480.00	Test Socket	Emulation Technologies
	$ 43,958.20	**Total for 80 Boards**	
	$ 36,377.50	**Total for 35 Boards**	

APV Package Design

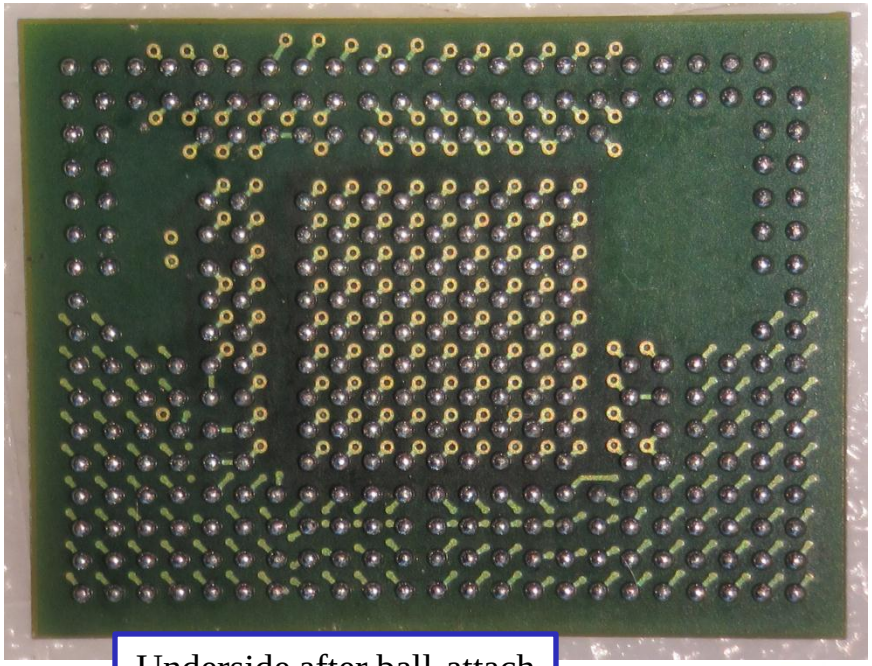


Substrate before die-attach and bonding

- All slow-controls, clock, trigger, chip outputs one edge of BGA
- All detector inputs on opposite edge of BGA no more than 4 balls deep from the edge (2 layer fanout)
- Power connections located on interior of grid
- 9x9 grid of balls directly under die with 9x9 grid of vias connecting to die attach pad for excellent thermal conduction

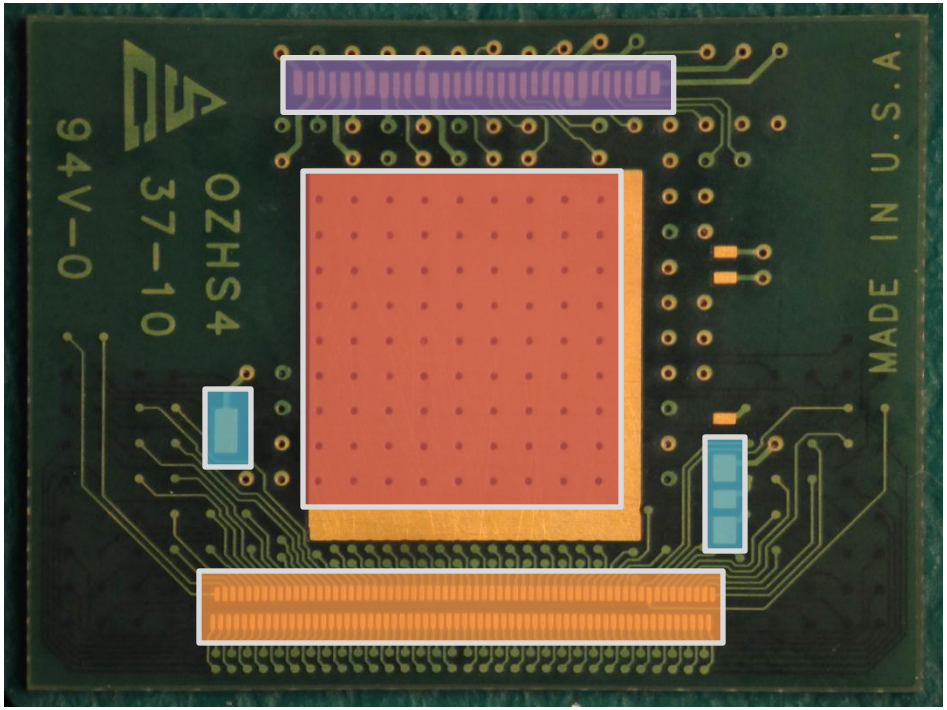
- 15mm x 20mm x 1.69mm
- 0.988g
- 17x23 ball grid, 0.8mm pitch, 0.45mm diameter solder ball (315 balls total)
- 4 Layers, 2/2design rules

BGA Mounted to Board

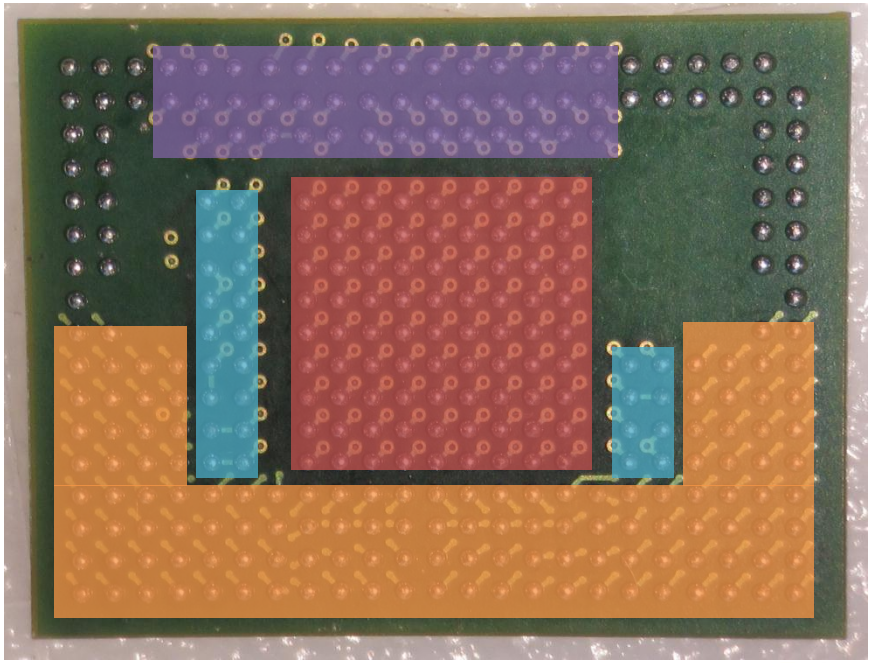


Underside after ball-attach

APV Package Design



- All slow-controls, clock, trigger, chip outputs one edge of BGA
- All detector inputs on opposite edge of BGA no more than 4 balls deep from the edge (2 layer fanout)
- Power connections located on interior of grid
- 9x9 grid of balls directly under die with 9x9 grid of vias connecting to die attach pad for excellent thermal conduction



- 15mm x 20mm x 1.69mm
- 0.988g
- 17x23 ball grid, 0.8mm pitch, 0.45mm diameter solder ball (315 balls total)
- 4 Layers, 2/2 design rules

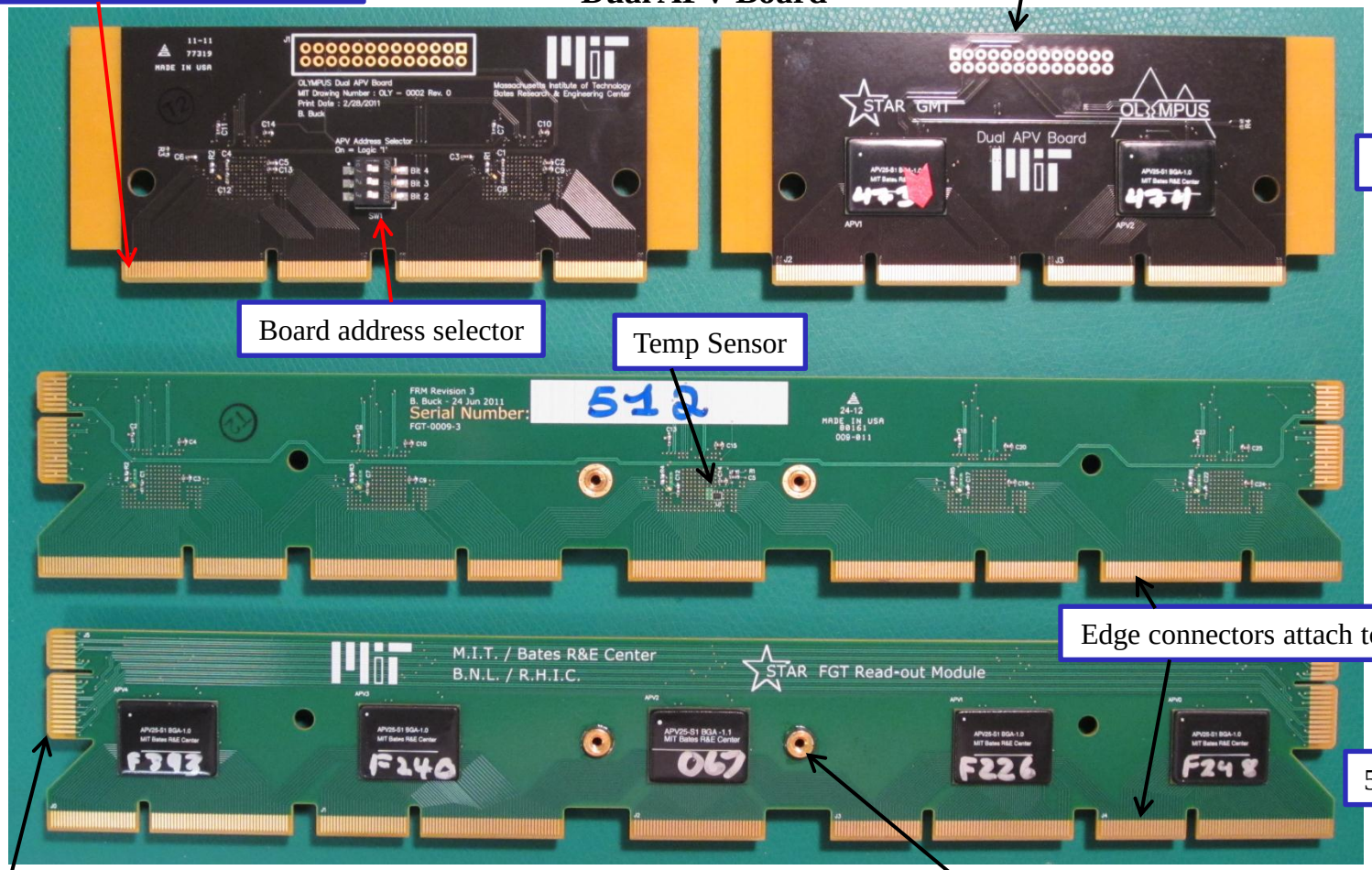
BGA Mounted to Board

Board layout

Edge connectors attach to signal pads and provide grounding (24 ground pins / bd)

Standard 100mil pitch square post for power and data

Dual APV Board



2 APV Chips

Edge connectors attach to signal pads

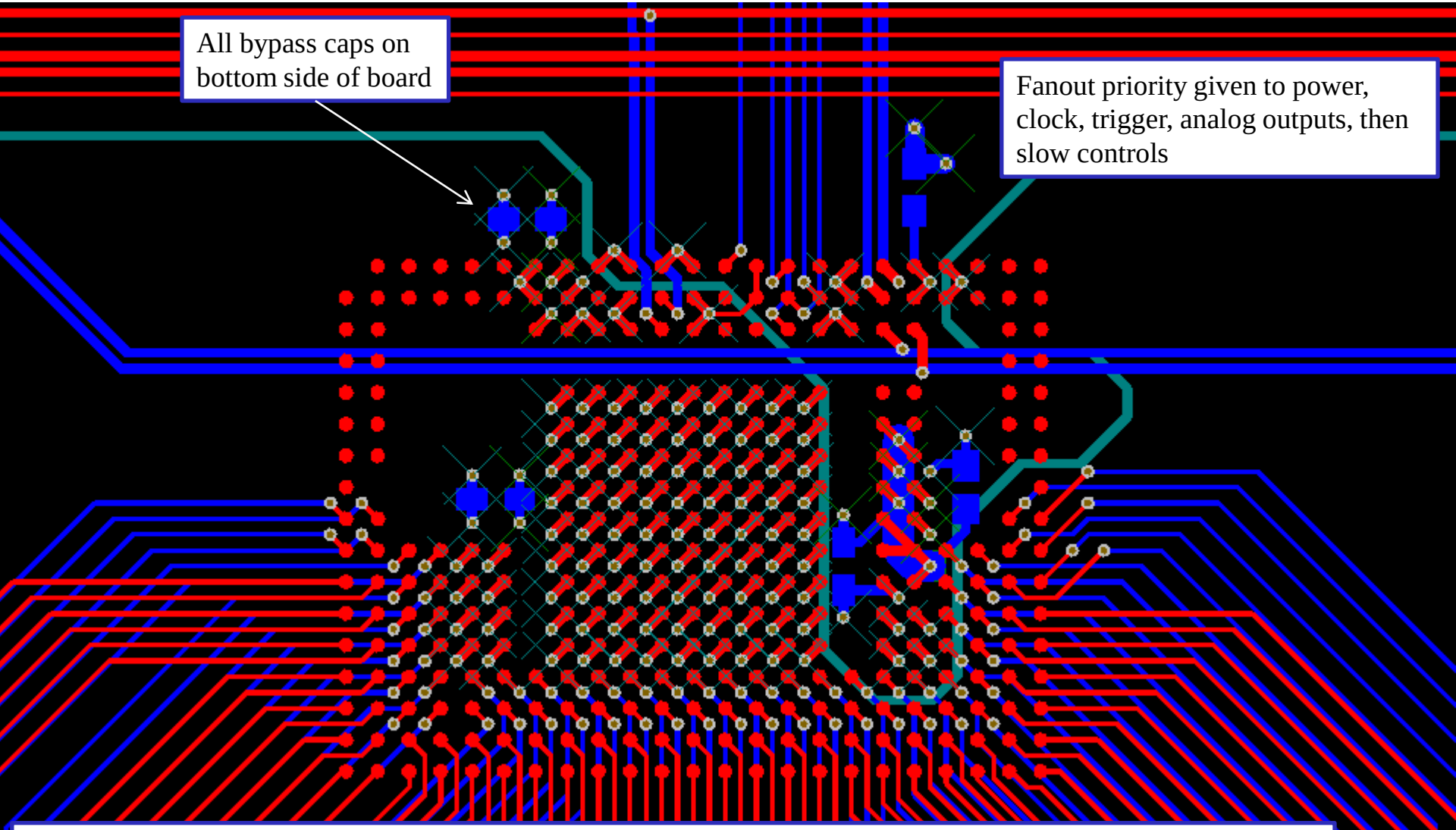
5 APV Chips

FGT Readout Module

Symmetric connectors on edge for power and data connection. Allows two boards to connect in parallel.

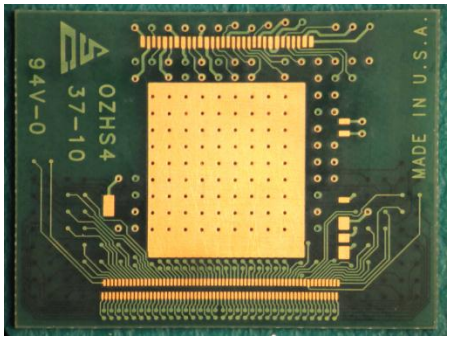
Detector ground provided by copper foil screwed in here

BGA Fanout Details

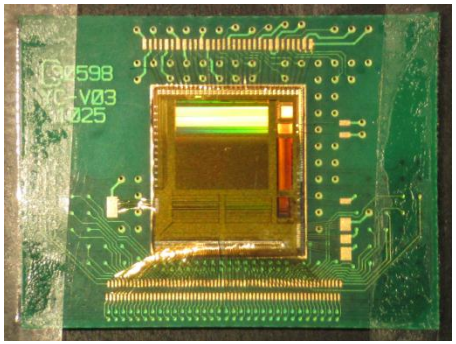


4 Layer Board: Red is top copper, blue is bottom copper, teal is power plane boundary. Ground plane also present

Production Experience



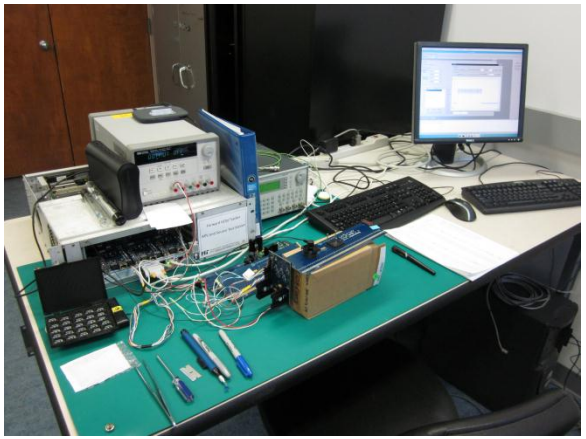
Manufacture Substrates – 20 days
Sierra Protoexpress, Sunnyvale, CA



Die attach, wire bond, encapsulation, solder ball attach – 5 days
Corwil Technology Corp. Milpitas, CA

Delivery to Bates – 1 day

Assembly into Front End Boards – 10 days
Proxy Manufacturing, Metheun, MA



Testing at Bates – 1-2 days

Minimum nominal time: 37 days

- Both substrate manufacture and board assembly can be sped up at a cost premium

Production Problems

- Epoxy flowing through substrate
  - First run: we got lucky; soldermask blocked vias
  - Had to respin lot of 185 packages with vias plated shut

- Moisture content of packages
  - 5 Prototype boards were sent out almost immediately after finished packages were received, all boards worked less one chip
  - Production boards were sent out later, and were not baked before reflow. This caused severe damage to many chips, severely reducing yield.
  - Subsequent runs avoided this problem by simply baking packages for 24 hours before installation within 48 hours after baking.

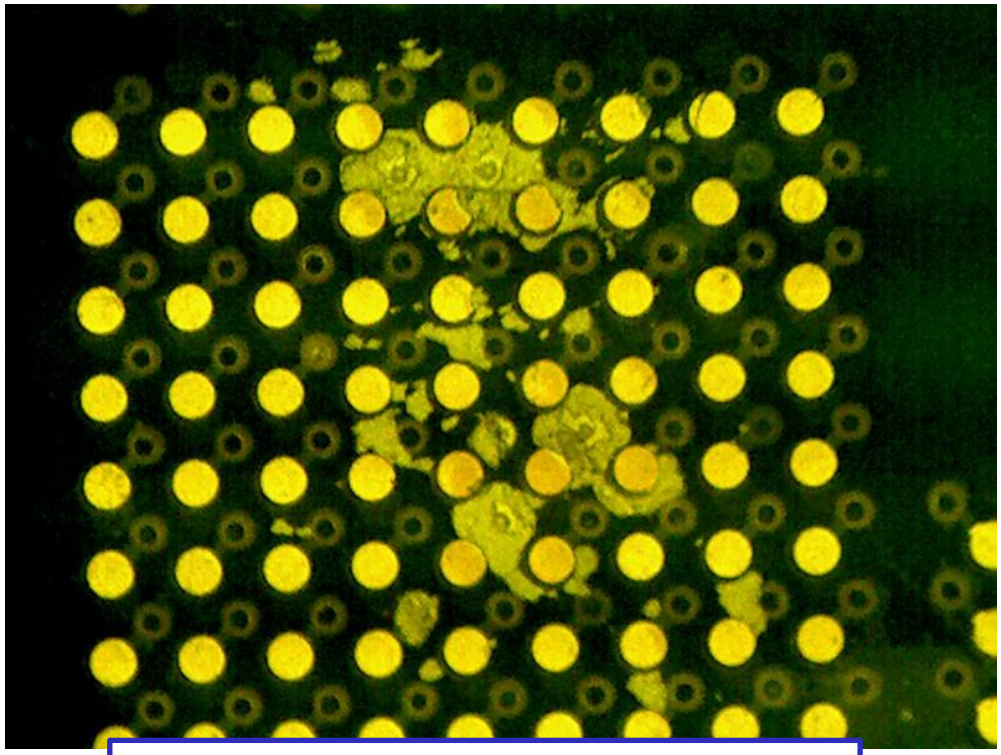


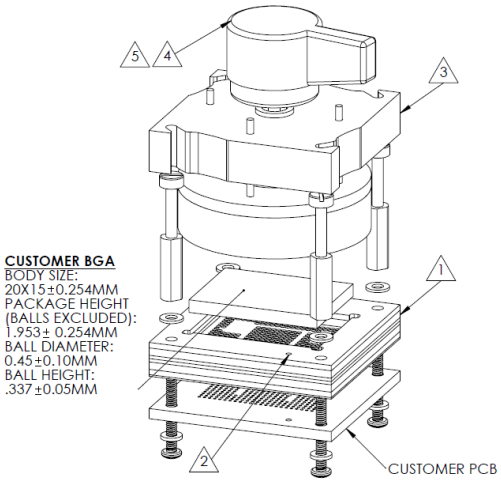
Photo from Corwil after discovering problem

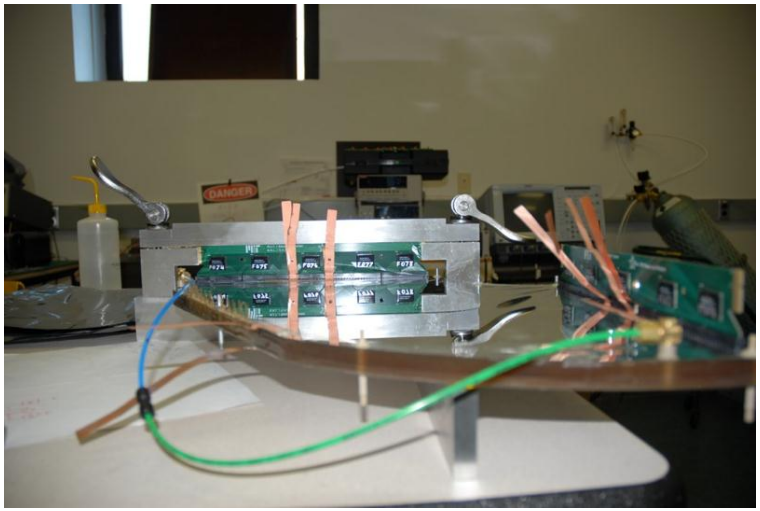
Results

- FGT Readout Module; 5 Chip FEE Board, 640 channels
  - First run yield was extremely poor due to moisture problem, nearly all of the boards had one or more chip broken
  - Most recent BGA run of 185 chips, incorporating all of lessons learned, had **94% yield** on packaged chips after testing at Bates.
  - Most recent FGT Readout Module assembly run of 35 boards had 100% yield after testing at Bates. These boards are installed currently in STAR.
    - Caveat: During the 2012 run, some chips on some boards failed. We are hoping that these new boards which did not experience extreme stress because of moisture content will be more reliable, but this information is not yet available!
  - Readout by a modular APV Readout System for STAR, also used the IST Experiment at STAR (designed by G. Visser at IUCF, see references)
- Dual APV Module; 2 Chip FEE Board, 256 channels
  - Boards from first run were salvageable.
  - Approximate 50% yield reported by both GMT and OLYMPUS
  - Repairs done at Proxy to remove damaged APV package and replace with functioning APV Package
  - Readout by the same modular APV Readout System for STAR for the GMT Experiment
  - Readout by a special VME readout system for the OLYMPUS Experiment, designed by Elektroniklaboratorien Bonn UG in Germany

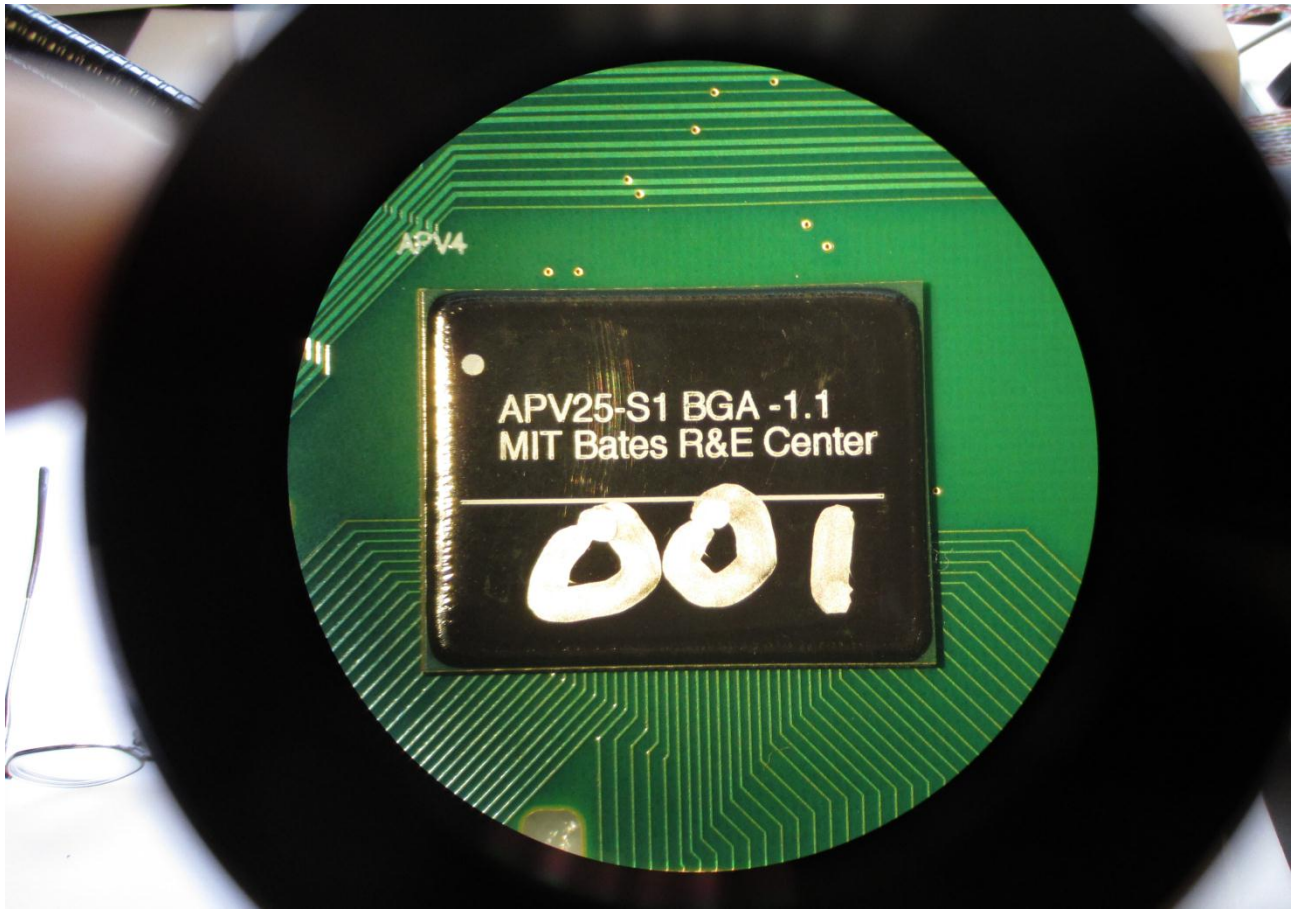
Recommendations

- Consult with a packaging company, but do the substrate design yourself; we ended up doing all of the engineering, and directing their designer how to do the layout.
- Layout a reasonable board before sending package design to be manufacturer.
- Check to see if a package socket exists or can be made to test your final product.
- Use a common size solder balls.
- Be sure to understand the moisture sensitivity of your packages: ask assembler about this!
- Include mechanical balls for package stability.
- Be wary of mechanical stresses during installation – excessive force may warp board and damage BGA solder connections





Questions?



We have invested significant amounts of time and money into our APV packaging design and front end card designs. Contact me if you would like to use any of these designs. We'd love to see other people using them!

bbuck@mit.edu

Recommended References

- G. Visser et. al., “A Readout System Utilizing the APV25 ASIC for the Forward GEM Tracker in STAR,” IEEE Real Time Conference Record, Berkeley, CA, 2012.
- L. Jones, “APV25-S1 User Guide Version 2.2,” Royal Academy London, 5 September, 2001.