Integration of SRS/SRU in the ATLAS Micromega readout

Installation of prototype chambers in ATLAS

- 2 chambers 9x4.5 cm² @MBTS region, r ~ 1,0 m
- 4 chambers 9x9 cm² @Small Wheel, r ~ 1,7 – 1,8 m
- Goal: compare MM tracks with ATLAS data

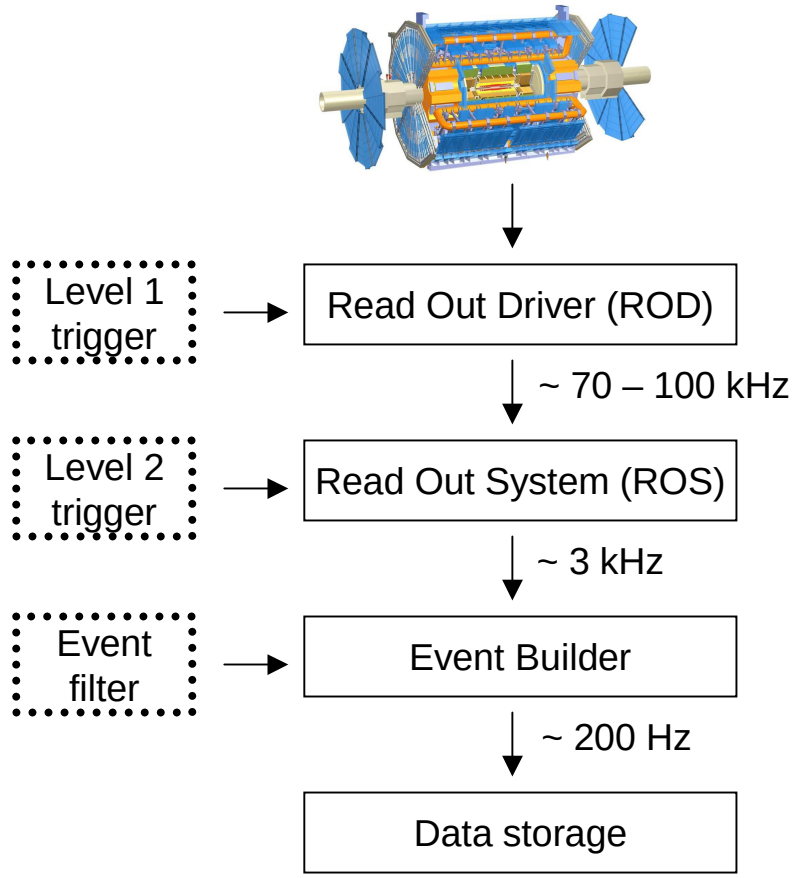
ATLAS data acquisition chain

- Read Out Drivers (ROD) read out detectors for each Level 1 trigger

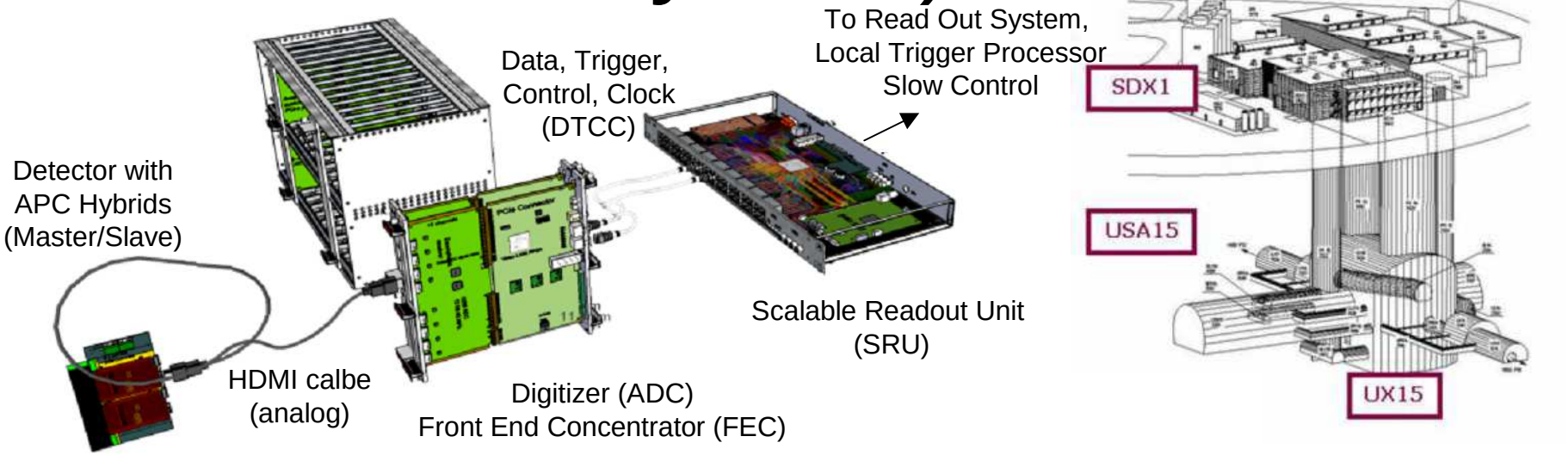
- Data is stored locally on „ROBIN“ cards, inside the Read Out System (ROS) PCs until a level 2 trigger decision is made

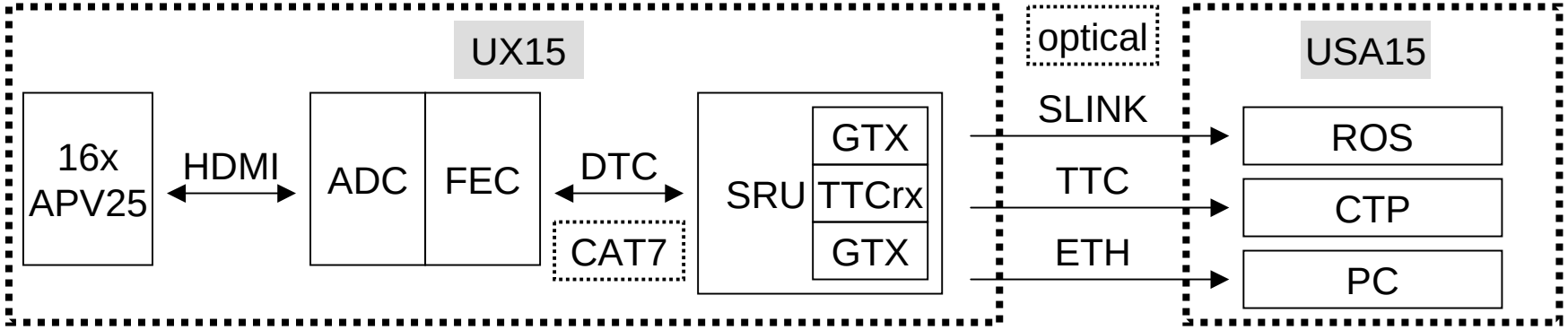
- Only raw data matching a Level 2 trigger are transferred to the ROS PC and the Event Builder PC farm

- Finally data are written to storage with ~200 Hz

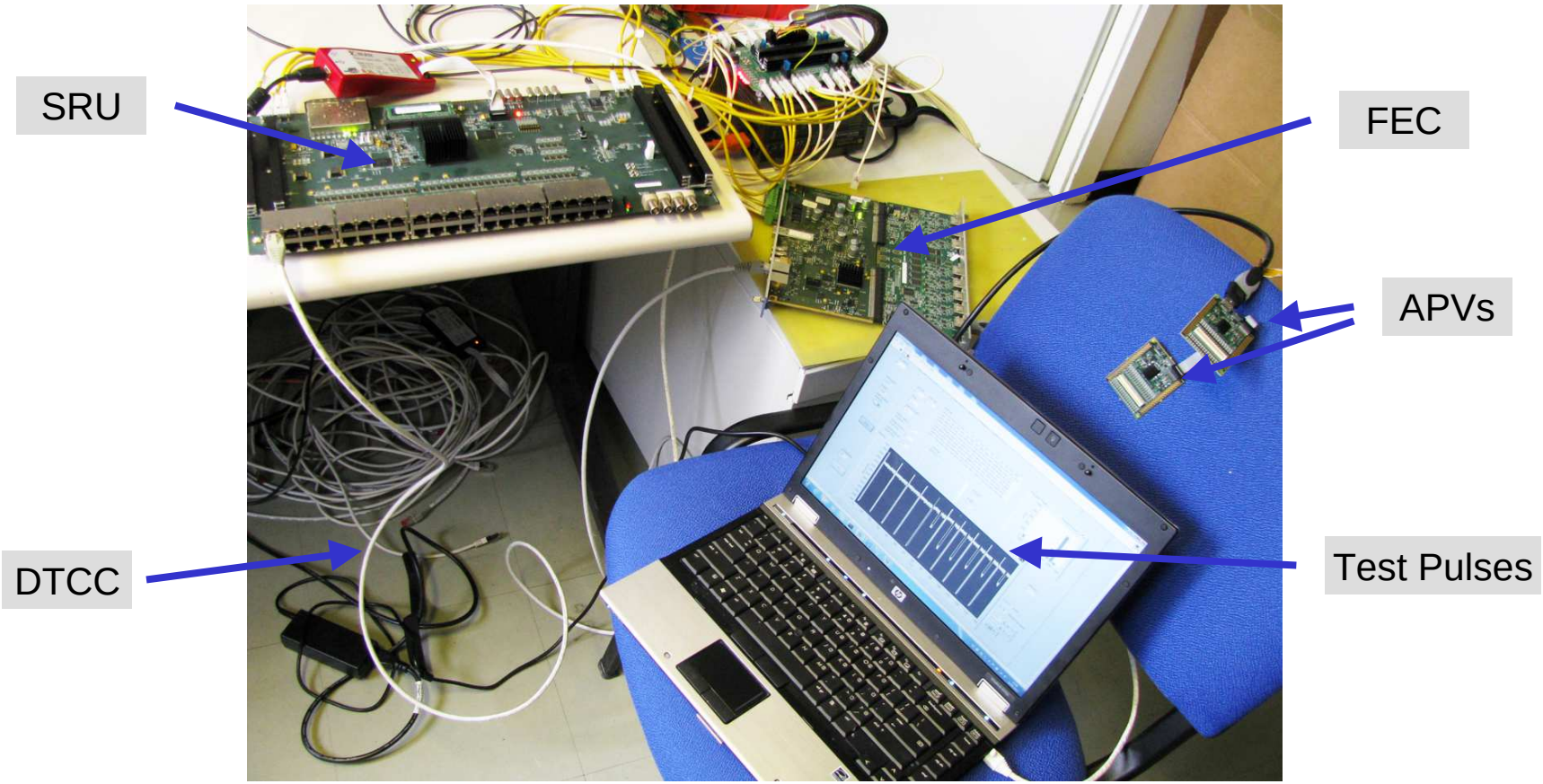


SRS (Scalable Readout System)

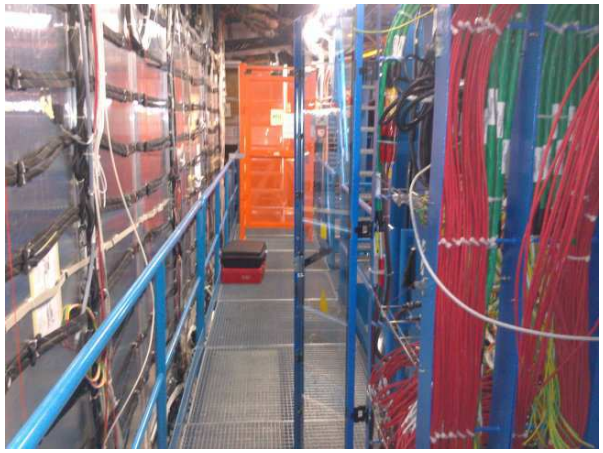




Desk setup



SRS Installation at ATLAS cavern



SRU (Scalable Readout Unit)

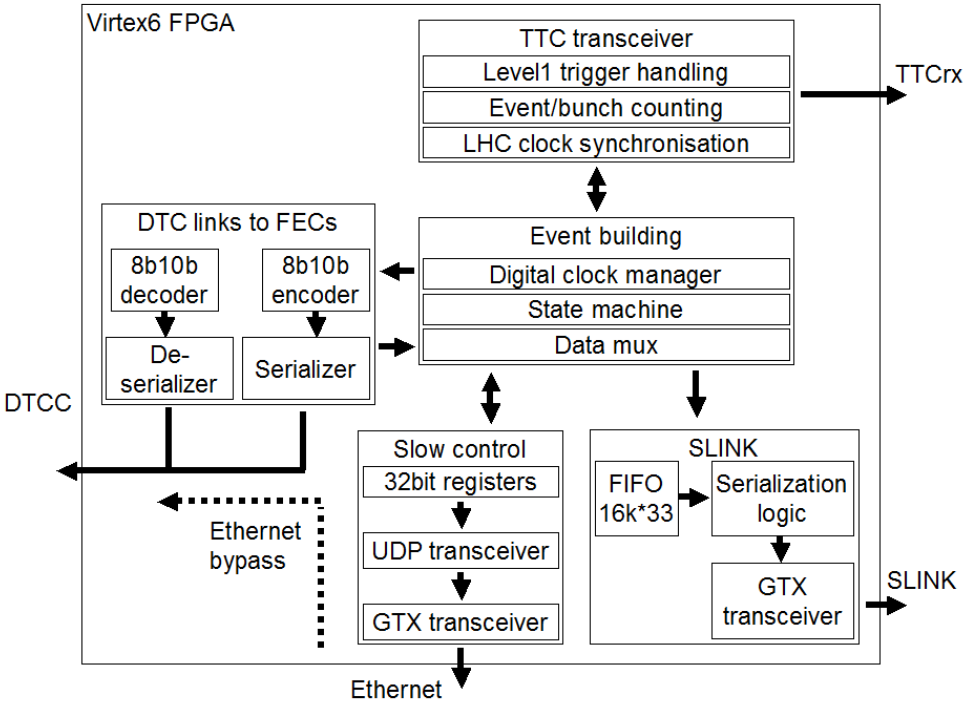
Main tasks:

• Reception and distribution of Level1 triggers, LHC synchronization
 - Clock Phase
 - Bunch Counter reset
 - Event Counter reset

• Detector data collection and event building
(BCID, EVID, ... , Data)

• Data transmission to ROS PC via SLINK

• Slow control / DCS / Data preview via Ethernet



TTC interface

- SRU uses onboard TTCrx chip to receive BC clock, L1A, ECR, BCR and trigger type
- Connect to CSC TTC partition with unique TTC address
- Additional user-programmable offset value for BCID
- Receive Broadcast or Individually Addressed Commands

DTCC Links

(A. Martinez)

- Uses 4 Cable pairs of a conventional CAT cable with RJ45 plugs to transmit Data, Trigger, Control and Clock
- Transmits TTC clock to FEC Cards and APVs
- Foreward triggers with fixed latency, synchronous to the BC clock
- Carry Slow Control commands to FEC and APV chip, ...
  SRU ist transparent for Ethernet frames dedicated to the FEC card
- Return detector event data at 640 Mbit/s, either to the SRU to to the Slow Control PC, bypassing the SRU
- Hot plug ability and automatic resynchronisation

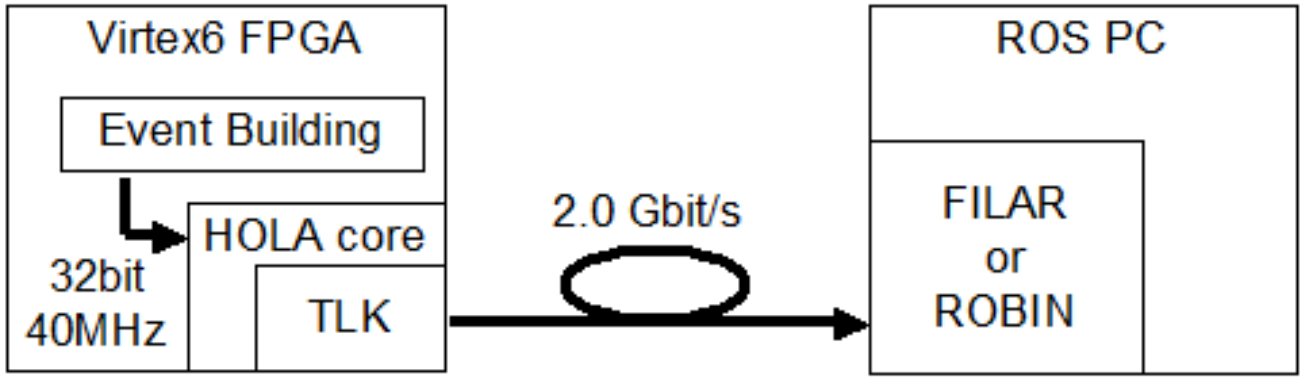
SLINK implementation

(M. Della Volpe, R. Giordano, V. Izzo, S. Perrella)

• Event data are transmitted using SLINK to the data aquisition system (formerly HOLA based)

• No need of a seperate HOLA daughter card, due to the implementation of the serialisation logic in the Virtex6 FPGA (GTX transceiver)

• Data transfer to a standard ROS PC tested successfully with both FILAR and ROBIN pci cards. Valid ATLAS data frames are received.



DCS / Slow control

- Slow control is done via optical Gbit ethernet connection to the SRU
- SRU DCS requests are handled directly, packets for FEC and APV are forewarded via DTC links (ethernet switch)
- Online access to parameters like run control and error conditions
- Fine tuning of TTCrx, APVs, etc...
- Possibility to bypass the SRU by sending detector data to the ethernet for online results of calibration, data preview, ...

FPGA Ressources

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	8,524	160,000	5%	
Number used as Flip Flops	8,499			
Number used as Latches	4			
Number used as Latch-thrus	0			
Number used as AND/OR logics	21			
Number of Slice LUTs	11,216	80,000	14%	
Number used as logic	7,828	80,000	9%	
Number using O6 output only	4,921			
Number using O5 output only	718			
Number using O5 and O6	2,189			
Number used as ROM	0			
Number used as Memory	2,856	27,840	10%	
Number used as Dual Port RAM	2,784			
Number using O6 output only	2,688			
Number using O5 output only				
Number using O5 and O6				
Number used as Single Port RAM				
Number used as Shift Register				
Number using O6 output only				
Number using O5 output only				
Number using O5 and O6				
Number used exclusively as route-thrus				
Number with same-slice register load				
Number with same-slice carry load				
Number with other load				

Number of LUT Flip Flop pairs used	13,504			
Number with an unused Flip Flop	6,250	13,504	46%	
Number with an unused LUT	2,288	13,504	16%	
Number of fully used LUT-FF pairs	4,966	13,504	36%	
Number of unique control sets	522			
Number of slice register sites lost to control set restrictions	2,017	160,000	1%	
Number of bonded IOBs	90	600	15%	
Number of LOCed IOBs	90	90	100%	
IOB Flip Flops	2			
IOB Master Pads	2			
IOB Slave Pads	2			
Number of bonded IPADs	6			
Number of LOCed IPADs	6	6	100%	
Number of bonded OPADs	4			
Number of LOCed OPADs	4	4	100%	
Number of RAMB36E1/FIFO36E1s	75	264	28%	
Number using RAMB36E1 only	75			
Number using FIFO36E1 only	0			
Number of RAMB18E1/FIFO18E1s	14	528	2%	
Number using RAMB18E1 only	14			
Number using FIFO18E1 only	0			
Number of BUFG/BUFGCTRLs	18	32	56%	
Number used as BUFGs	18			
Number used as BUFGCTRLs	0			
Number of ILOGICE1/ISERDESE1s	2	600	1%	

Event building

- Each L1A trigger (generated either by TTCrx (ATLAS), NIM (Lab) input or slow control (debug)) is stored in a FIFO memory, and processed sequentially
- Not every Level 1 trigger (~70 kHz) can be served by the APV chips, due to multiple time-bin readout (see later slide), but skipped triggers will also form a (quite empty and marked with status word) ATLAS data word, including all neccessary headers and trailers
- Converted data from the APV chips will be zero-suppressed and then written (via DTC link) to FIFO memorys in the SRU FPGA
- Full event is formed and sent out via SLINK to the ROS PC

L1A rate vs. APV readout time

- Using the MicroMegas detectors in a „TPC-Mode“ requires to read several time bins from the APV. Reading >10 timebins is only possible with <30kHz rate
- The Readout of a full event takes longer than the mean time difference between Level 1 triggers (~70 kHz)
- Implementation of busy-logic to decide, which event to process normally (trigger to APV chips), and which not
- Skipped events will also generate an ATLAS event frame, with very limited content, but in the correct event order (FIFO storage for triggers)
- Tested and working with up to 100 kHz random trigger rate, L1A FIFO buffer is 4096 elements deep (Can also be increased)

L1A rate vs. ROS speed

- Currently the ROS PC connected to the SRU runs a „stand-alone“ Data aquisition partition („safe mode“)
- In this way, the ROS does not receive online Level 2 trigger information
- All Level1 triggers have to be stored, which is only possible up to a rate of ~11 kHz
- Another stage of busy logic had to be added, to check the SLINK FIFO on SRU and skip events in case it is „almost full“
- To keep data consistency, consecutive L1IDs are written to the event header and „real“ L1ID are written to the events payload
- Offline Synchronisation with L1ID and Timestamp

Status and outlook

• All neccessary hardware has been installed in the ATLAS cavern during the September technical stop

• Event bulding firmware is running and generating valid ATLAS ROD fragments

• DTCC link transmits APV data either to the SRU for eventbuilding, or to the slow control PC (via ethernet) for debugging/preview

• Running in „safety mode“ since ~1 week

ToDo during the remaining 9 weeks of Proton collisions:

• Tuning of several parameters, debugging

• Take as much data as possible for offline analysis and comparison with ATLAS data