

LHCb Upgrade
Mar 01, 2012
CERN

Toward the readout board project

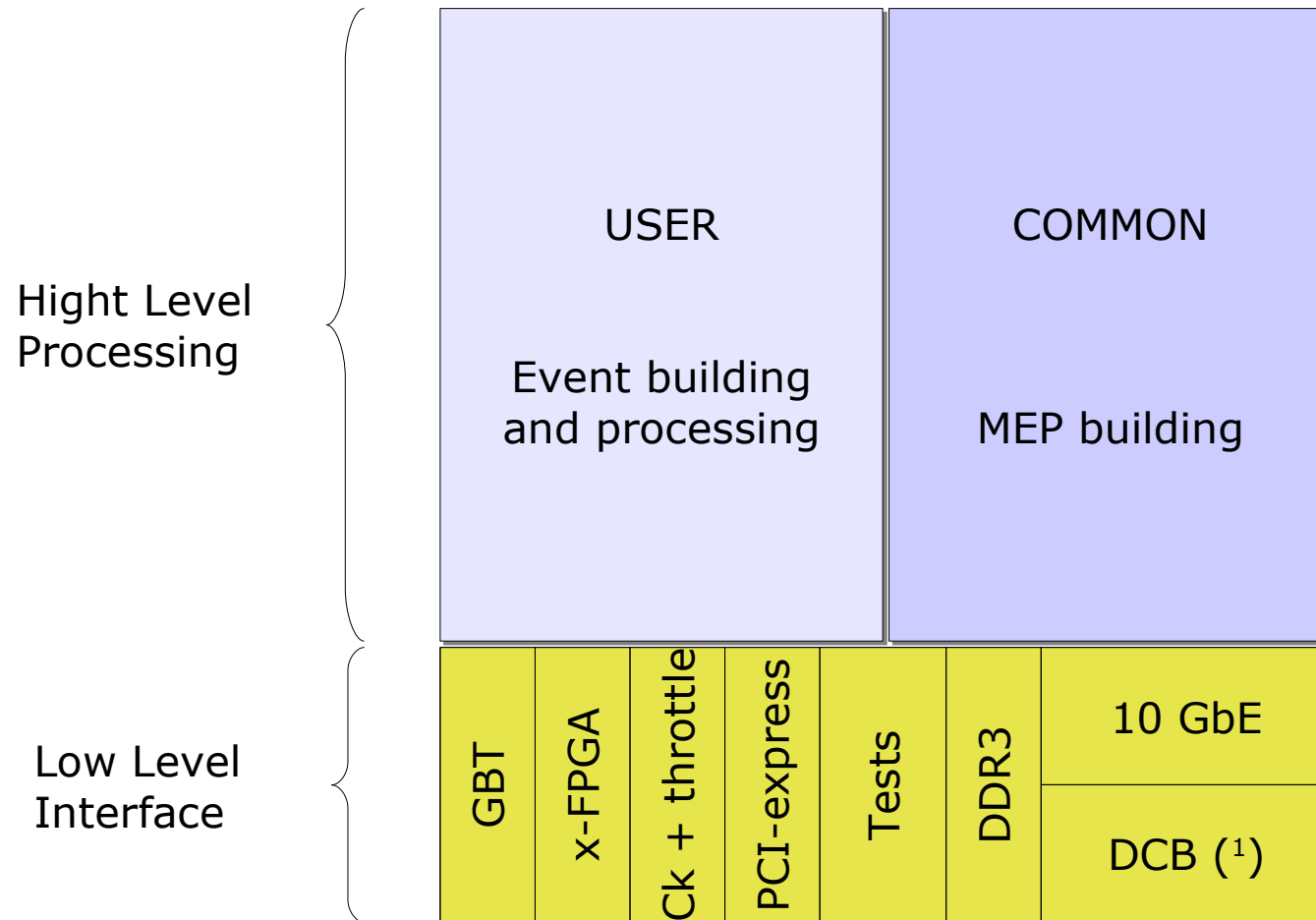
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The Readout Board project

<i>WP</i>	<i>Work Package Title</i>	<i>Interested Lead Participant</i>
0	Coordination	Marseille
1	Hardware	Marseille
2	Firmwares	Annecy
3	PVSS Supervision	
4	Commissioning	
5	Maintenance	

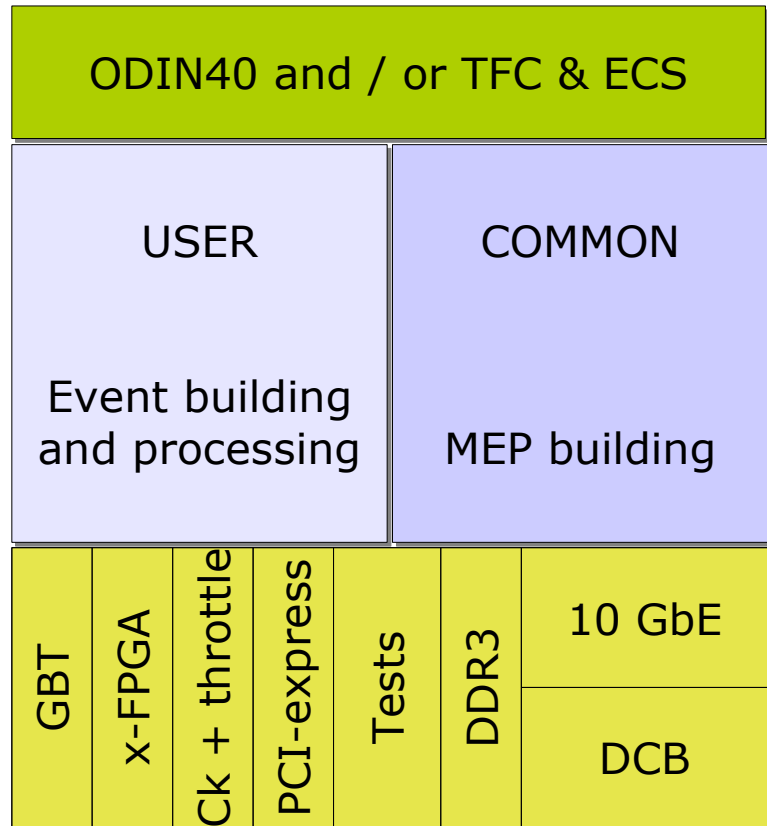
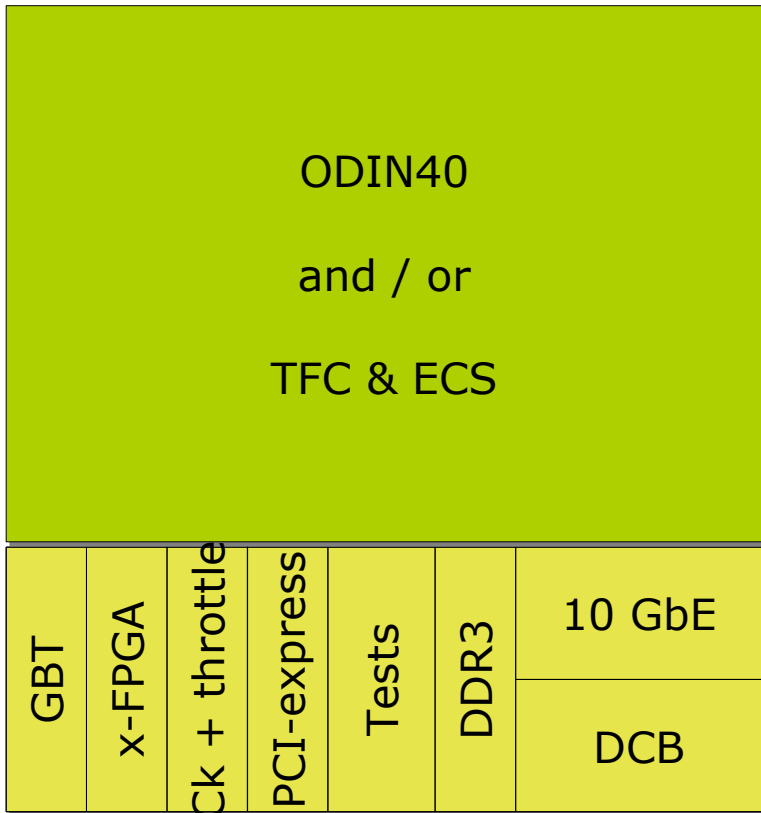
WP 2: firmware developments

Radiography of the TELL40 FPGA



⁽¹⁾ Data Center Bridging

Variants



Firmware Development Work Packages

WP	Title	Participant(s)	Ø(FTE)	Cost	Developpers
0	Coordination	Annecy		–	Stéphane T'Jampens + Cyril Drancourt
1	Specifications, documentation and reviews	Annecy		–	Stéphane T'Jampens + Cyril Drancourt
2	Low Level Interface	Marseille	6	–	Jean-Pierre Cachemiche et al.
3	Data Centre Bridging	CERN		–	Rainer Schwemmen
4	TELL40 MEPs building	Annecy (tbc)	4	–	Cyril Drancourt et al.
5	TELL40 generic user	Annecy (tbc)	2	–	Cyril Drancourt et al.
6	ODIN40, TFC&ECS	CERN		–	Federico Alessio + Richard Jacobsson
7	VELO pixel	Manchester, AGH-Krakow		–	Chris Park et al. + Tomasz Szumlak et al.
8	VELO strip			–	
9	Central Fiber Tracker			–	
10	Scilicon Strip Tracker			–	
11	OT	Dormunt		–	Stefan Swientek et al.
12	RICH	Cambridge		–	Stephen Wotton
13	TORCH			–	
14	CALO			–	
15	MUON	Italie		–	
16	LLT CALO	Annecy	2.5	–	Cyril Drancourt et al.
17	LLT MUON	Marseille	2	–	Jean-Pierre Cachemiche et al.
18	LLT L0DU	Clermont		–	Régis Lefèvre et al.
19	CCPC and test bench	Rio (CBPF)			André Massafferri

Next steps

- ▶ Kick off meeting with interested developers:
requirements, architecture of TELL40 FPGA, tools, ...
- ▶ May 2012:
 - Addendum to the LoI ready:
cost, schedule, milestones, interested institutes / commitments
- ▶ **End 2012 (R&D milestone)**
 - Validate that the selected Stratix V has enough resource to satisfy the requirements of the most demanding user (VELOPIX)
- ▶ Mid 2013:
 - TDR ready
- ▶ End 2013:
 - deploy a small fraction of the new readout