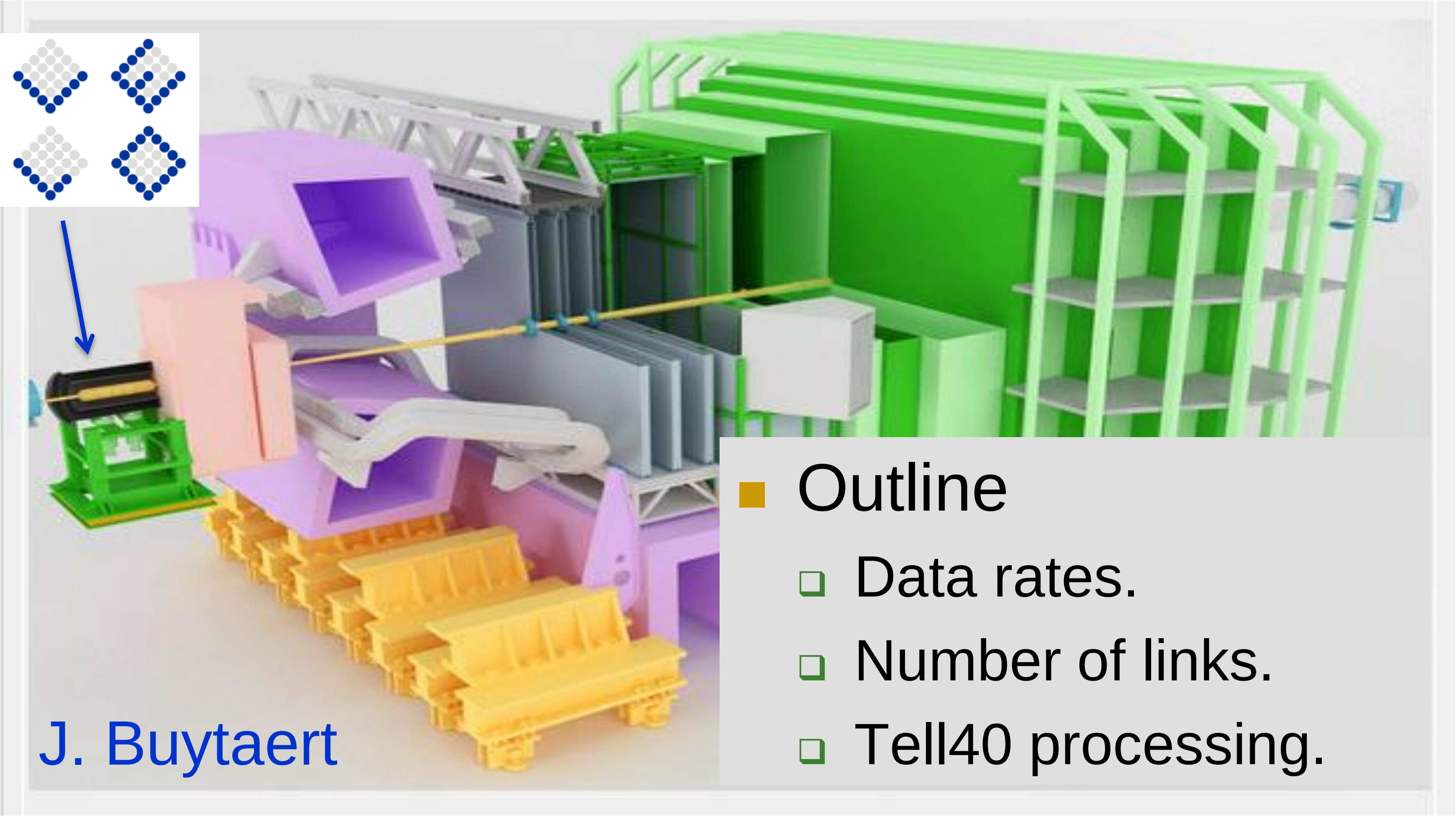
VELO Upgrade Tell40.



- Outline
  - Data rates.
  - Number of links.
  - Tell40 processing.

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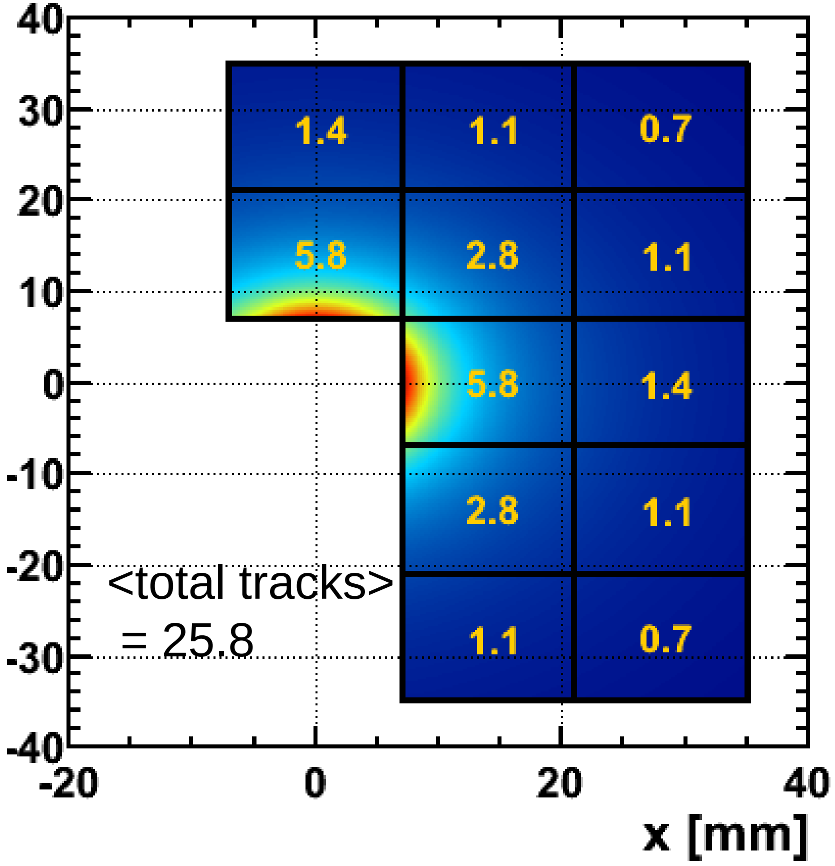
Pixels : track, pixel and data rates @ L=2 x 10^{33}

- Hottest ASIC: 5.8 tracks/25 ns = 230MHz track rate.
- Half station : 25.8 tracks/25ns = 1 GHz track rate.
- Assume 1 track = 1 cluster. (not true for super pixel boundary)
- Simulation gives 2.2 pixel hits/cluster.
- Hottest chip must cope with ~ 500 MHz pixel hit rate.
- Compressed data scheme has (28+n*8) bits per cluster (n= # pixel in cluster). On average 52.3 bits/cluster.
- Hence 12.2 Gbit/s from hottest chip.
- 54 Gbit/s from a halfstation.
- 2.8 Tbits/s from whole VELO …

(For L=10^{33} these numbers are all divided by 2)

Half station :
Number of tracks/ asic / event

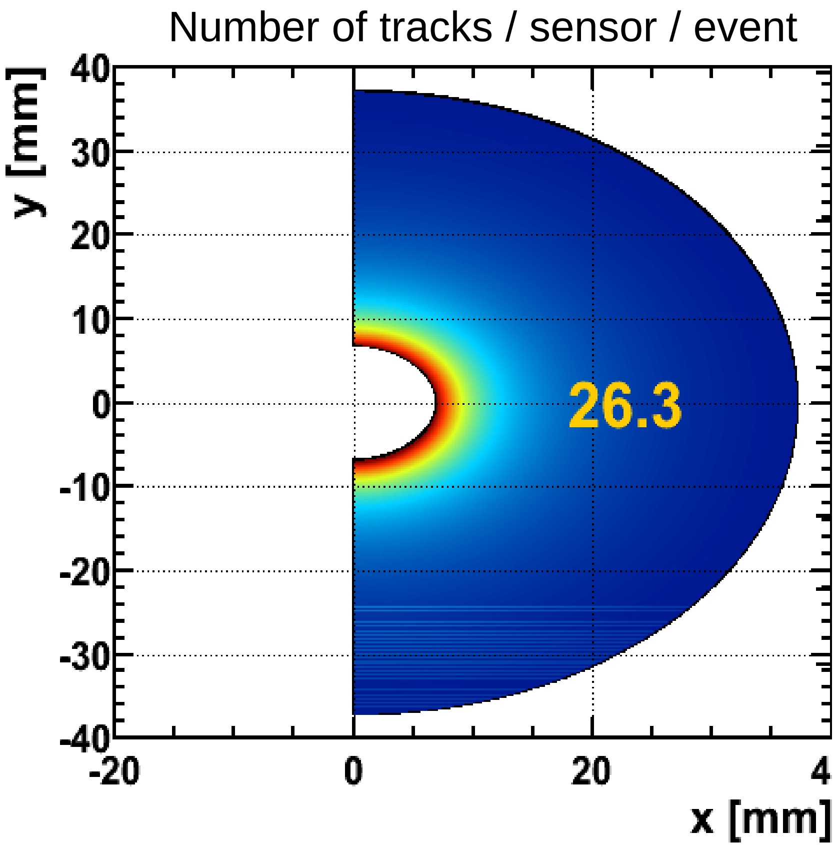


<total tracks>
= 25.8

Strips: track, strip and data rates @ L=2 x 10^{33}

- Half station is an R and PHI sensor !
- Options: 128 channel or 256 channel asic.
- 20 (10) asics/ sensor or 40 (20) asics /half station

- 26.3 tracks /sensor / 25ns.
- 1.3 (2.6) clusters per ASIC (ignore diff between R and P)
- 1.6 hits per cluster (ignore diff between R and P)
- On average, 26.5 (21.5) bits per cluster .
- 1.4 (2.24) Gbit/s per asic . (not entirely true for PHI)
- 56 (44.7) Gbit/s per half station.
- 2352 (1880) Gbit/s for the whole VELO .



VELO numerology @ $L=2 \times 10^{33}$

For strips ‘halfstation’
= r + phi sensor !

	strips 128 ch/asic 256 ch/asic	pixels	comment
# ASICS/half station	40 (20)	12	
# half stations	42	52	Strip inner coverage is better.
# ASICS total	1680 (840)	624	More asics for strips
Cluster size	1.6 (1.6)	2.2	Pixels share in 2 dimensions.
# clusters / half station/ 25 ns.	52.6 (52.6)	25.8	Twice more clusters for strip (R+PHI !)
# pixel(strips) hits/half station/25ns.	84.2 (1.6)	56.8	
# bits / cluster	42.4 (34.4)	52.3	~ equal
# bits / pixel(strip) hit	26.5 (21.5)	23.8	~ equal (note only 4 bits are analog info)
Hottest chip output rate	1.4 Gbit/s (2.24)	12.2 Gbit/s	Factor 10 ! Very uniform strip occupancy.
Coolest chip output rate	1.4 Gbit/s (2.24)	1.5 Gbit/s	
Data rate / half station	56 Gbit/s (44.7)	54.3 Gbit/s	~ equal
Total data rate	2352 Gbit/s (1880)	2823 Gbit/s	~ slightly smaller for strips.

Bottom line: 1. ~ equal data rates per halfstation : ~ 56 Gbits/s.
2. data rates/asic: very uniform for strips, but factor 10 spread for pixels.
3. Total data rates : strips 2.3 Tbit/s < pixel 2.8 Tbits/s

Number of links

Assuminga serial link with 3.2 Gbit/s user bandwidth.

- Pixel :
  - Hottest asic requires 4 links => 12.8 Gbit/s. No margin to increase luminosity beyond lumi20 !
  - All 'inner' asics will have 4 links. All 'outer' asics will have 2 links (redundancy !)
  - Halfstation :
    - (4 inner x 4) + (8 outer x 2) = 32 links.
    - Average bandwidth utilization is only 53% !

      = 54.3 Gbit/s / (32*3.2 Gbit/s)
  - Full VELO 52 x 32 = 1664 links

- Strip :
  - All asics have nearly equal data rates : 1.4 (2.2) Gbit/s.
  - 1 link /asic sufficient.
    - Could cope with lumi40 for 128 ch strip.
    - No redundancy.
  - Half station (R+PHI) :
    - 40 (20) links.
    - Average bandwidth utilization is only 43% !

      = 56 Gbit/s / (40*3.2 Gbit/s)
  - Full VELO : 42 x 40 (20) = 1680 (840) links.

Bottom line : Equal # links for pixel (1664) and 128 ch Strip (1680) options.

Tell40 processing

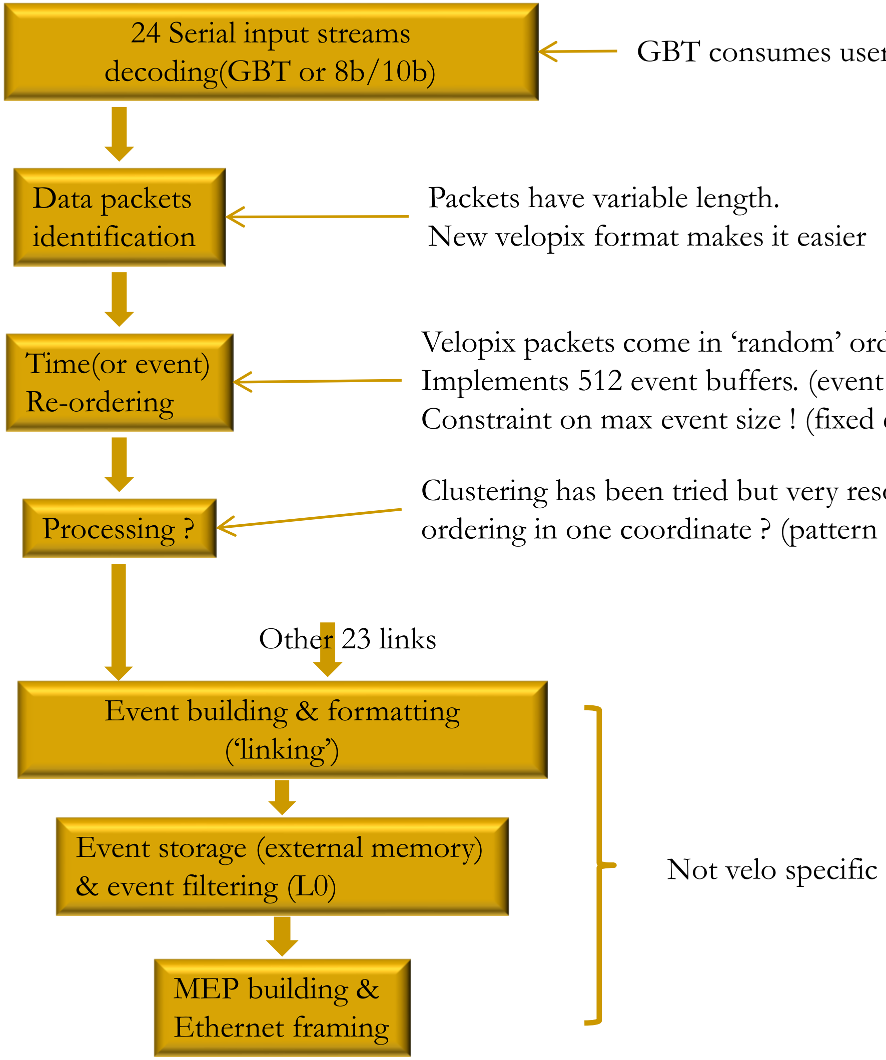
- Pixels:
  - Individual serial input links:
    - Extract variable length packets.
    - Event building :group all hits from the same bcid. ('time reordering').
  - Event building from all input links on same AMC:
    - 1 half station per AMC : 32 links ?
  - Data reduction ?
    - Remove common 12 bit bcid
      - Average event size per half station ~1350 bit
      - Remove bcid : save 25 x12 = 300 bit .
    - Add asic ID code identification on each hit:
      - 25 x4 bit : 100 bit
    - Add extra formatting :
      - Half station ID, header words, padding bits ,…
    - Assume NO data reduction or increase.
  - BUT : input link utilization is only 53 % . So , only need 32/2=16 output links.

- Strips:
  - common mode suppress, clustering is done an asic.
  - Data packets
    - Also variable length.
    - Assumed to time ordered.
  - Still not very clear since digital backend of Strip asic has not been designed yet.
  - Processing appears to be similar to pixels , except for time ordering.

VHDL code.

- For pixels, an architecture and VHDL implementation has be written by Xavier Gremaud & Guido Haefeli (EPFL Lausanne).
  - Details in last Presentation in LHCb General Electronics on tell40 :
    - https://indico.cern.ch/contributionDisplay.py?contribId=1&confId=121556)
  - LHCb note with full description is added to agenda.
- Manchester University and Cracow University have recently expressed interest in taking responsibility for further development of both pixel and strip TELL40 code.

Current TELL40VHDL pixel architecture



24 Serial input streams decoding(GBT or 8b/10b)

GBT consumes user logic, 8b/10b not.

Data packets identification

Packets have variable length.
New velopix format makes it easier

Time(or event) Re-ordering

Velopix packets come in 'random' order.
Implements 512 event buffers. (event number modulo 512).
Constraint on max event size ! (fixed event buffer length)

Processing ?

Clustering has been tried but very resource intensive.
ordering in one coordinate ? (pattern recognition !)

Other 23 links

Event building & formatting ('linking')

Event storage (external memory) & event filtering (L0)

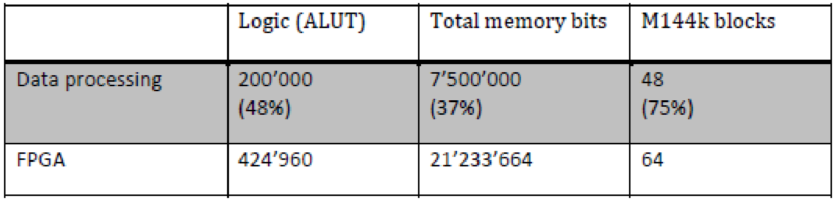
MEP building & Ethernet framing

Not velo specific

- 24 GBT link compile in Altera Stratix IV
- A lot of pipeline processing
- Most blocks run at 200 MHz.
- Very large data busses
- Almost no data reduction possible.

FPGA Ressource use:

- For 24 input links and without GBT decoding.
  - Should be increased to 32 …?
- Compiled and fits in Altera Stratix IV EP4SGX530.
- AMC prototype now : STRATIX V.
- Final AMC STRATIX VI ?
- Do not exceed 50%.
  - Add monitoring
  - New features (remember 1MHZ readout !)



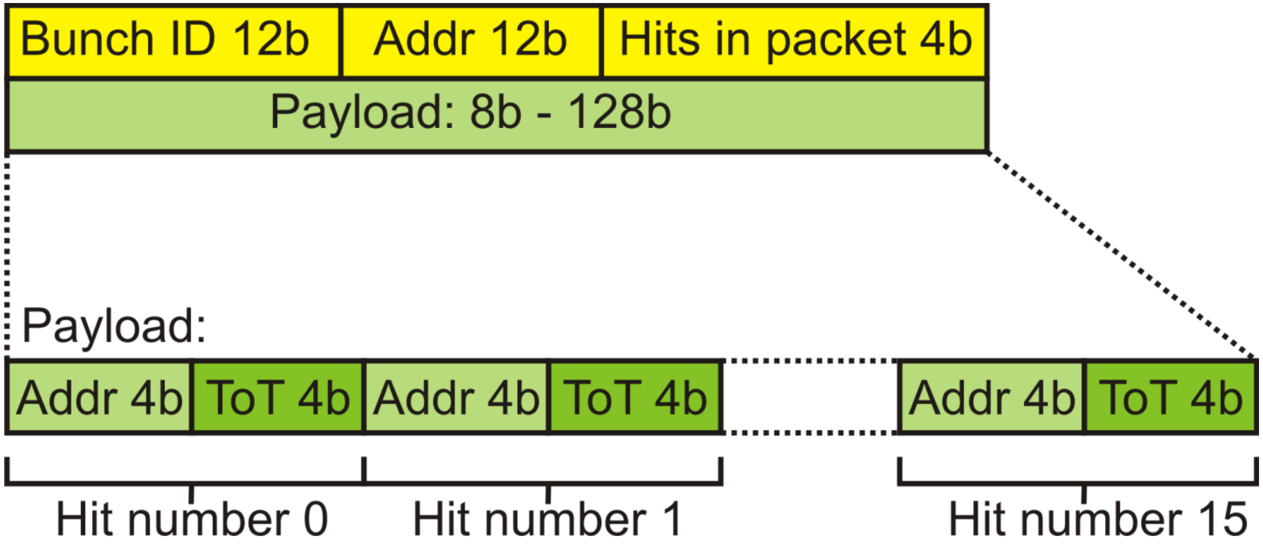
	Logic (ALUT)	Total memory bits	M144k blocks
Data processing	200'000 (48%)	7'500'000 (37%)	48 (75%)
FPGA	424'960	21'233'664	64

Figure 2-1 : FPGA resource utilization with unpacking the nSPP format and not much monitoring

Conclusions.

- Pixel and Strip hit rates are quite well understood from simulations.
- Modeling of the frontend ASIC is quite advanced for the pixel. It will start soon for the strip version.
- The number of link is identical in both versions ~ 1700.
- Tell40 code for the pixel is 90% available. It will start later for the strip and is supposedly easier.
- A 24 link pixel code fits in STRATIX IV, (with restrictions.)
- Development is taken over by Manchester and Cracow universities.

Velopix New Output Data Format



•Number of hits needs to be included in a packet to determine where a packet ends and the next one starts

•Grouping of pixels into a super pixel reduces the data rate by 25% (shared address and bunch ID).

• No compression efficiency is lost by the change to new format.