

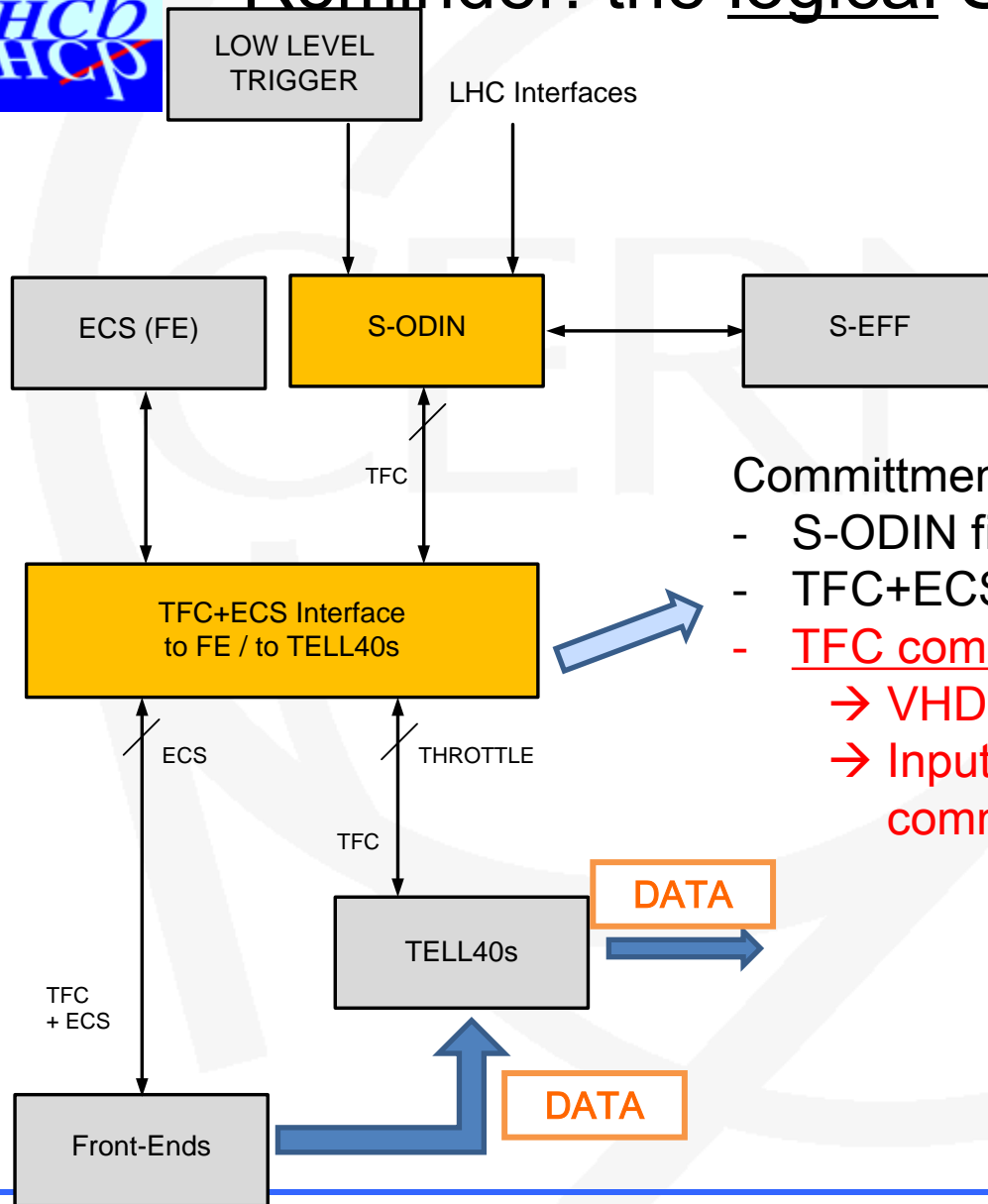


TELL40 FW discussion:
«*upgraded*» TFC points of view

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Reminder: the logical S-TFC at a glance



Commitment to provide:

- S-ODIN firmware
- TFC+ECSInterface firmware
- TFC commands decoding block in TELL40
 - VHDL entity to be plugged in
 - Input parallel TFC word, output commands



S-TFC documentation

- TFC system-level specifications note for the Upgrade just published
 - [LHCB-PUB-2012-001](#)
 - *Thanks for all the useful comments, please continue reading it!*

Soon:

- Functional specifications (shorter) for BE and FE
 - detailed definitions and usages of TFC commands in BE and FE
 - *aim at April*



TFC Back-End Word Format

TFC Word to BE: 44 bits (60 with Reed-Salomon encoder) @ 40 MHz = 1.76 (2.4) Gb/s

Encoding	43 .. 32	31 .. 16	15 .. 12	11 .. 8
TFC Info	BID(11..0)	MEP Dest(15..0)	Trigger Type(3..0)	Calib Type(3..0)

7	6	5	4	3	2	1	0
Trigger	BX Veto	NZS	Header Only	BE reset	FE reset	EID reset	BID reset

Constant latency after S-ODIN

- ✓ **THROTTLE Information from BE:** 1 bit per board connected to TFC+ECSInterface. Full set of bits sent to S-ODIN by TFC+ECSInterface.



TFC Back-End control commands

- ✓ Control functions for Back-End
 - Same as Front-End
 - **Bunch ID for synchronization check with internal counter and data from FE**
 - Bunch Counter Reset
 - Event Counter Reset (reset of same counters as FE + all event related counters)
 - Header Only → Force FE to transmit only header and no data (Informative)
 - Calibration pulsing (informative)
 - Non-zero suppressed readout of current crossing (Informative)
 - Bunch Crossing Type Veto (Informative)
 - Front-End electronics reset (Expect only header from FE)
 - Back-End Reset (Header Only from FE during reset)
 - Trigger
 - Reject data (Header still sent to farm or not?)
 - Attention: In TFC word, the trigger (& MEP destination) is not associated to the transmitted BunchID and the rest of the TFC word
 - S-ODIN pipes the asynchronous local trigger information for the maximum latency possible for BE
 - **Realignment of all data for BE is done in TFC+ECSInterface via pipeline logic**
 - Trigger Type to define type of event, processing type, destination type etc
 - Multi-Event Packet Destination IP
 - Transmitted when MEP should be closed and transmitted
 - Any other needs? → Reserve bits



General comments

Development of S-ODIN and TFC+ECSInterface firmwares are *decoupled* from the development of TELL40 firmware:

- Independent VHDL entities with *dedicated functionalities*
- *Not many common points* in the development (of FW)

→ «plug&play» TFC decoding block for TELL40 provided as VHDL entity

→ S-ODIN and TFC+ECSInterface firmwares will be developed as VHDL code which will «plugged in» in their dedicated AMC40 FPGA

→ i.e., a VHDL block with inputs and outputs to the GX transceivers



General comments

But, **common points** (not from us though..):

- Profit from common low-level interface of AMC40 from Marseille
 - a common way to use the links interface is definitely a plus!
 - collaboration wide validation of the system
- Profit from common ECS-CCPC development
 - ... but with some *personalized variants* ... :

S-ODIN and TFC+ECSInterface needs hundreds of monitoring registers

→ counters and status registers above all

Also, possibility to change registers «on the fly», while running: *we need maximum flexibility at any moment during running!*

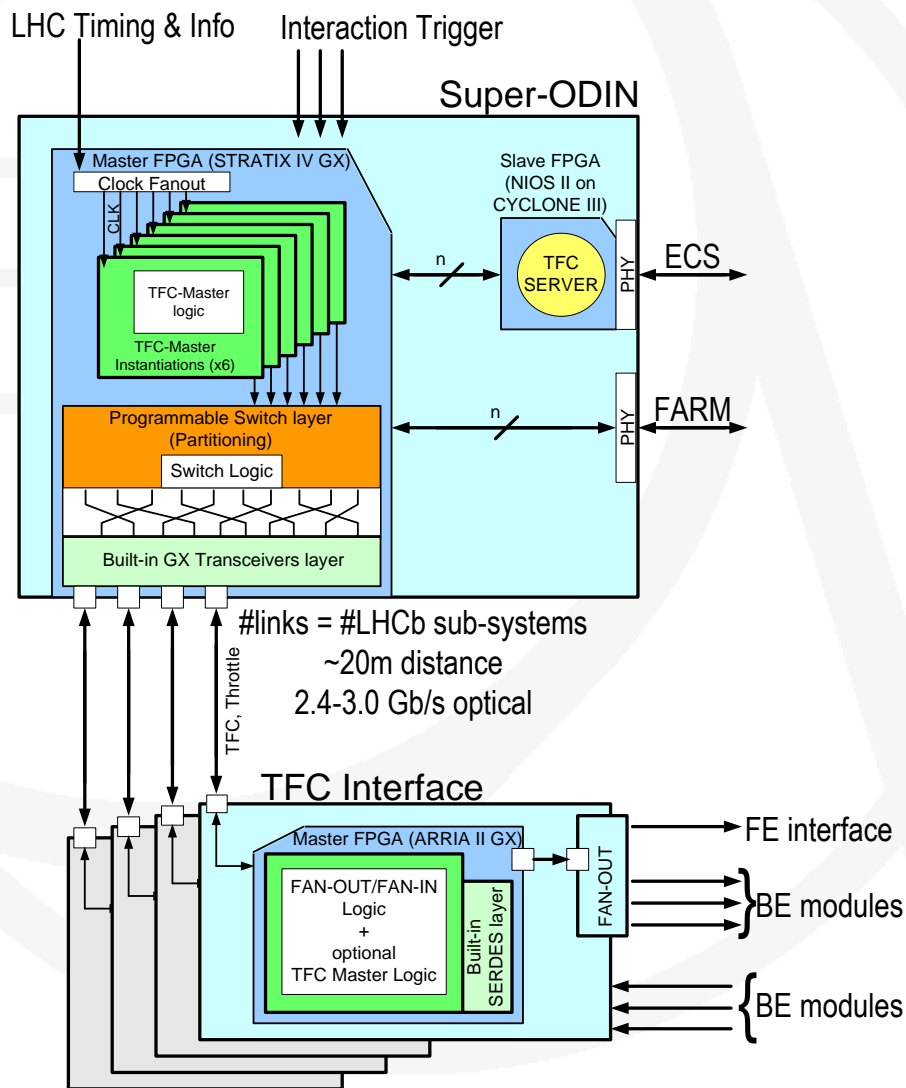
- ✓ «real time control» of FPGAs ...
- ✓ then the VHDL code will protect the readout control



CERN

Backups

S-TFC concept reminder





TFC Front-End control commands

- ✓ Control functions for Front-End
 - Bunch ID for synchronization check with internal counter
 - Bunch Counter Reset
 - Event Counter Reset
 - Reset of counter for accepted crossings = crossings for which header+data was sent
 - Reset of counter of truncated events
 - And all other event related counters (TFC command counters, etc!)
 - Header Only → Force FE to transmit only header and no data
 - Calibration pulsing (How many types do we need?)
 - Non-zero suppressed readout of current crossing
 - Following n crossing will receive “Header Only” → Header only transmission
 - Bunch Crossing Type Veto based on crossing scheme from LHC
 - Send header only for empty crossings and most single beam crossings
 - Front-End electronics reset
 - During the time of the reset (common duration) Front-End receives “Header Only” command and should transmit header only
 - Any other needs? → Reserve bits
- ✓ All TFC commands (individual signal) require local configurable delay



Front-End TFC Word format

TFC Word to FE: 24 bits inside GBT frame @ 40 MHz = ~1 Gb/s

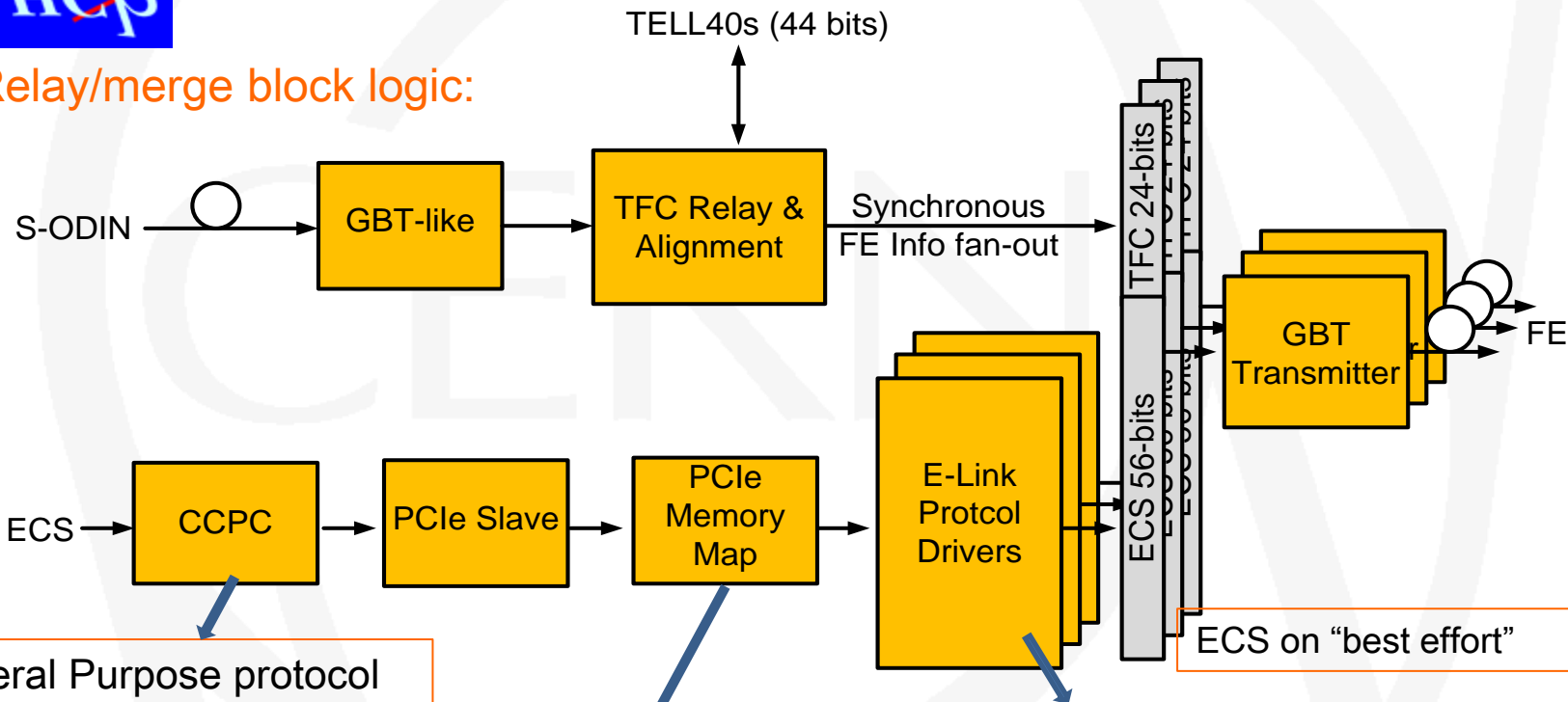
Encoding	23 .. 12	11 .. 9	8 .. 5	4	3	2	1	0
TFC Info	BID(11..0)	Reserve	Calib Type(3..0)	BX Veto	NZS	Header Only	FE reset	BID reset

✓ All TFC commands (individual signal) require local configurable delays



TFC+ECS Interface

Relay/merge block logic:



General Purpose protocol through DIM server on Ethernet (→goes PCIe)

'Memory Map' with internal address scheme for GBT addressing, E-link addressing and bus type

'Protocol drivers' build GBT-SCA packets with addressing scheme and bus type for SCA user busses:
- I2C, JTAG, Single-wire, parallel-port, JTAG, Memory, Temperature sensing, ADC



S-ODIN data bank

S-ODIN transmits a data bank for each accepted event in a MEP



S-ODIN data bank and LLT data bank is merged

(reminder: LLT is in same board as new S-ODIN)

- Info about timestamp, trigger type, bxid, trigger decision...
 - Mostly like now
- Will need at least 10GbE connection directly to FARM
 - what about 40GbE...? ☺
 - has to allow bandwidth partitioning as well
 - In fact «several» 10GbE (n*10GbE...)
 - reduced bank size for local tests
 - No LLT for instance