# SLAC I&C System Upgrades for LCLSII & Main Linac

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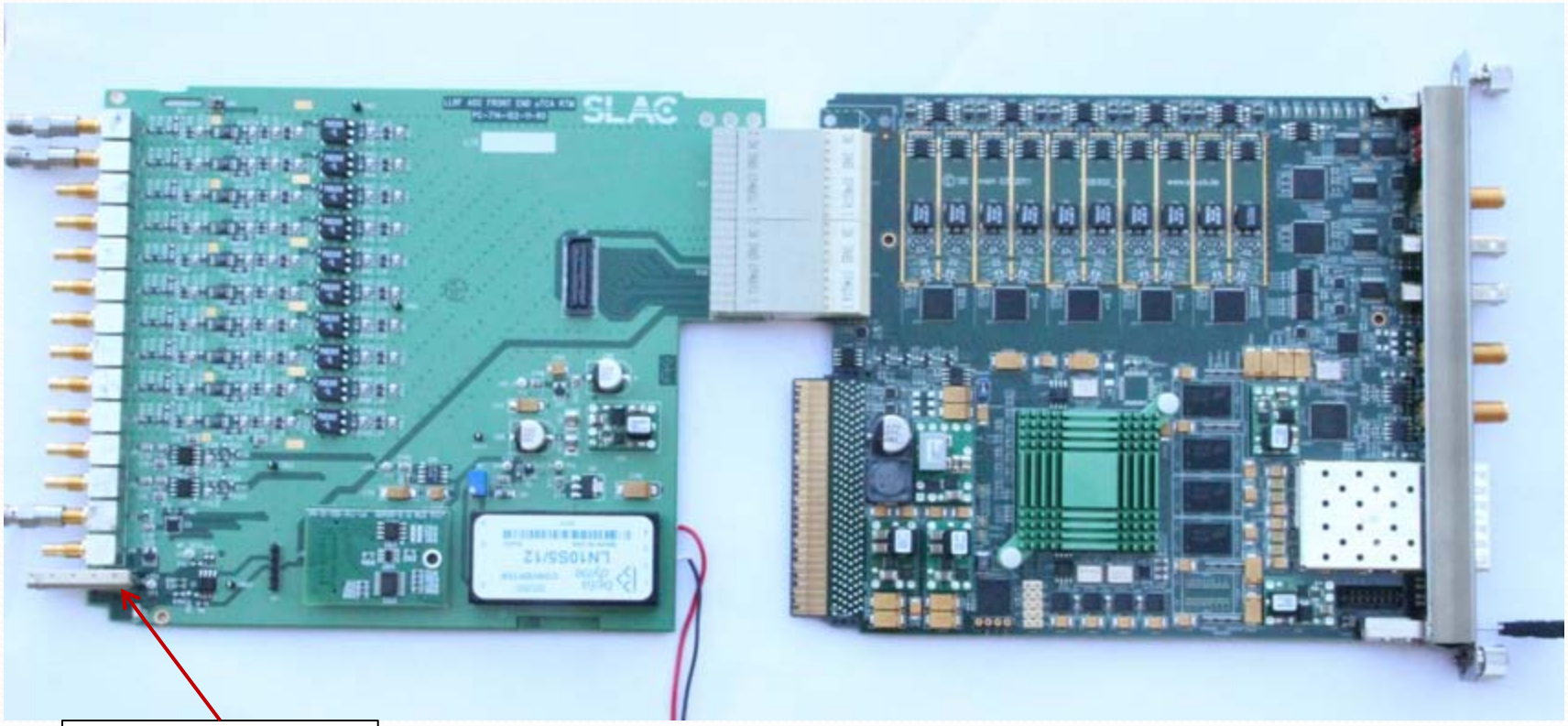
# Accelerator Upgrades

- LCLSII 4th generation light source underway
- Injector approved for construction 2013-15
- Linac, beamlines (2 undulators) 2014-17
- MTCA.4 proposed
  A. Limited application to Injector RF, BPMs
  B. Broader application to RF, Controls, Interlocks for 2-mile main linac (1/3 linac used by LCLSI, LCSLII and FACET high energy plasma wakefield experiment)

# Subsystems in Development

1. LLRF Feedback
2. BPMs Stripline
3. Klystron Interlocks

# 1. RF 10 Ch RTM, ADC-DAC

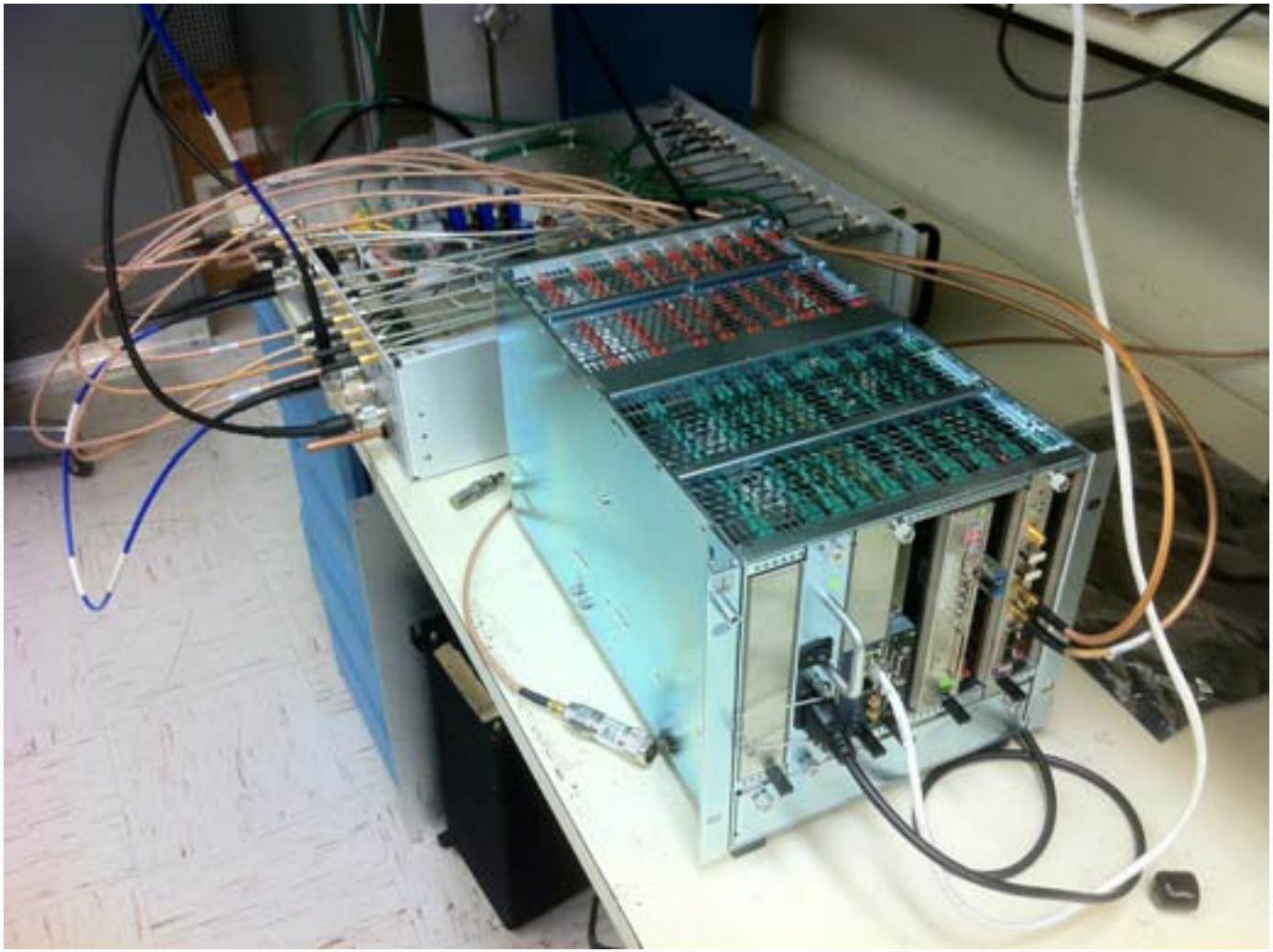



Trig,
RF
Ref
In

IPMI Extender
To RF Chassis

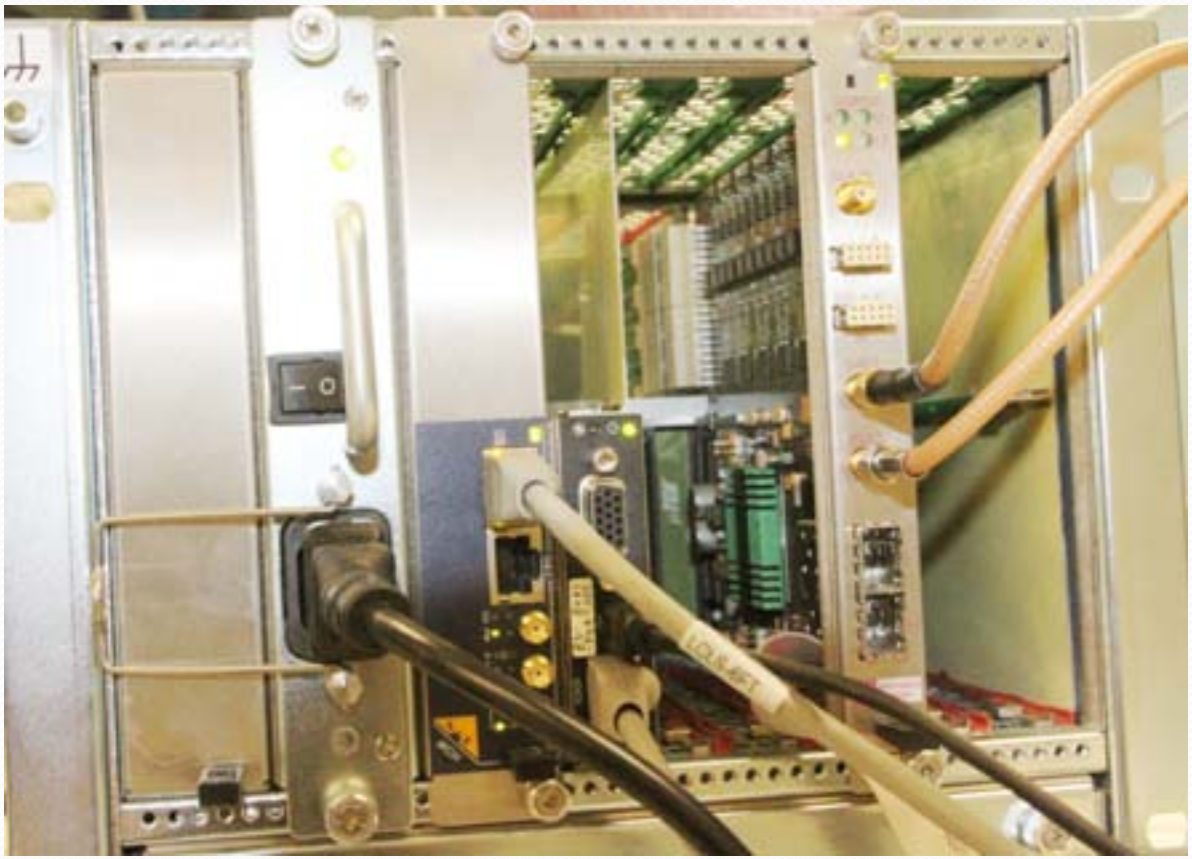
*RTM Design – A. Young*
*RTM layout – C. Yee*
*ADC-DAC – Struck SIS8300*

# Bench test simulation with RF chassis in background



- RF Chassis design by R. Akre & B. Hong
- MTCA .4 system, firmware, software design by Z. Geng
- Infrastructure SW support by C. Xu

# LLRF System Upgrade- Intrapulse Feedback

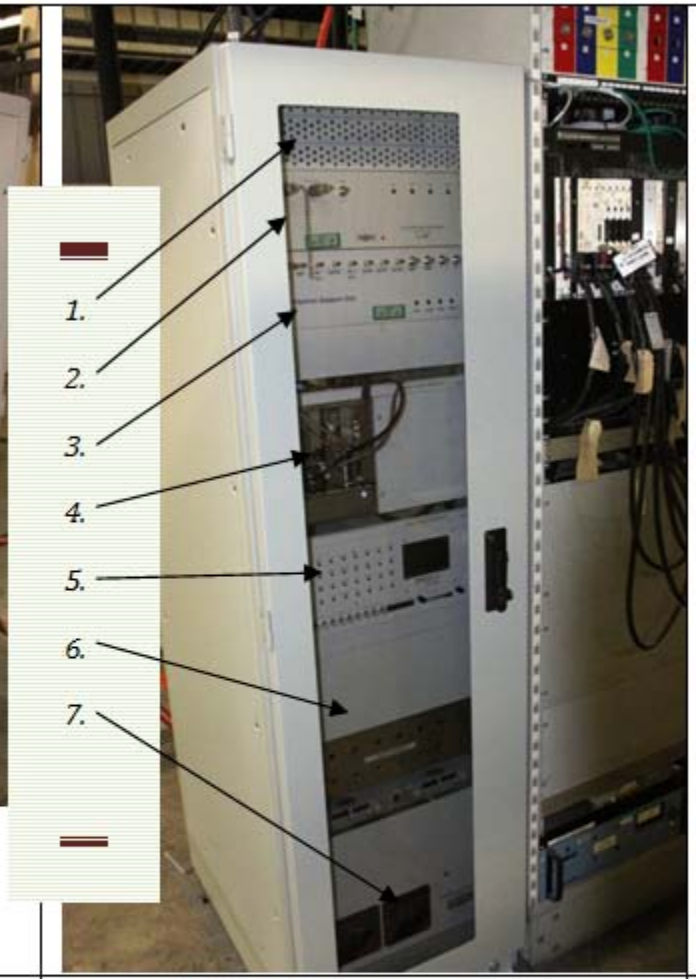


6-Slot Schroff

L to R:

- Power unit
- MCH
- Processor
- ADC-DAC
- Not shown:
- EVR timing receiver on PMC AMC Adapter

Rear Side View Water Stabilized Rack




Front View Next to Fiat Rack

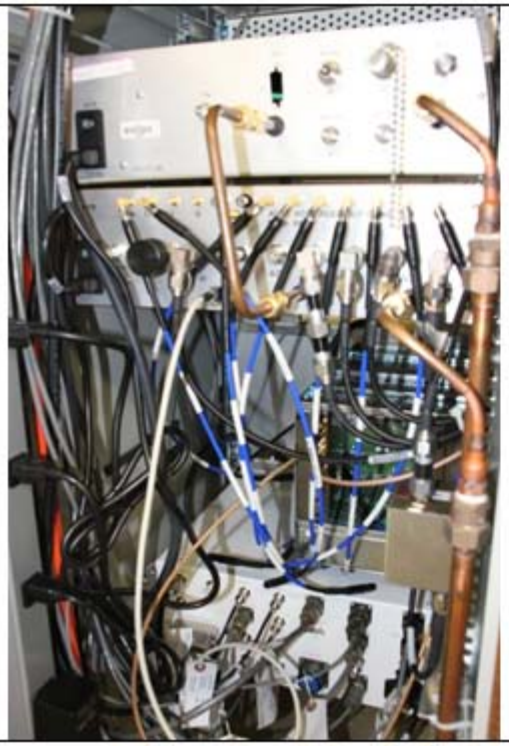
Top to Bottom:

1. Air Return
2. Solid State Sub-Booster
3. RF Front End Chassis
4. MTCA.4 6-Slot Chassis
5. MKSUII
6. Dummy Heat Load (Future Solenoid PS)
7. Air-Water heat Exchanger Air Out

Rear View Door Open
Power & Plumbing
(before cables installed)

Top to Bottom:

1. Solid State Sub-Booster
2. RF Front End Chassis
3. MTCA.4 6-Slot Chassis



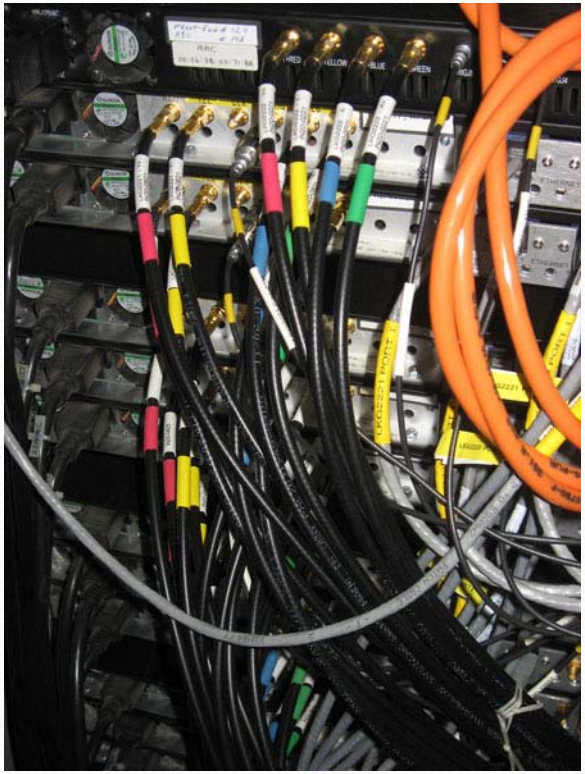
RF Cables, MTCA Installed

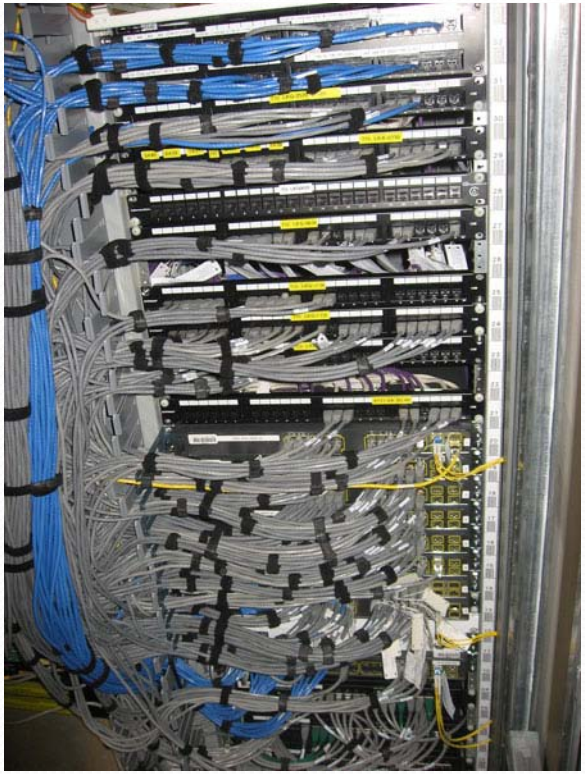
Front View SSSB, RF, MTCA, MKSUII

Flow Meters 2 GPM & 7 GPM

# 2. New BPM Design- Motivation

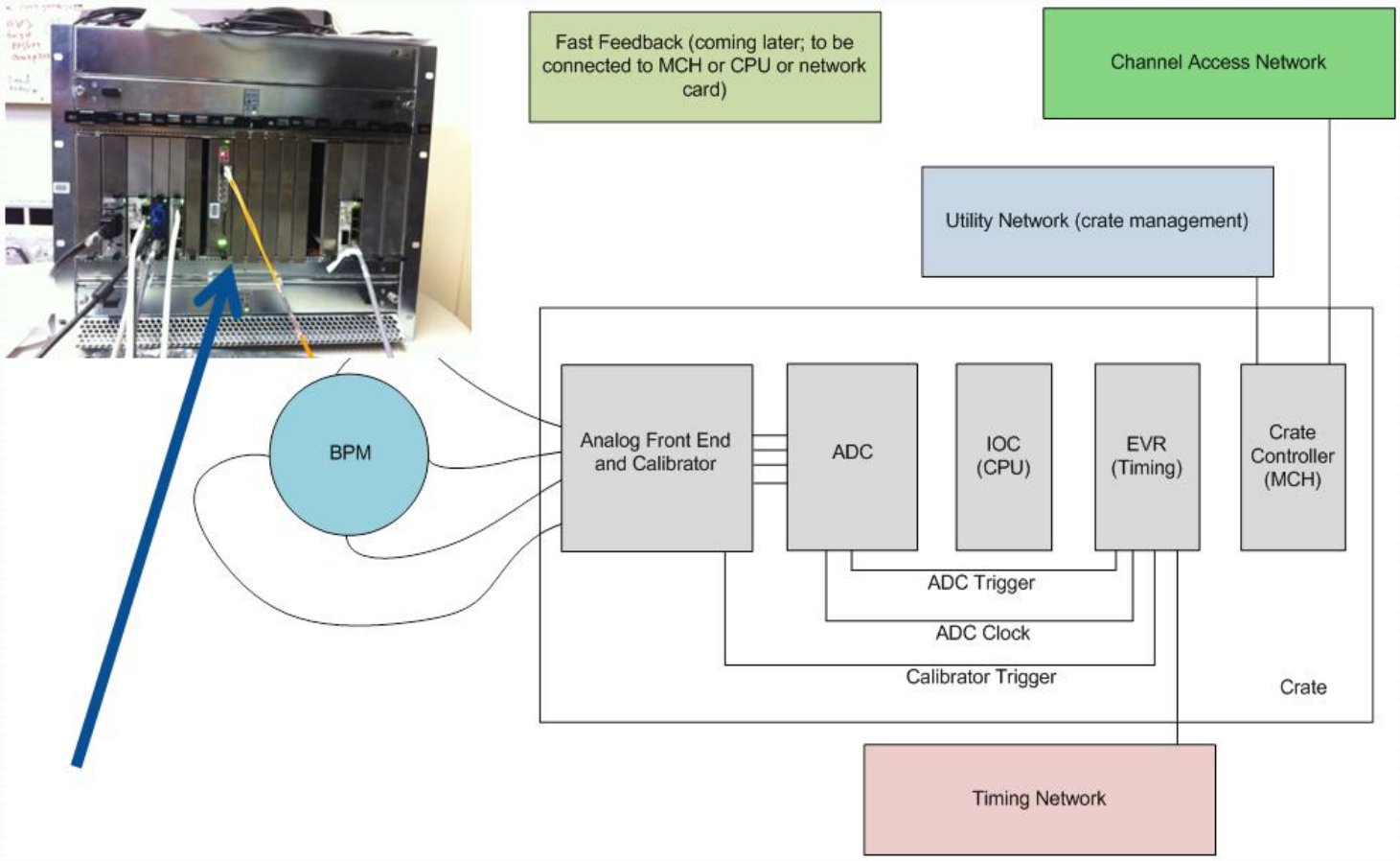
- Nobody likes Pizza Boxes



*Slide courtesy D. van Winkle*

# BPM System Integration

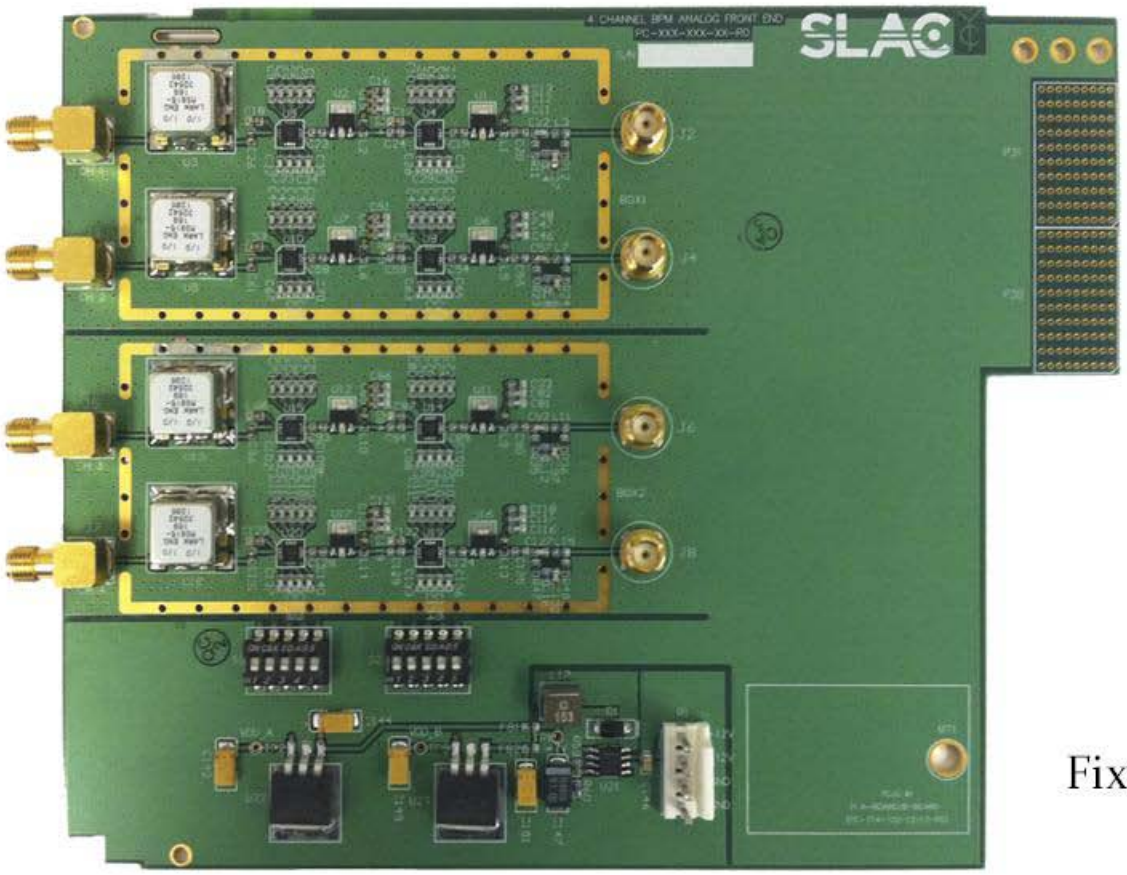



Note:

- EVR to be replaced by Timing Module driving Single backplane trigger line.
- Calibration triggers (2) derived in FPGA of each ADC-DAC
- External network cables (slide 9) reduced to single input trigger line by MTCA.4 backplane

*Slide Courtesy D. van Winkle*

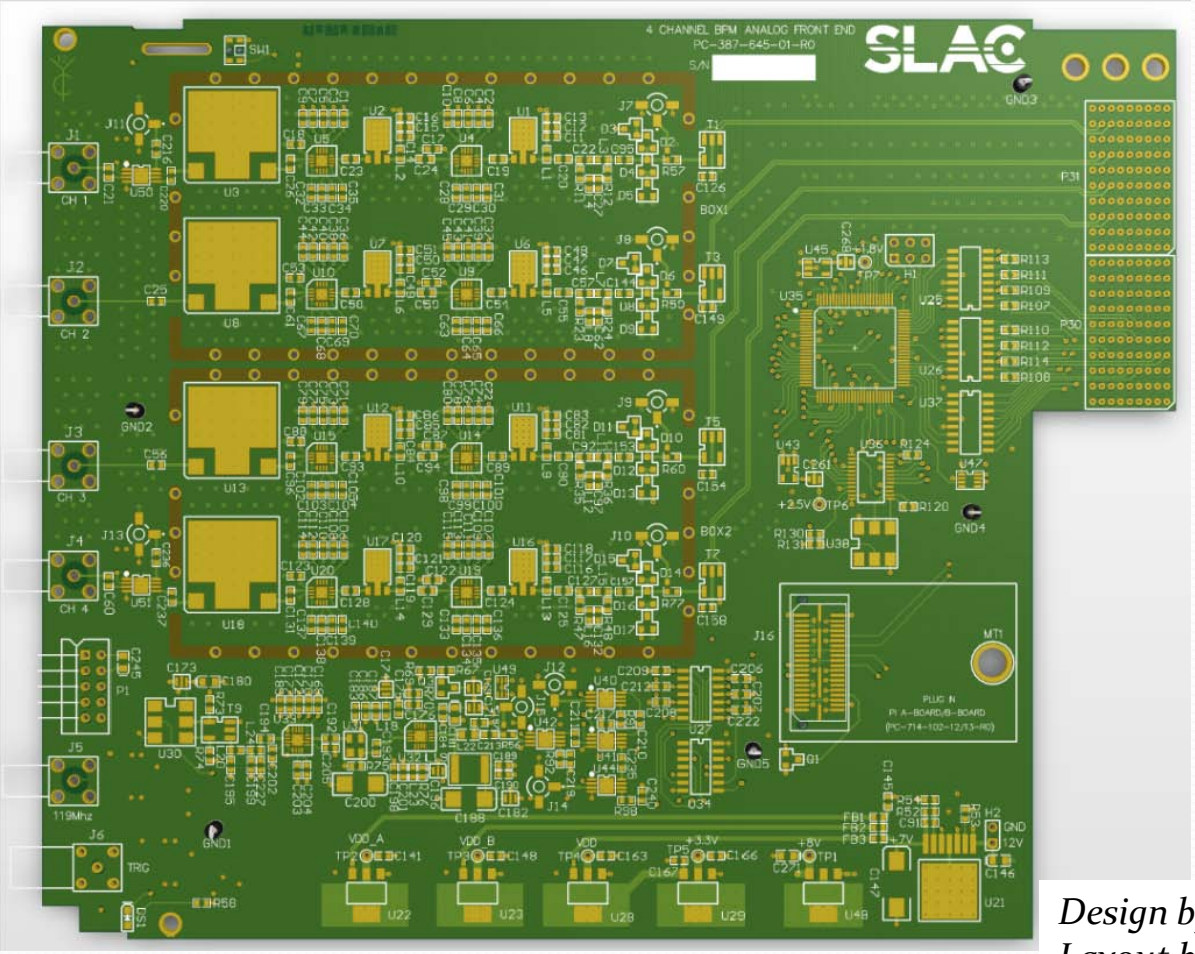
# 4 Ch BPM RTM Prototype Filters




Minor problem uncovered
- Second Filter off freq


Fixed in final design

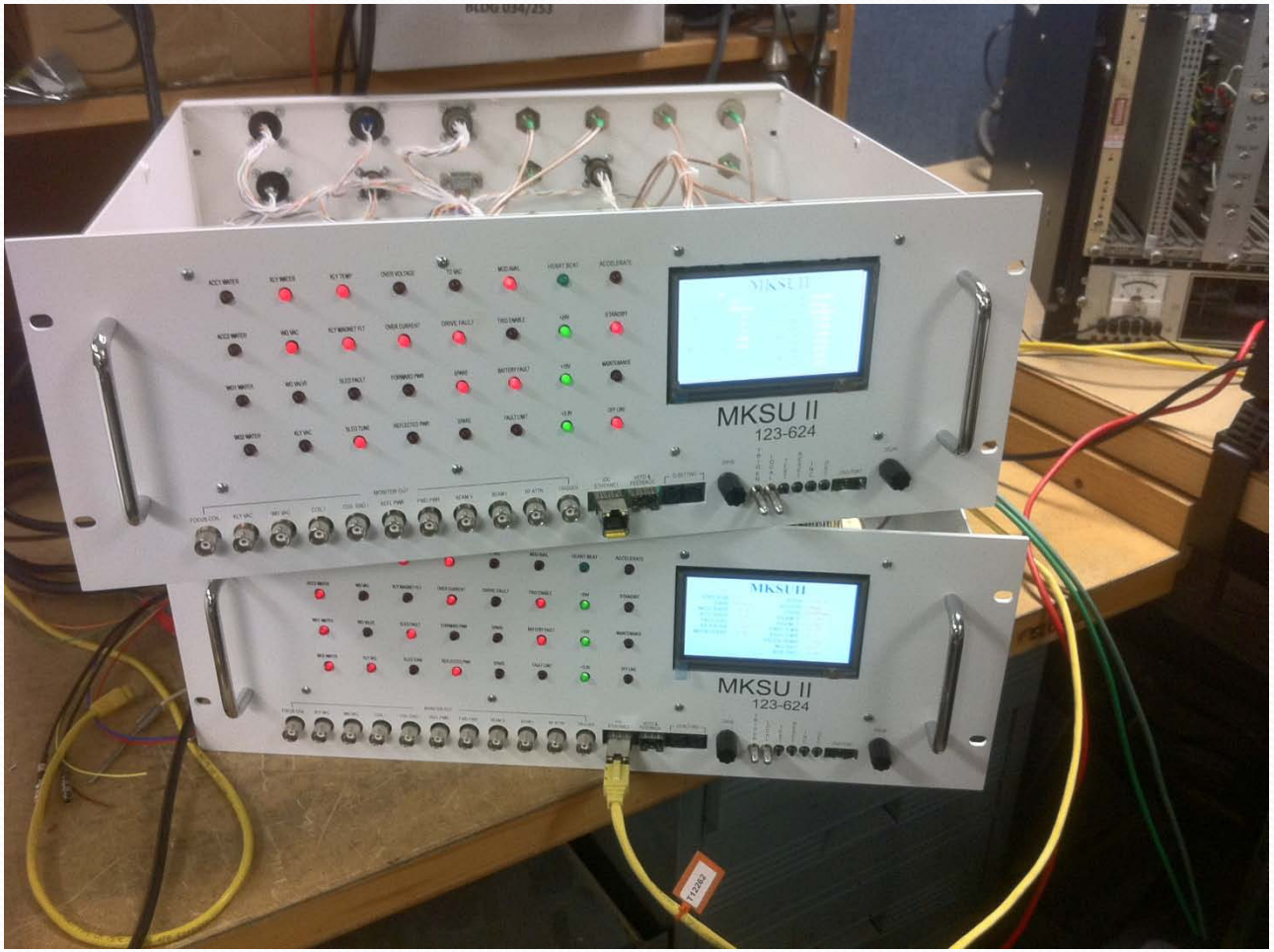
# BPM 4 Ch Final – Out for loading




First unit will sample at 119 MSPS, RF synchronized single beam pulse, ringing signal
Final unit will sample at 238 MSPS, RF synchronized for double pulse (or more)

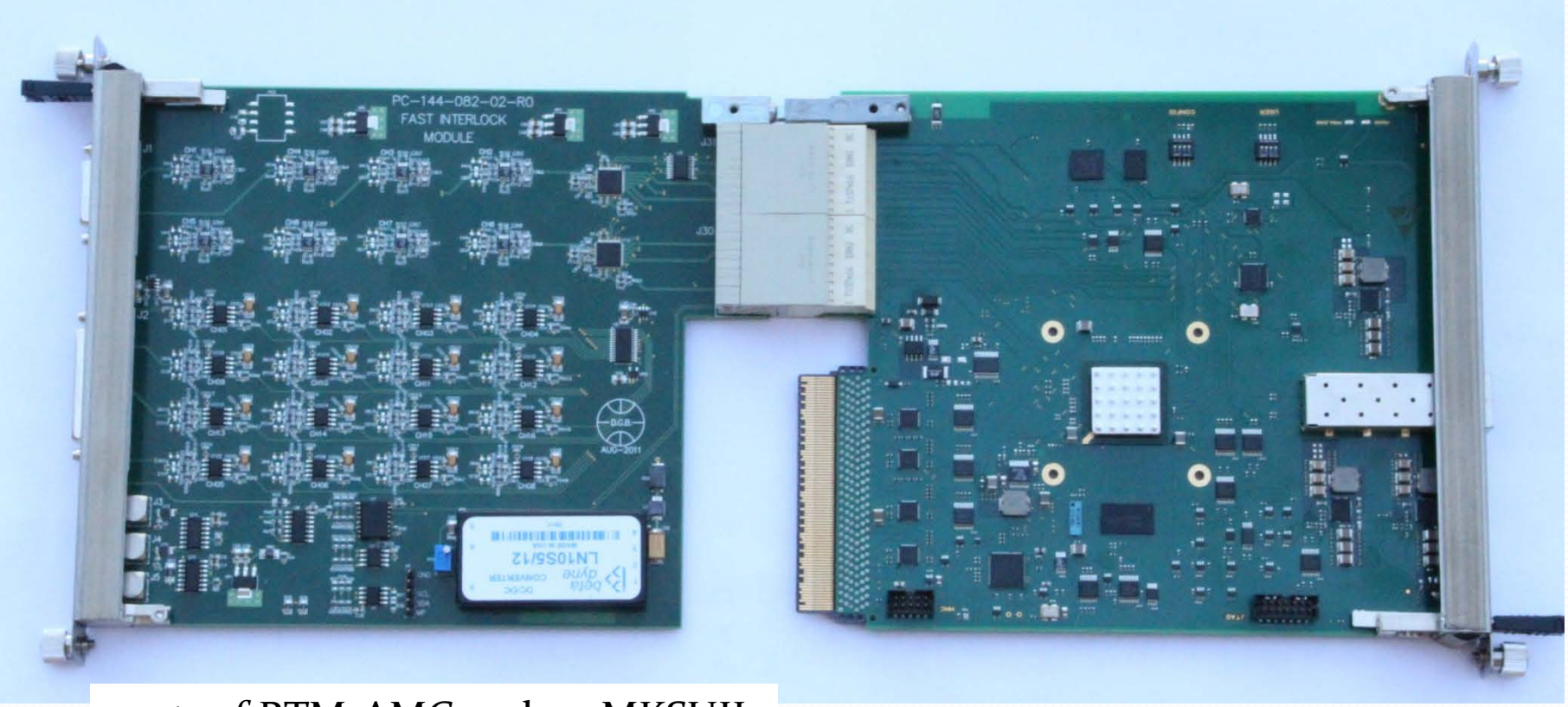
*Design by E. Medvedko, D. van Winkle*
*Layout by C. Yee*

# 3. Klystron Interlock Upgrade




MKSUII
- Latest design
- FPGA interlock formation
- Fast & slow channels
- Front panel LEDs and information screen
- BNC monitors
- Single large board design

# MTCA.4 Design
# Klystron Interlock RTM, FPGA AMC




3 sets of RTM-AMC replace MKSUII
Firmware to be ported from MKSUII

*RTM Fast-Slow ADC Board design by D. Brown*
*Layout by C. Yee*
*TAMC651 by TEWS company*

# Summary

- RF prototype with intra-pulse feedback successfully demonstrated on-beam with SIS8300, 25 MHz IF
  - Further tests planned, aiming for LCLSII Injector install
- BPM RTM in fabrication
  - Will be tested with 125MSPS SIS8300, later with 250 MSPS 4 Ch ADC
- Klystron Interlock system in prototype tests
  - Aiming to test on L-Band system in FY12
  - Firmware, SW to be ported from successful MKSUII design