Silicon pixel and strip detector development for the upgrade of the ALICE Inner Tracking System

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Physics motivations & Design goals

See R. Lemmon's talk 17th August, Parallel 6C: New Experimental Developments

The main physics motivation for the upgrade of the Inner Tracking System of the ALICE experiment is to measure:

- **Quark mass dependence of in-medium energy loss** through
  - Baryon-to-meson ratio for charm (Λ_c/D) and beauty (Λ_b/B) for transverse momentum p_T as low as 2 GeV/*c*
  - Elliptic flow for B and charm and beauty baryons for p_T as low as 2 GeV/*c*
- **Thermalization of heavy quarks in the medium** through
  - Nuclear modification factors of the p_T distributions of D and B mesons separately

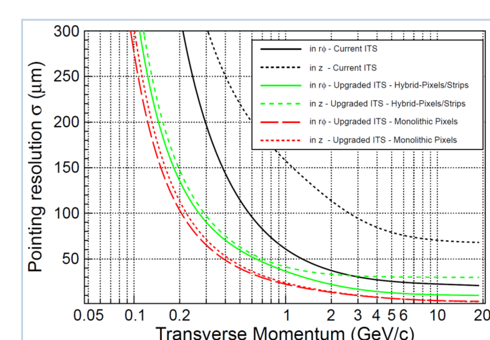
on charm and beauty production in heavy-ion collisions, which address important questions that cannot be answered with the present experimental setup. The target for the ITS Upgrade is the second long LHC shutdown (LS2), which is at the moment planned for 2017-2018

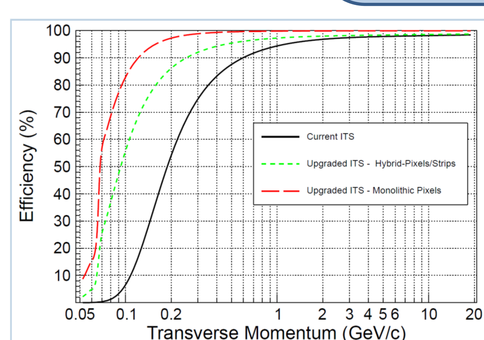
Design goals

- Reconstruct displaced decay vertices
- Track charged particles with high resolution at all momenta
- Identify charged particles down to low transverse momentum

Required improvements

- Impact parameter resolution (factor 3 @1 GeV/*c*)
- Standalone tracking efficiency (> 95% @0.2 GeV/*c*)
- Transverse momentum resolution
- Capability to handle 1 Mrad per year, 150 hits/cm²
- Interaction rates: 50 kHz in Pb-Pb
- Particle identification capability





Comparison current ITS - upgraded ITS in simulation

Left: Pointing resolution as a function of p_T: a factor 3 improvement can be achieved in rφ with respect to the present performance

Right: Tracking efficiency for charged pions as a function of p_T: at 0.2 GeV/c a tracking efficiency >95% can be achieved using monolithic pixel detectors, > 85% using hybrid pixel and microstrip detectors, compared to the present ~55%

Detector requirements & Technology options

Targets for Inner Layers (1, 2, 3)

- $r\varphi$ & z spatial precision: 4 μm
  - Pixel size ($r\varphi$, z): 20-30 , 20-50 μm
- Material budget per layer: 0.3-0.5% X_0
  - 0.1% X_0 under study for Layer 1
- Radiation env: 1 Mrad/1.6·10¹³ n_{eq} per year
- Granularity: 150 cm⁻² particle density

→ Monolithic Pixels, Hybrid Pixels

Targets for Outer Layers (4, 5, 6, 7)

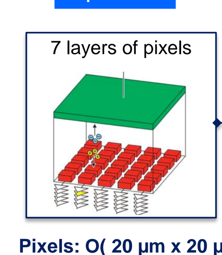
- $r\varphi$ spatial precision: < 20 μm
  - Larger pixel size
  - Strip pitch 95 μm, stereo angle 35 mrad
- Material budget per layer: 0.5-0.8% X_0
- Radiation env: 10 krad/ 3*10¹¹ n_{eq} per year
- Granularity: 2 cm⁻² particle density
- Low cost per m²

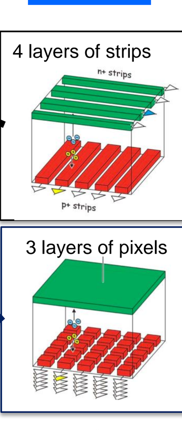
→ Monolithic Pixels, Microstrips

Two layout options

A. 7 layers of monolithic pixel detectors
- Better standalone tracking efficiency and transverse momentum resolution
- Worse PID or no PID

B. 3 innermost layers of hybrid pixel + 4 layers of micro strip detectors
- Worse standalone tracking efficiency and transverse momentum resolution
- Optimal PID

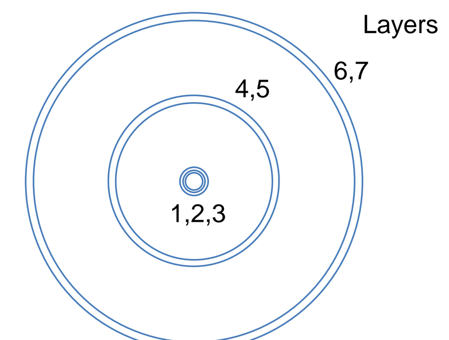




ITS Upgrade geometry

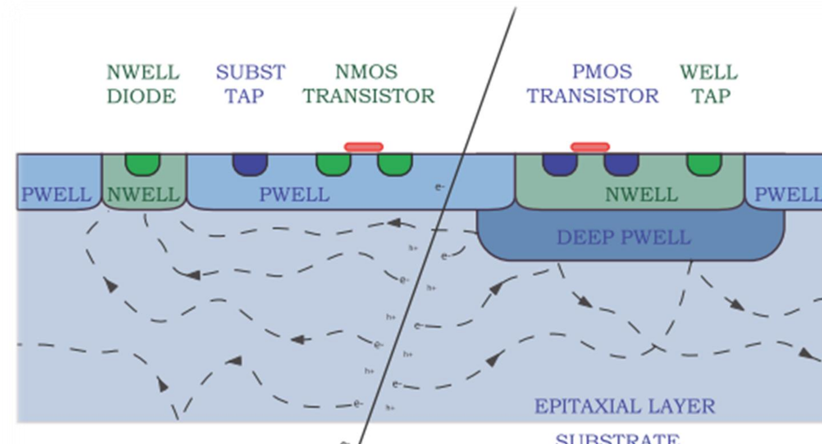
- **Beam pipe** outer radius reduced to 19.8 mm, wall thickness to 0.5 mm
- **First detection layer** close to the beam pipe: r_1 =22 mm
- Increase **radial extension** 22-430 mm
  - Increasing the outermost radius to 500 mm would result in a 10% improvement in transverse momentum resolution
- Layers are **grouped**: (1,2,3) (4,5) (6,7)
- **η coverage**: ±1.22 over 90% of luminous region → z dimension

Layer	Radius [cm]	± z
1	2.2	13.5
2	2.8	13.5
3	3.6	13.5
4	20	39.0
5	22	41.8
6	41	71.2
7	43	74.3



Monolithic Pixel Technology

Deep p-well 0.18 μm CMOS technology



The presently preferred technology uses a process available at Tower/Jazz* in 0.18 μm CMOS, which includes the so-called «deep p-well». In standard monolithic active pixels (MAPS) the detecting element is formed by a reverse bias diode whose terminals are an n-well and the substrate.acts as the collecting electrode. A deep p-well is placed underneath the PMOS n-wells, screening them: the charge is focused towards the collecting electrode.

* TOWER/JAZZ, http://www.jazzsemi.com/

Features

- All-in-one: detector-connection-readout
- Moderate resistivity (~1 kΩ·cm) epitaxial sensor included in ASIC chip
- Small pixel size: 20 μm x 20 μm
- Small material budget: 0.3% X_0 per layer
- Low cost

Options under study

- **Deep p-well 0.18 μm CMOS**
  - MIMOSA series
  - ARACHNID INMAPS
- **90 nm CMOS technology**
  - LePIX prototypes
    - 90 nm CMOS technology
    - Charge collection by drift
    - Large Signal-to-Noise ratio
    - Prototypes under study

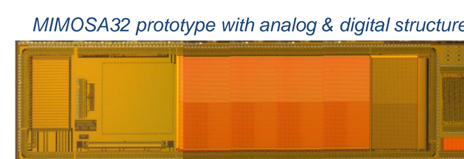
Under evaluation

- Radiation hardness
- Power consumption

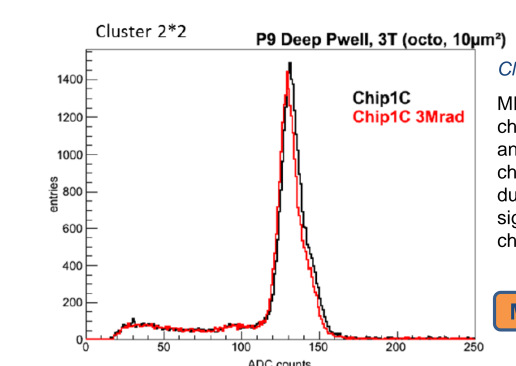
Deep p-well prototypes and tests

MIMOSA series (IPHC Strasbourg - Tower/Jazz): deep p-well with rolling-shutter readout

- Following development for STAR HFT:
  - 10x improvement in radiation tolerance thanks to 0.18 μm technology
  - Reduced readout time thanks to double-sided rolling shutter (but increased power dissipation)
- Continuous charge collection mostly by diffusion inside the pixel
- Pixel matrix are read periodically row by row: column parallel readout with end-of-column discriminators
- Integration time = readout period < 10 μs achievable with double-sided/submatrix rolling-shutter readout
- Target power dissipation: < 250 mW / cm²



MIMOSA32 prototype with analog & digital structures

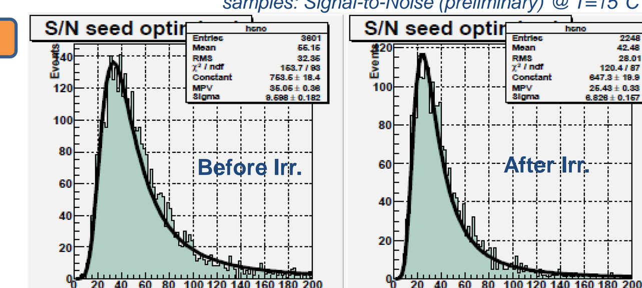


Cluster charge collected after 3 Mrad TID (preliminary)

MIMOSA32 irradiation with 5.9 keV X-Rays from ⁵⁵Fe: charge collected in the set of 4 pixels in a cluster before and after 3 Mrad TID. The cluster collect most of the charge confirming the limited diffusion of the charges due to the high-resistivity of the epitaxial layer. No significant degradation is observed in noise, S/N and charge collection efficiency

M. Winter et al.

1 Mrad & 10¹³neq/cm² combined irradiation of 20x20 mm pixel samples: Signal-to-Noise (preliminary) @ T=15°C



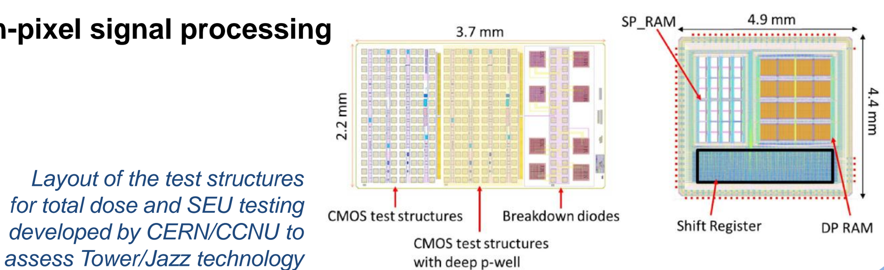
M. Winter et al.

1 Mrad & 10¹³neq/cm²	S/N	Detection efficiency
Before irradiation	35.05 ± 0.36	99.97 ± 0.03 %
After irradiation	25.43 ± 0.33	99.69 ± 0.12 %

ARACHNID INMAPS (RAL UK - Tower/Jazz): deep p-well with in-pixel signal processing

- Matrix is read only upon trigger request → low power consumption
- Good S/N with low sensor capacitance (~fF)
- Pixel size limited by the included logic (30 μm x 30 μm)
- R&D activities:
  - Irradiation tests on existing structures
  - Reduce power consumption exploiting detector duty cycle (5%)
  - Develop fast read-out system

Layout of the test structures for total dose and SEU testing developed by CERN/CCNU to assess Tower/Jazz technology



Hybrid Pixel Technology

Features

- CMOS chip + high resistivity (~80 kΩ·cm) sensor
- Bump-bonding connections
- Charge collection by drift: high S/N > 50
- Well known technology

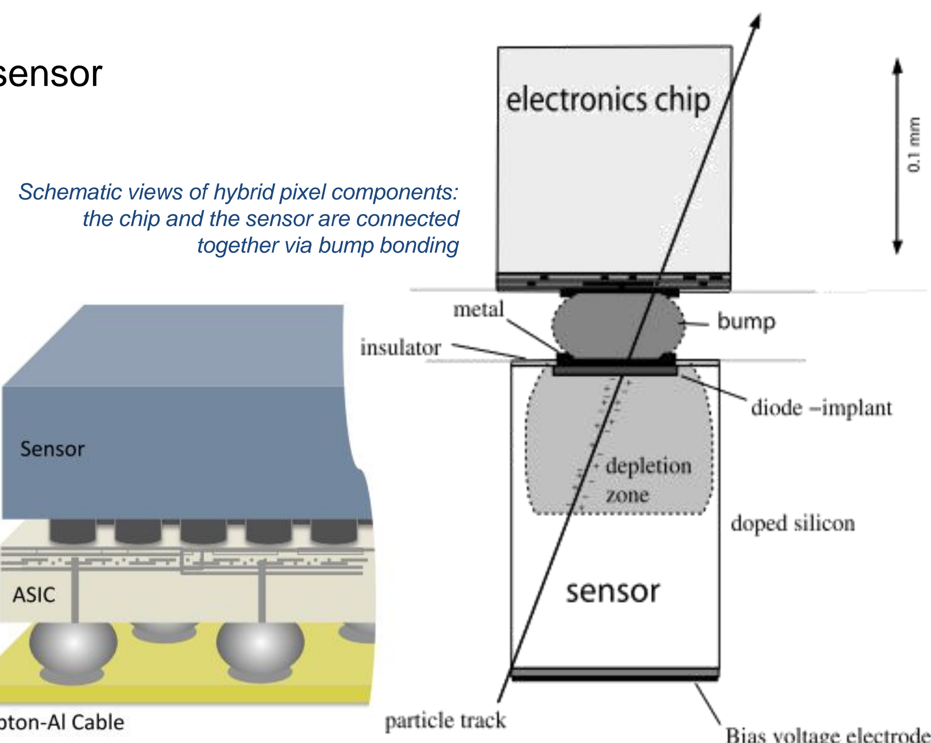
Disadvantages

- Larger material budget: 0.5% X_0 target
- Larger pixel size: 30 μm x 30 μm target
- High cost per m² for fine pitch bonding

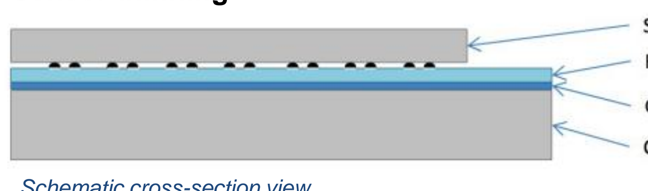
R&D focused on:

- Sensor thinning
- Edgeless sensors
- Low cost bump-bonding
- Low power FEE chips

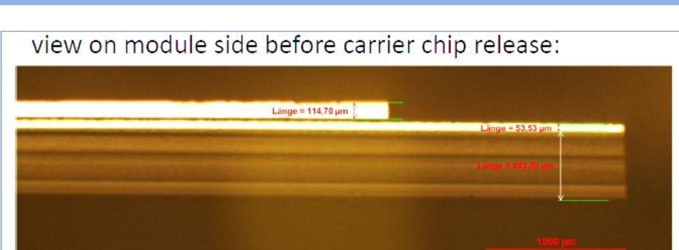
Schematic views of hybrid pixel components: the chip and the sensor are connected together via bump bonding



Sensor thinning



Schematic cross-section view



Sensor 100 μm, readout chip 50 μm, glass carrier 300 μm

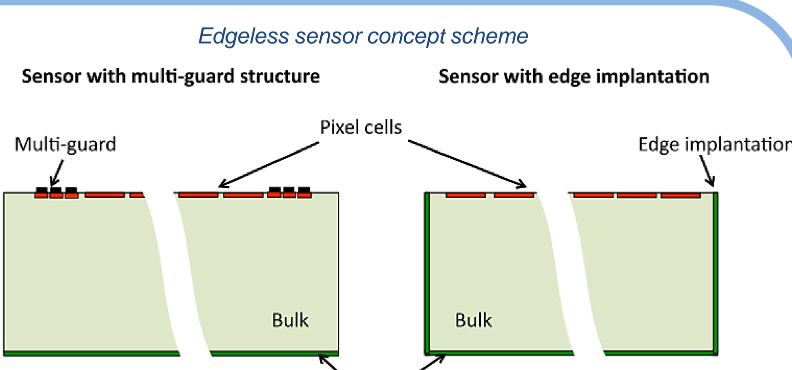
The target thickness is 100 μm for the sensor and 50 μm for the chip, corresponding to ~0.5 % X_0. Single- and multi- chip assemblies with dummy components have been produced and thinned down to the required thickness at IZM**. After thinning, the glass carrier is removed.

** Fraunhofer Institute for Reliability and Microintegration (IZM), Dept. High Density Interconnect and Wafer Level Packaging, Berlin

Edgeless sensors

- **Idea:** reduce the inactive edge region from ~600 μm to 10-100 μm by introducing a highly n-doped trench
- **Advantage:** reduce the inactive region which only adds material
- **Technical challenge:** etching the trench and post-processing the wafers for bumping and thinning
- **First prototypes** realized by FBK*** Trento with SPD geometry: high resistivity epitaxial layer with edgeless design, deposited on a carrier wafer
- **Test structures** with and without guard rings, trench at different distances from the pixels to optimize the layout (depletion, V_{bd})

Edgeless sensor concept scheme

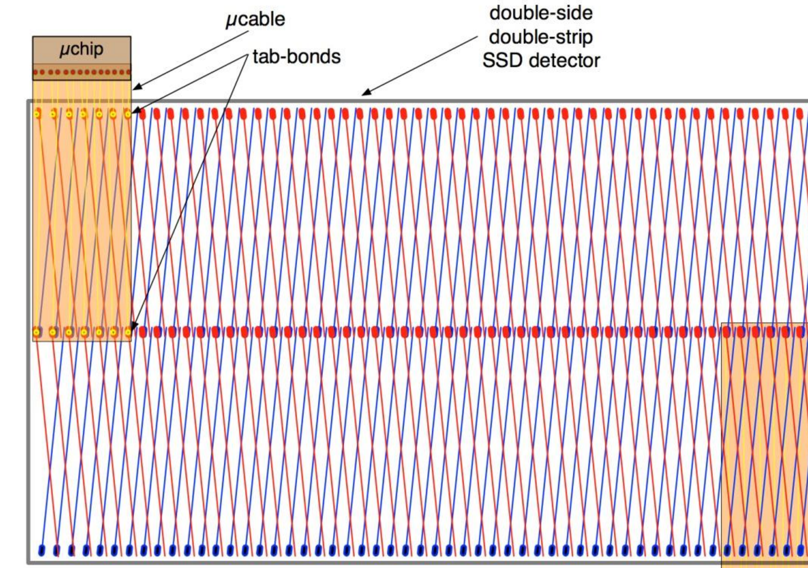


*** Fondazione Bruno Kessler, Trento, Italy, www.fbk.eu

Microstrip Technology

Features

- Low power consumption
- Optimal PID capability
- Good $r\varphi$ spatial precision (< 20 μm)
- Low power consumption
- Robust and mature technology



Schematic view of the new sensor layout: two rows of 768 strips are arranged on each side (in red and blue for the front and back side). The dots represent the corresponding bonding pads

Module concept

- Based on present SSD with shorter strips:
  - 300 μm double-sided sensor (7.5 cm x 4.2 cm)
  - 35 mrad stereo-angle between p- and n-side strips
  - Reduced strip length down to 20 mm
- New design advantages:
  - Half cell-size: ~ 95 μm x 20 mm
  - Higher granularity
  - >95% ghost hit rejection efficiency
  - Lower strip C: higher S/N
- Drawbacks:
  - Double number of interconnections
  - Bonding at very low pitch
  - Increased power consumption

R&D activities

- Small pitch micro-cable development
- Assembly procedure validation

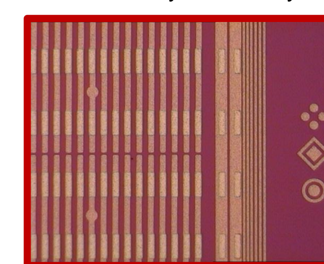
Interconnection cables R&D

- Micro-cables in aluminum trace on polyimide layer
- Very low material budget: 10 μm + 10 μm
- Very flexible
- Trace pitch: 42.5 μm (chip side) / 47.5 μm (sensor side)
- Length: ~ 25 mm / ~ 50 mm
- First prototypes in 2 versions, hosting 128/256 channels

First microcable prototype with 42.5 μm inter-trace pitch (SE SRTIIE - Kharkov, UA)

Assembly and folding

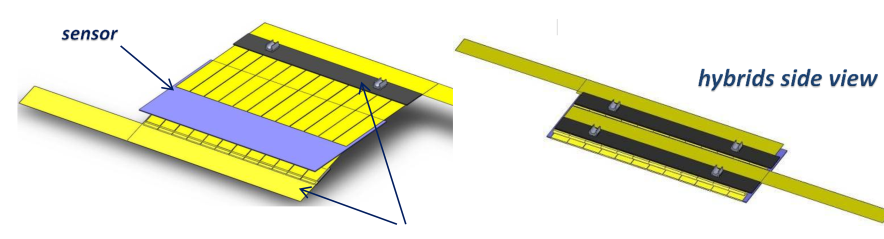
- Tape-Automatic Bonding (TAB) technique:
  - Allows chip tests, less material, safe folding
  - Challenging at trace pitch < 50 μm
- Assembly of dummy components under test



Dummy strip sensor detail: the horizontal gap halving the strip length is visible (INFN Trieste - FBK Trento)

First aluminum-polyimide cable bonded to a dummy chip via TAB technique (SESRTIIE, UA)

- Compact module layout procedure
  - 12 tabbed chips are bonded to a hybrid circuit providing connections and cooling
  - The cables are also bonded on each side of the sensor
  - The cables are then folded around the sensor



Schematic view of the strip module after bonding the hybrids on the sensor (left) and after folding the cables around the sensor edge (right)