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Radiation-Hard High-Speed Parallel Optical Links

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We have designed two ASICs for possible applications in the optical links of a new layer of the ATLAS pixel detector for the initial phase of the LHC luminosity upgrade. The ASICs include a high-speed driver for a VCSEL and a receiver/decoder to extract the data and clock from the signal received by a PIN diode. Both ASICs contain 12 channels for operation with a VCSEL or PIN array. Among these channels, the outer four channels are designated as spares to bypass a broken PIN or VCSEL within the inner eight channels. The ASICs were designed using a 130 nm CMOS process to enhance the radiation-hardness. With the spacing of 250 μm between two VCSEL or PIN channels, the width of an optical array is only 3 mm. This allows the fabrication of compact parallel optical engine for installation at a location where space is at a premium. The fabricated receiver/decoder properly decodes the bi-phase marked input stream with no bit error at low PIN current. The performance of the VCSEL driver at 5 Gb/s is satisfactory. We are able to program the ASICs to bypass a broken PIN or VCSEL and the power-on reset circuits have been successfully implemented to set the ASICs to a default configuration in an event of communication failure. We have irradiated the receiver/decoder to high dose and observe no significant degradation and the SEU rate is low. We plan to irradiate the VCSEL drivers in the summer to measure the radiation hardness. We will present results from the study at the conference. In addition, we will briefly present the status of the design of a new VCSEL driver ASIC to operate at 10 Gb/s which will yield an aggregated bandwidth of 120 Gb/s for a fiber ribbon.

Summary

The LHC at CERN is now the highest energy and luminosity collider in the world. To enhance the physics potential, the ATLAS experiment plans to add a new pixel layer to the current pixel detector during the 2013 shutdown. The optical data transmission system will also be upgraded to handle the higher data transmission speed. Two ASICs have been prototyped for this new generation of optical links to incorporate the experience gained from the current system. The ASICs include a high-speed driver for a VCSEL and a receiver/decoder to extract the data and clock from the signal received by a PIN diode. Both ASICs contain 12 channels for operation with a VCSEL or PIN array. The outer four channels are designated as spares to bypass a broken PIN or VCSEL within the inner eight channels. The ASICs were designed using a 130 nm CMOS process to enhance the radiation-hardness. With the spacing of 250 μm between two VCSEL or PIN channels, the width of an optical array is only 3 mm. This allows the fabrication of compact parallel optical engine for installation at a location where space is at a premium.

Each of the receiver/decoder circuits includes pre-amplification, a bi-phase mark clock/data recovery circuit, and LVDS outputs for both the clock and data. In order to allow remote control of the chip, the ASIC includes command decoders that have been designed to be single event upset (SEU) tolerant. All latches are based on a dual interlocked storage cell (DICE) latch to enhance the SEU tolerance. The driver ASIC is designed to operate at 5 Gb/s. Each channel has an LVDS receiver, an 8-bit DAC, and a VCSEL driver. The 8-bit DAC is used to set the VCSEL modulation current. Both ASICs contain multiplexer networks to bypass a broken PIN or VCSEL. To enable operation in case of a failure in the communication link to the command decoder, we have included a power on reset circuit that will set the ASICs to its default 1:1 signal routing state and the VCSEL modulation current to 10 mA.

The fabricated receiver/decoder properly decodes the bi-phase marked input stream with no bit error at low PIN current. The performance of the VCSEL driver at 5 Gb/s is satisfactory. We are able to program the ASICs

to bypass a broken PIN or VCSEL and the power-on reset circuits have been successfully implemented. We have irradiated the receiver/decoder with 24 GeV/c protons to a dose of 1.13x10ˆ15 p/cmˆ2 (30 Mrad) and observe no significant degradation and the SEU rate is low. We plan to irradiate the VCSEL drivers in the summer to measure the radiation hardness. We will present results from the study at the conference. In addition, we will briefly present the status of the design of a new VCSEL driver ASIC to operate at 10 Gb/s which will yield an aggregated bandwidth of 120 Gb/s for a fiber ribbon.

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