

Beam Collision Feedbacks

for future Lepton Colliders

Philip Burrows

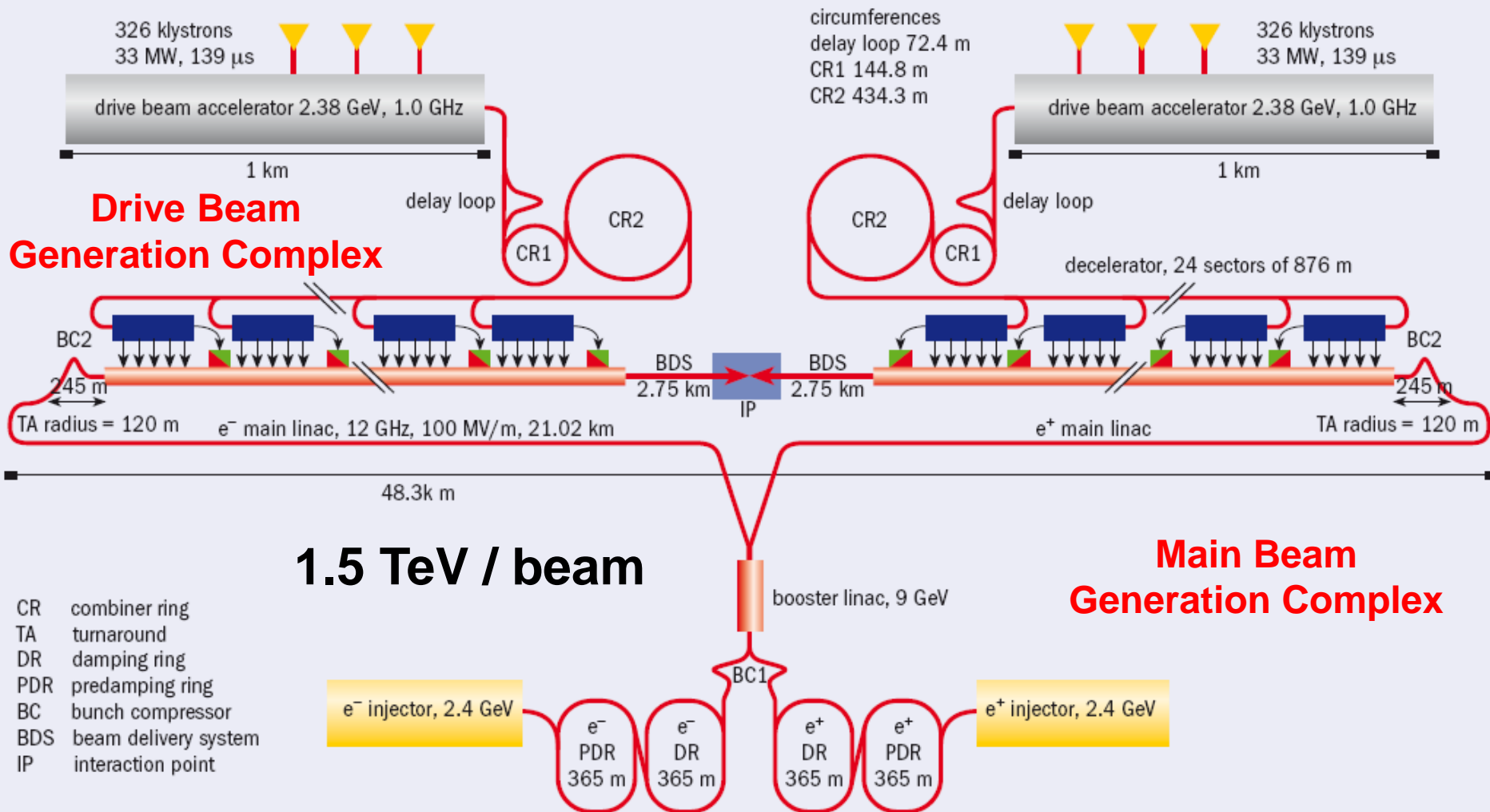
John Adams Institute

Oxford University

Outline

- **Introduction and system concept**
- **ILC design status**
- **CLIC design status**
- **FONT prototype systems performance**
- **Outstanding technical issues**
- **Summary**

Compact Linear Collider (CLIC)



Beam parameters

	ILC (500)	CLIC (3 TeV)	
Electrons/bunch	0.75	0.37	10**10
Bunches/train	2820	312	
Train repetition rate	5	50	Hz
Bunch separation	308	0.5	ns
Train length	868	0.156	us
Horizontal IP beam size	655	45	nm
Vertical IP beam size	6	0.9	nm
Longitudinal IP beam size	300	45	um
Luminosity	2	6	10**34

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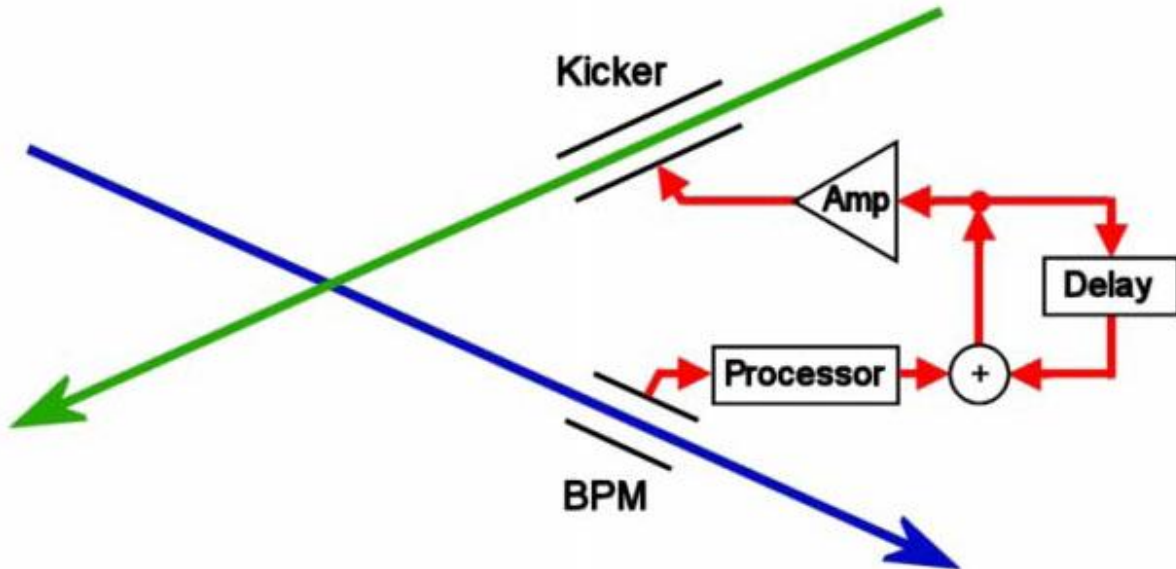
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IP beam feedback concept

Last line of defence
against relative
beam misalignment

Measure vertical
position of outgoing
beam and hence
beam-beam kick
angle

Use fast amplifier and
kicker to correct
vertical position of
beam incoming to IR



FONT – Feedback On Nanosecond Timescales

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General considerations

Time structure of bunch train:

ILC (500 GeV): c. 3000 bunches w. c. 300 ns separation

CLIC (3 TeV): c. 300 bunches w. c. 0.5 ns separation

Feedback latency:

ILC: O(100ns) latency budget allows **digital** approach

CLIC: O(10ns) latency requires **analogue** approach

Recall speed of light: $c = 30 \text{ cm / ns}$:

FB hardware should be close to IP (especially for CLIC!)

Two systems, one on each side of IP, allow for redundancy

IP FB Design Status: ILC

Conceptual design documented in ILC RDR (2007):

1. IP position feedback:

beam position correction up to ± 300 nm vertical at IP

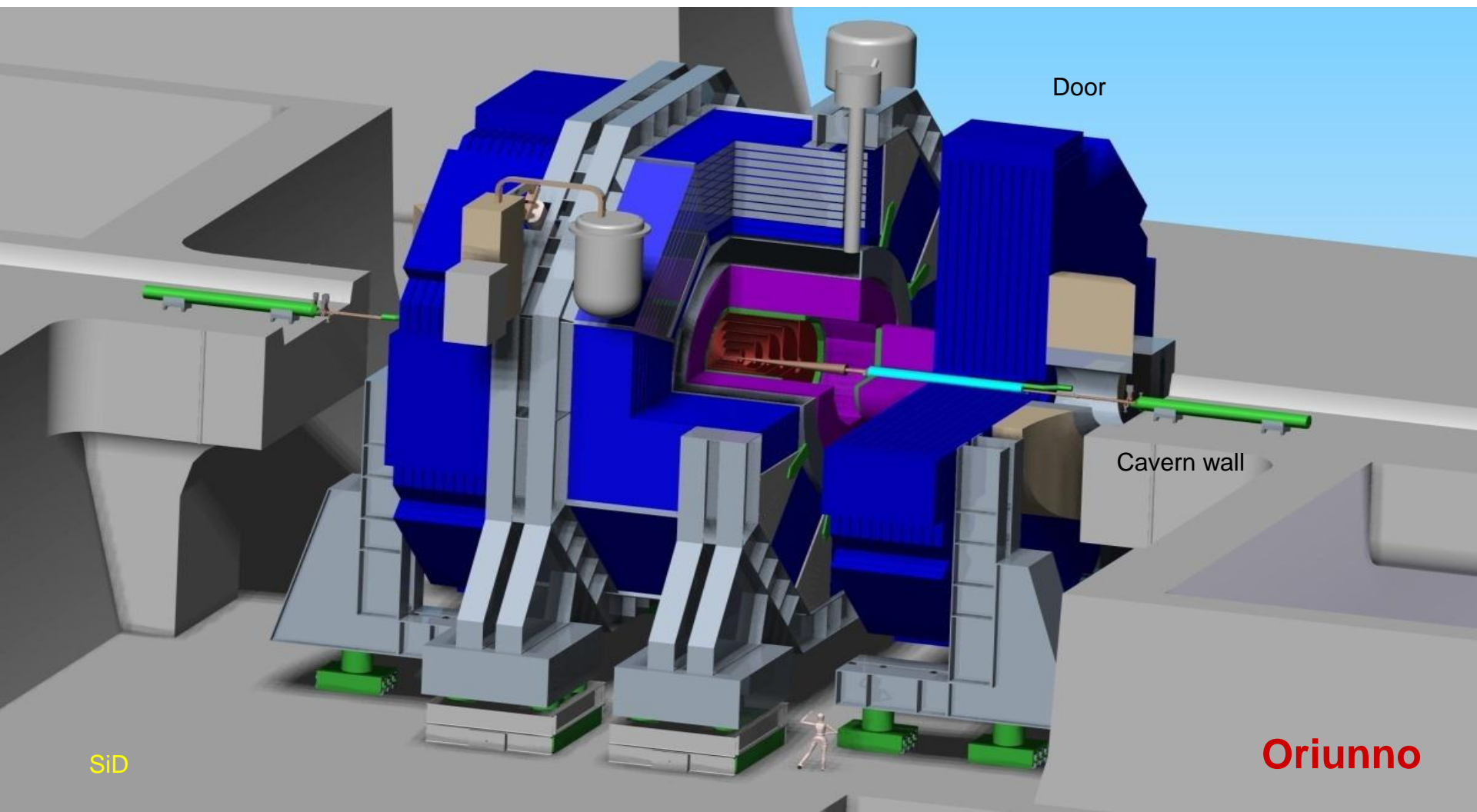
**2. IP angle feedback: hardware located few 100 metres upstream
conceptually very similar to position FB, less critical**

3. Bunch-by-bunch luminosity signal (from BEAMCAL)

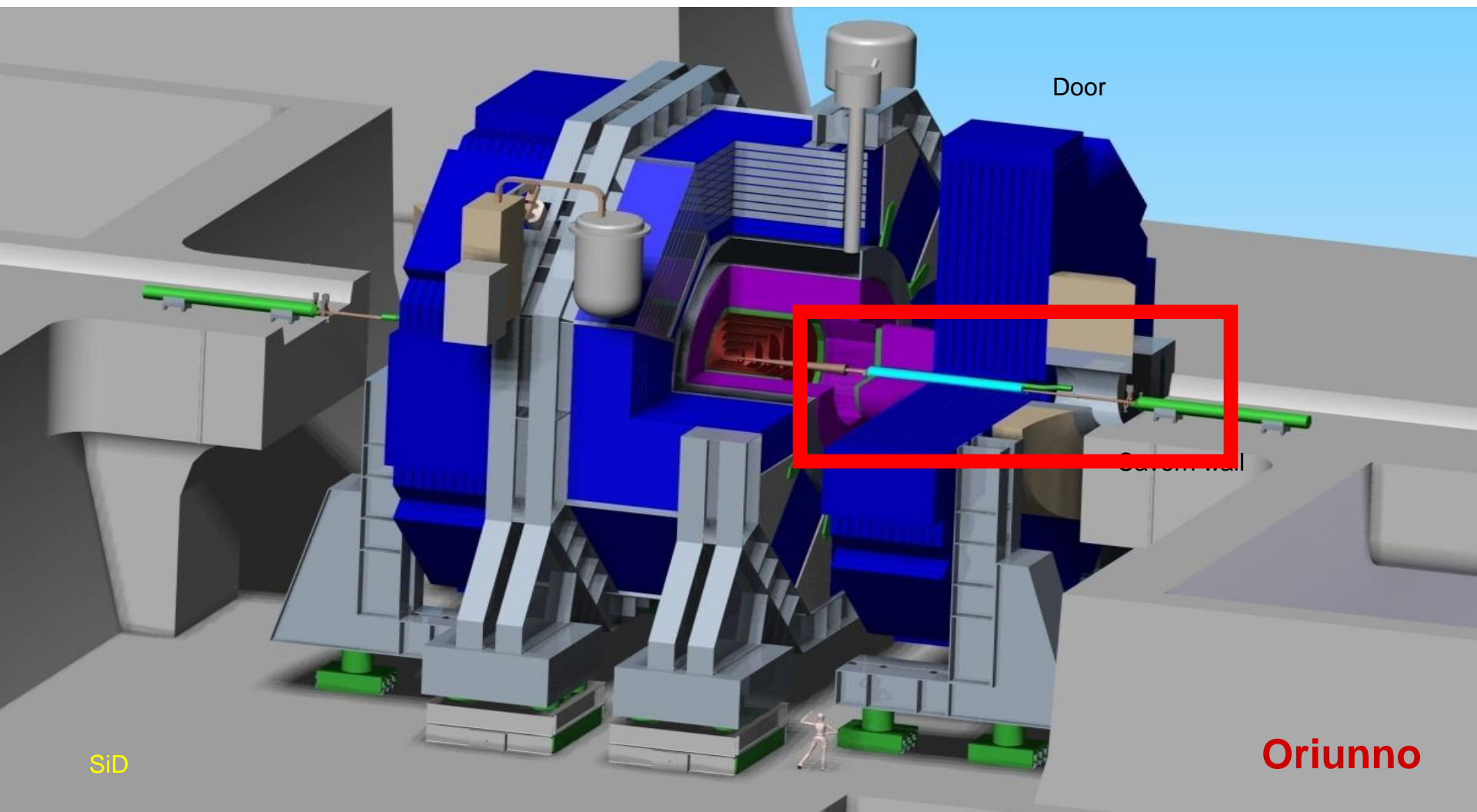
‘special’ systems requiring dedicated hardware + data links

More realistic engineering design in progress for TDP report (2012)

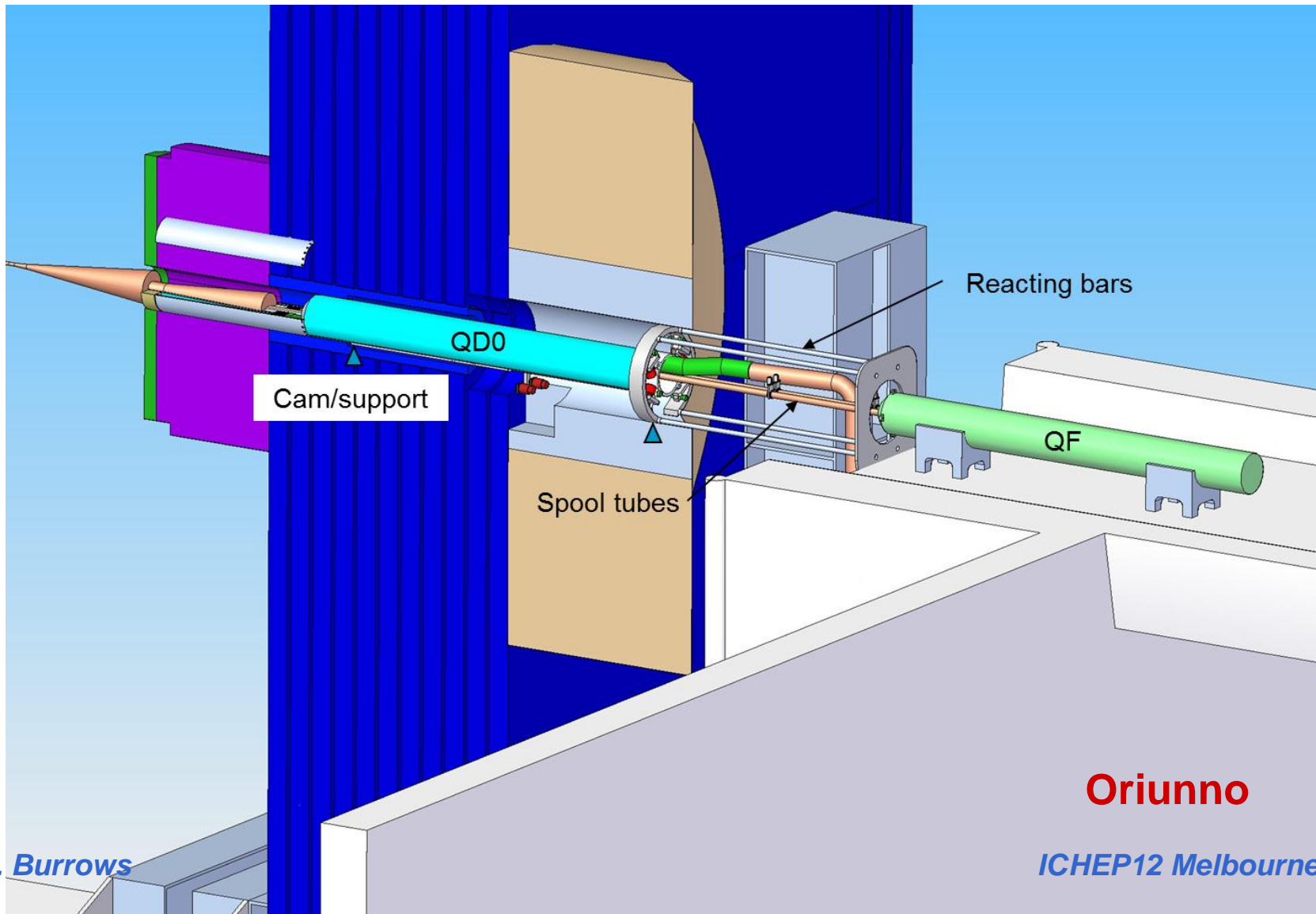
ILC IR: SiD for illustration



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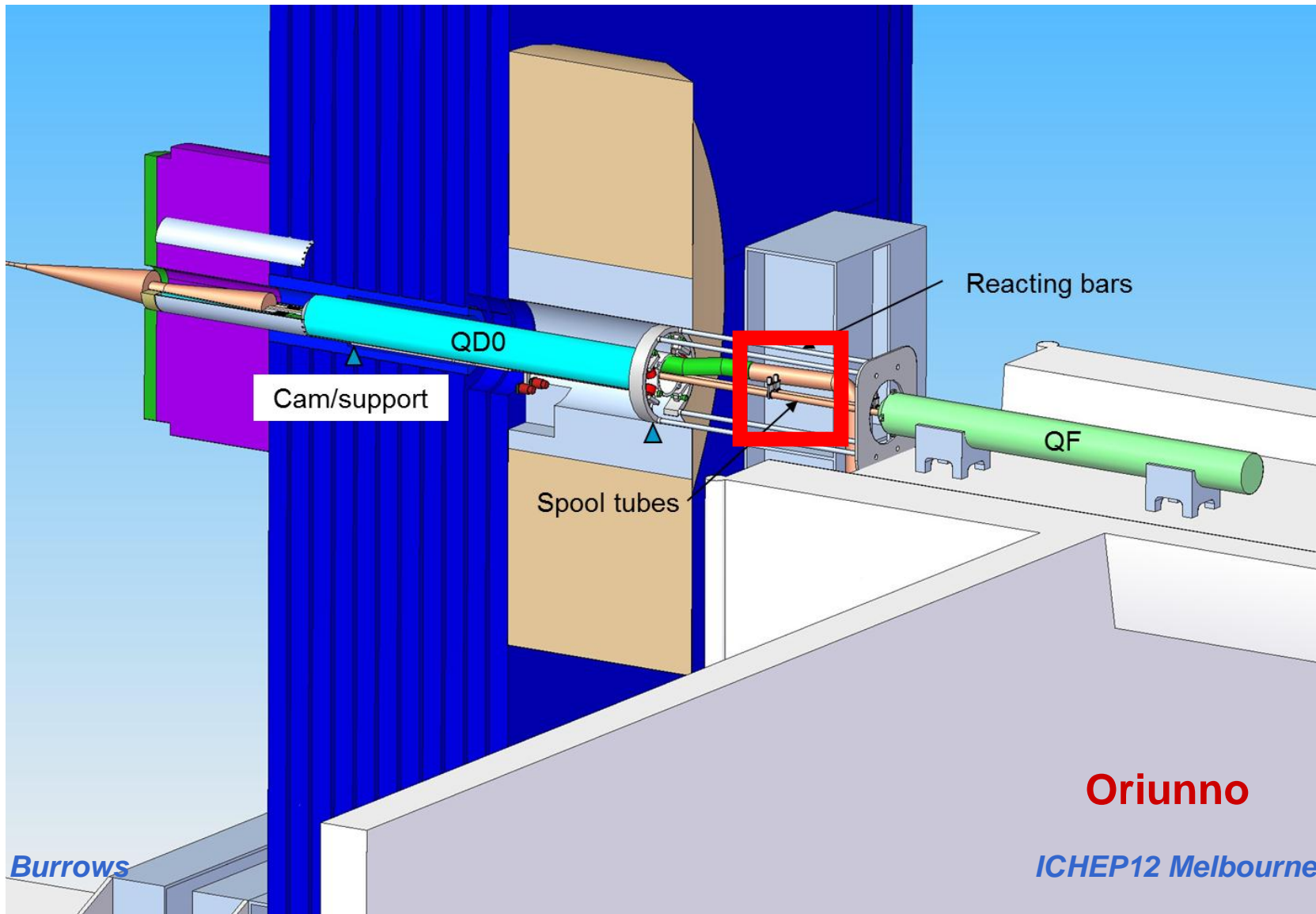


Final Doublet Region (SiD)



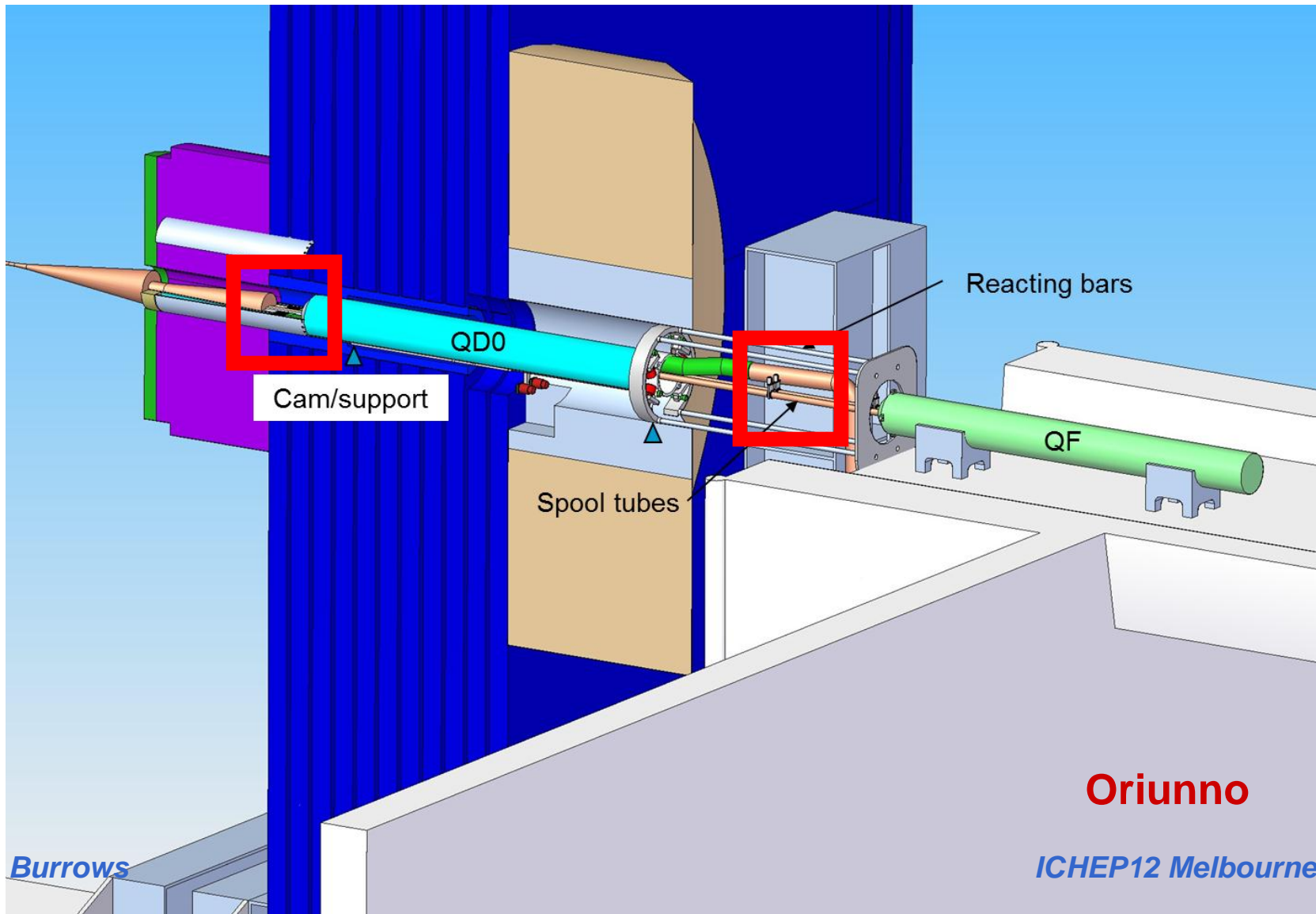
Oriunno

Final Doublet Region (SiD)

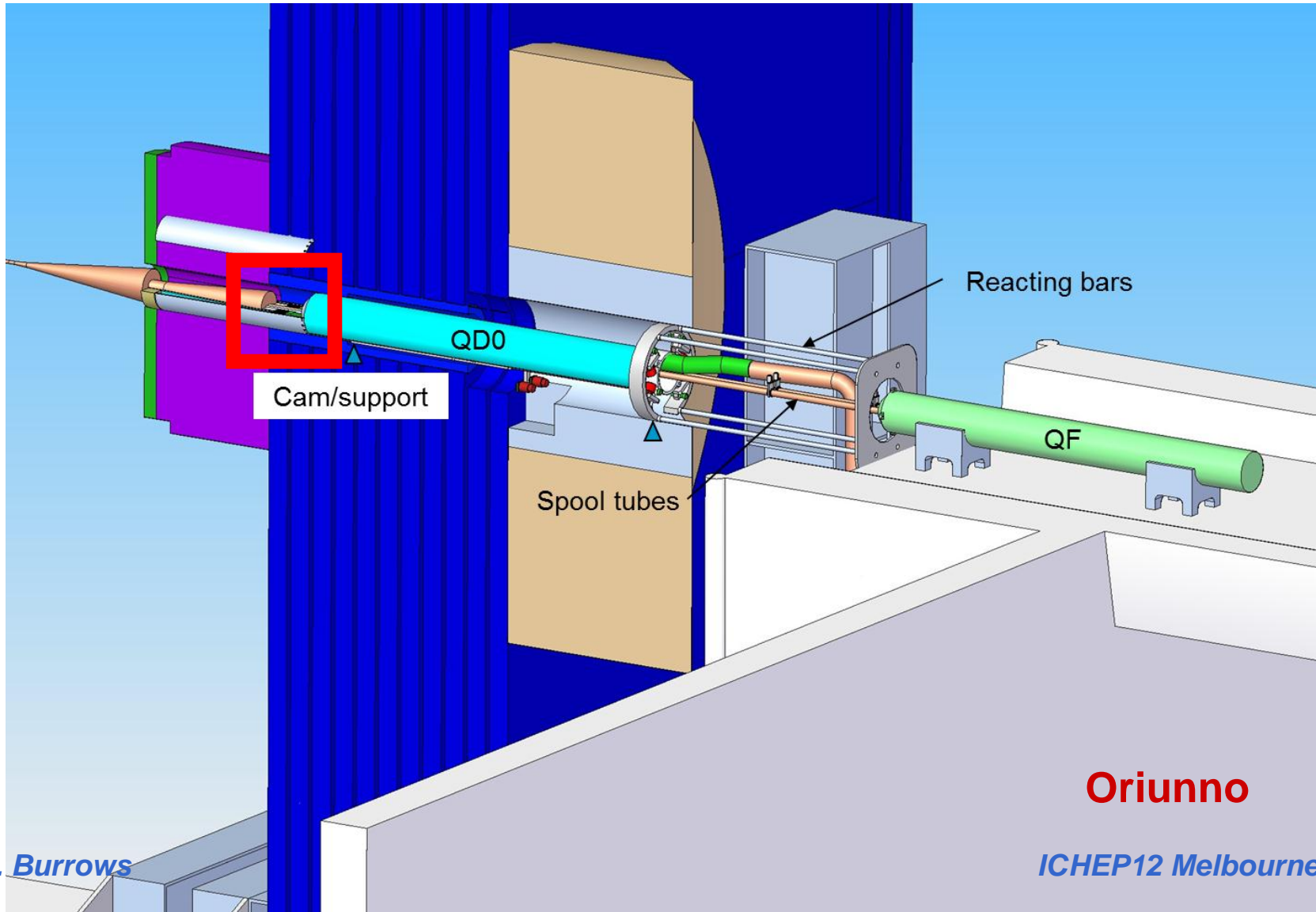


Oriunno

Final Doublet Region (SiD)

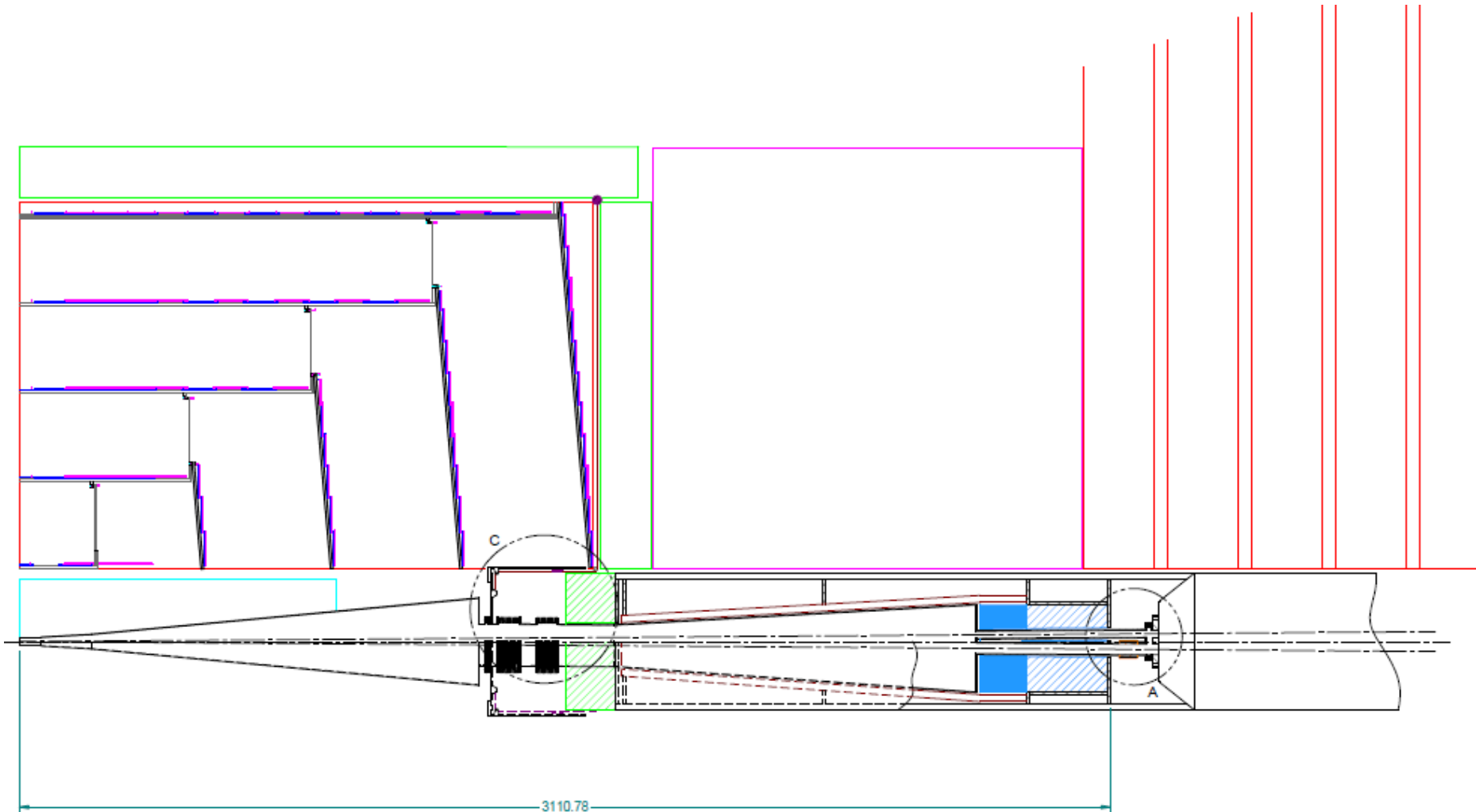


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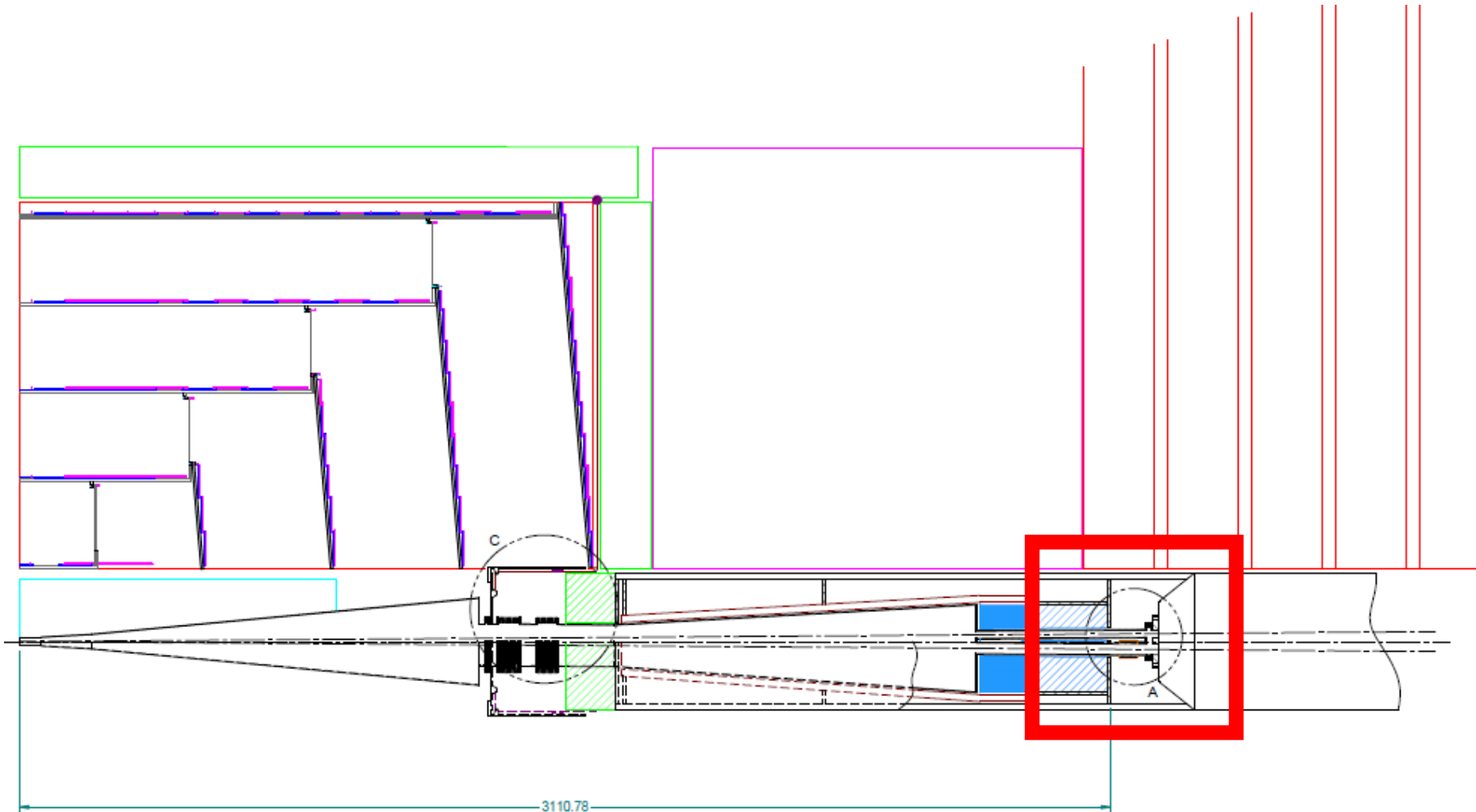


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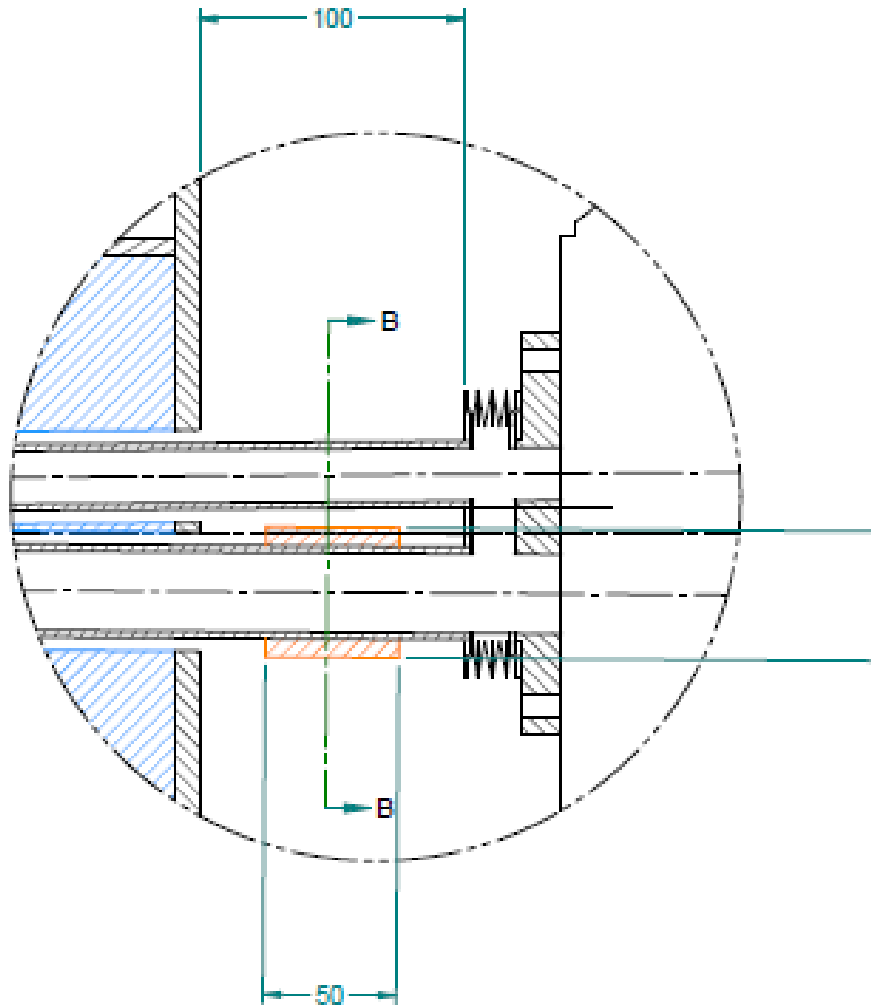
IP Region (SiD)



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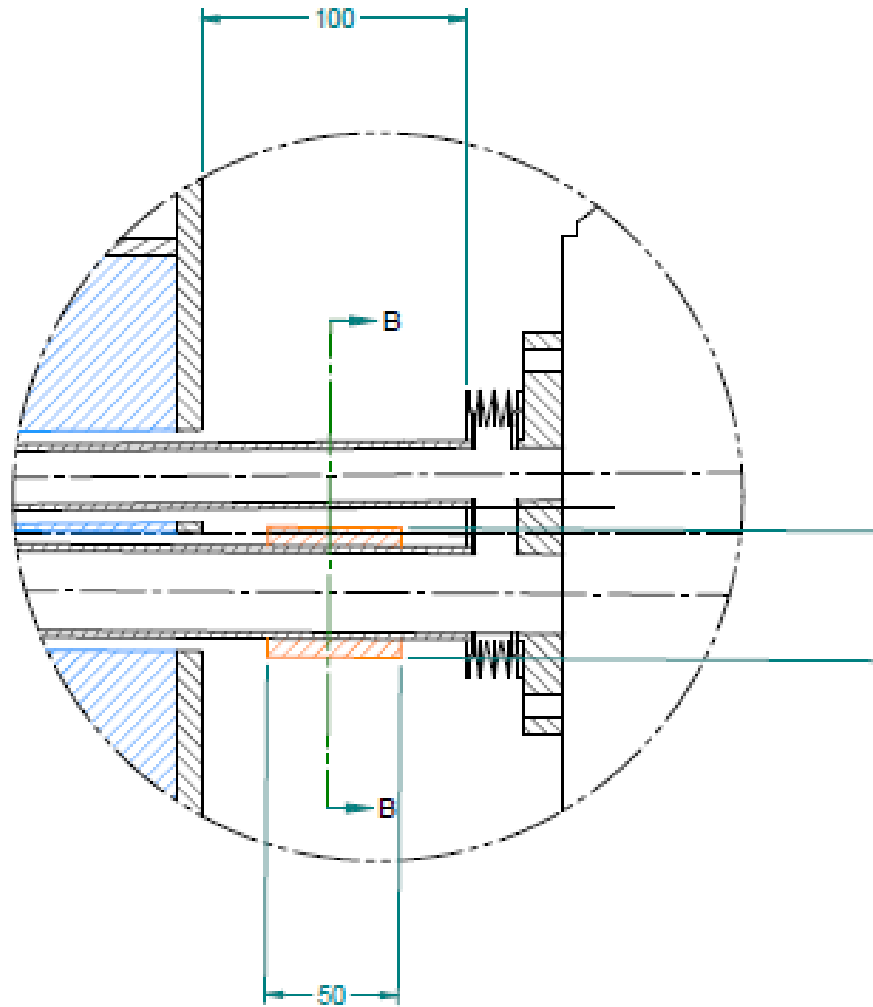


Beamcal – QD0 Region (SiD)

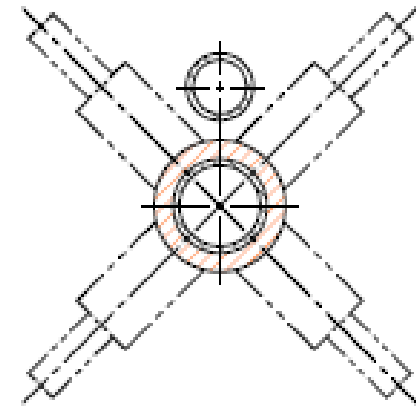


DETAIL A
SCALE 4:1

IP FB BPM Detail (SiD)

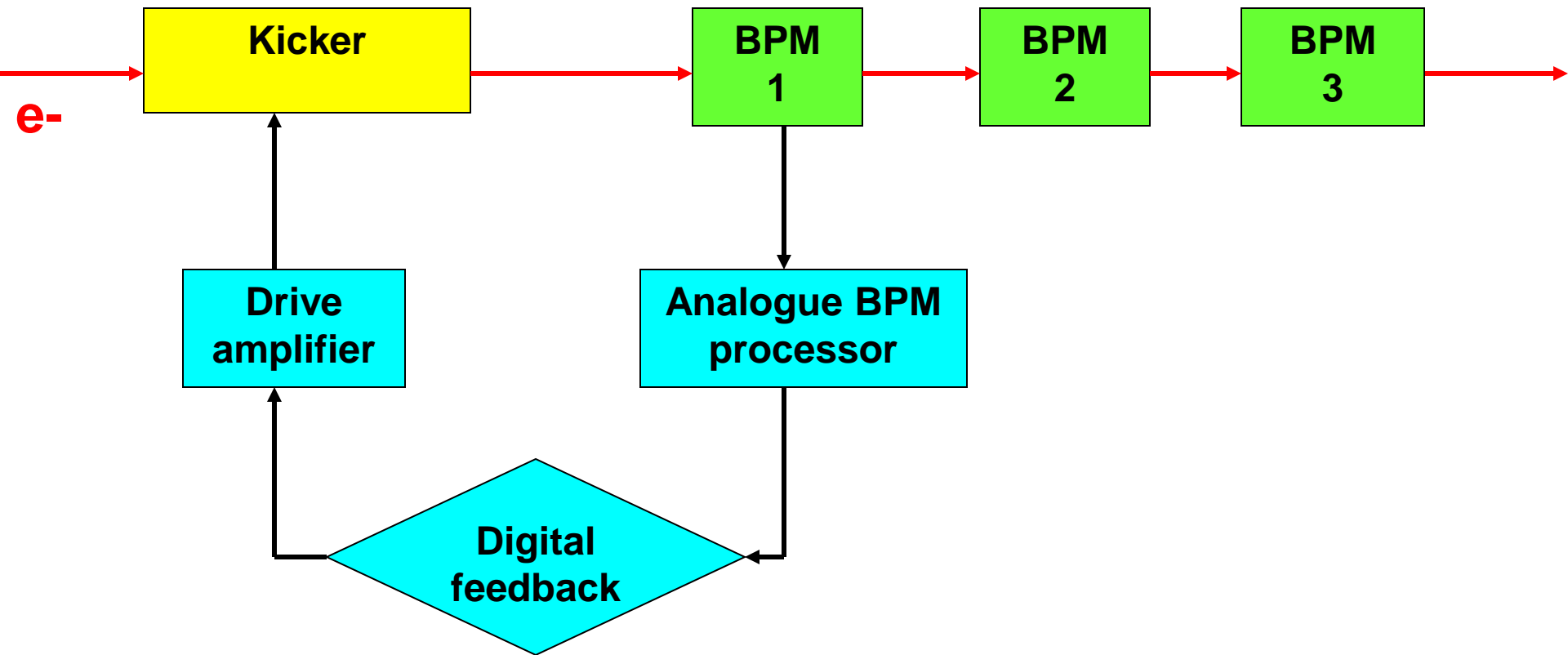


DETAIL A
SCALE 4:1

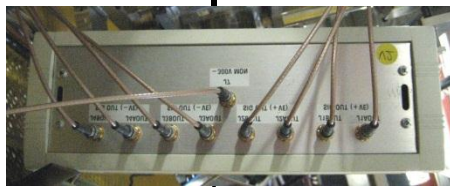


SECTION B-B
SCALE 4:1

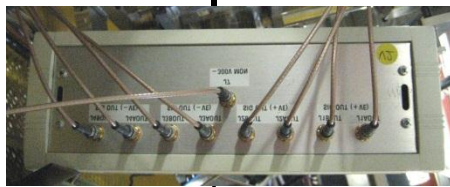
FB prototypes: FONT at KEK/ATF



ILC prototype: FONT4 at KEK/ATF



ILC prototype: FONT4 at KEK/ATF



BPM resolution < 1 μ m
Latency ~ 130ns
Drive power > 300nm
@ ILC

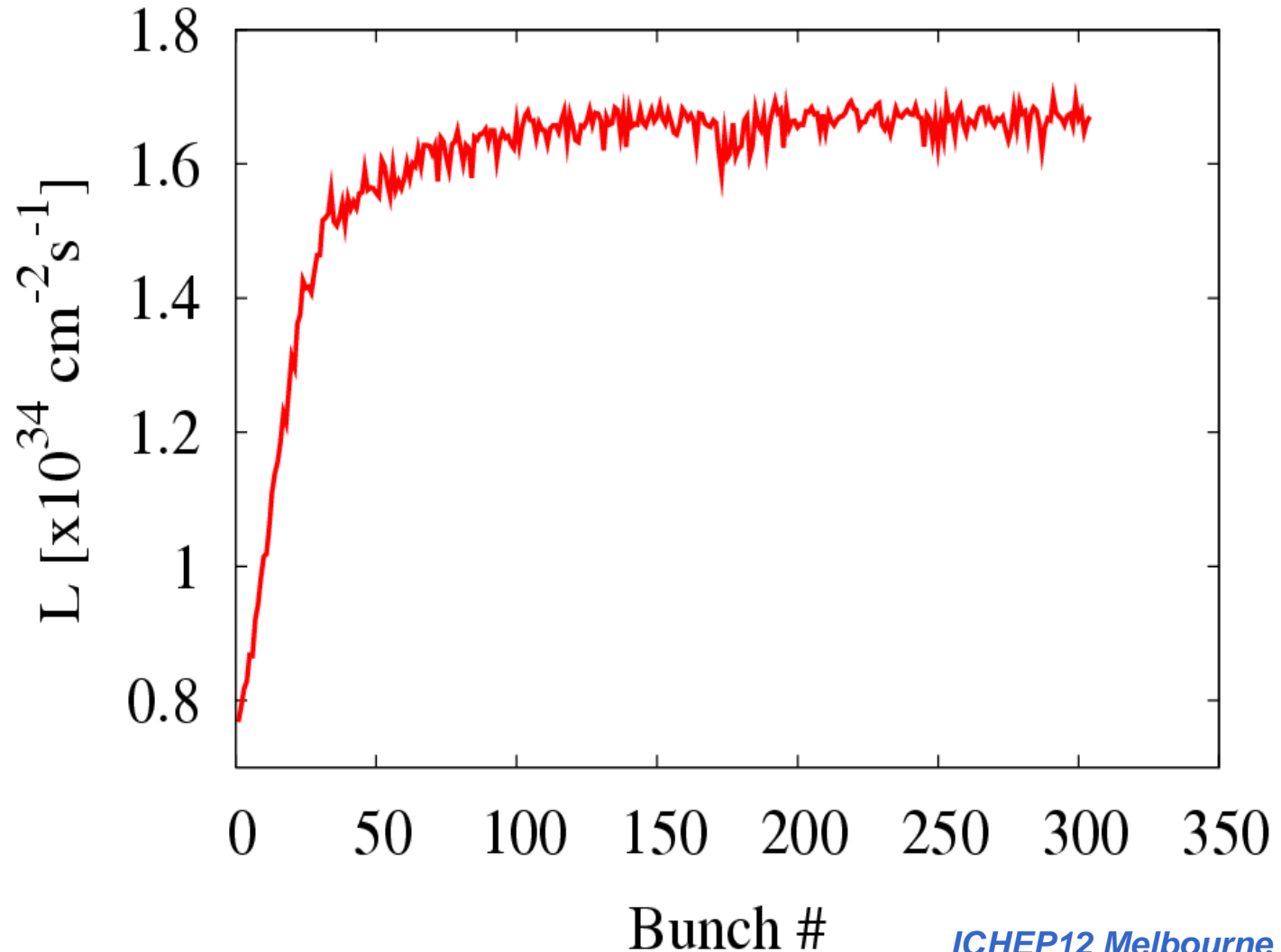
Latency

- Time of flight kicker – BPM: 12ns
- Signal return time BPM – kicker: 32ns
- **Irreducible latency: 44ns**

- BPM processor: 10ns
- **ADC/DAC (4.5 357 MHz cycles) 14ns**
- **Signal processing (8 357 MHz cycles) 22ns**
- **FPGA i/o 3ns**
- Amplifier 35ns
- Kicker fill time 3ns
- **Electronics latency: 87ns**

- **Total latency budget: 131ns**

ILC IP FB performance



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ICHEP12 Melbourne 7/7/12

IP FB Design Status: CLIC

Conceptual design developed and documented in CLIC CDR (2011)

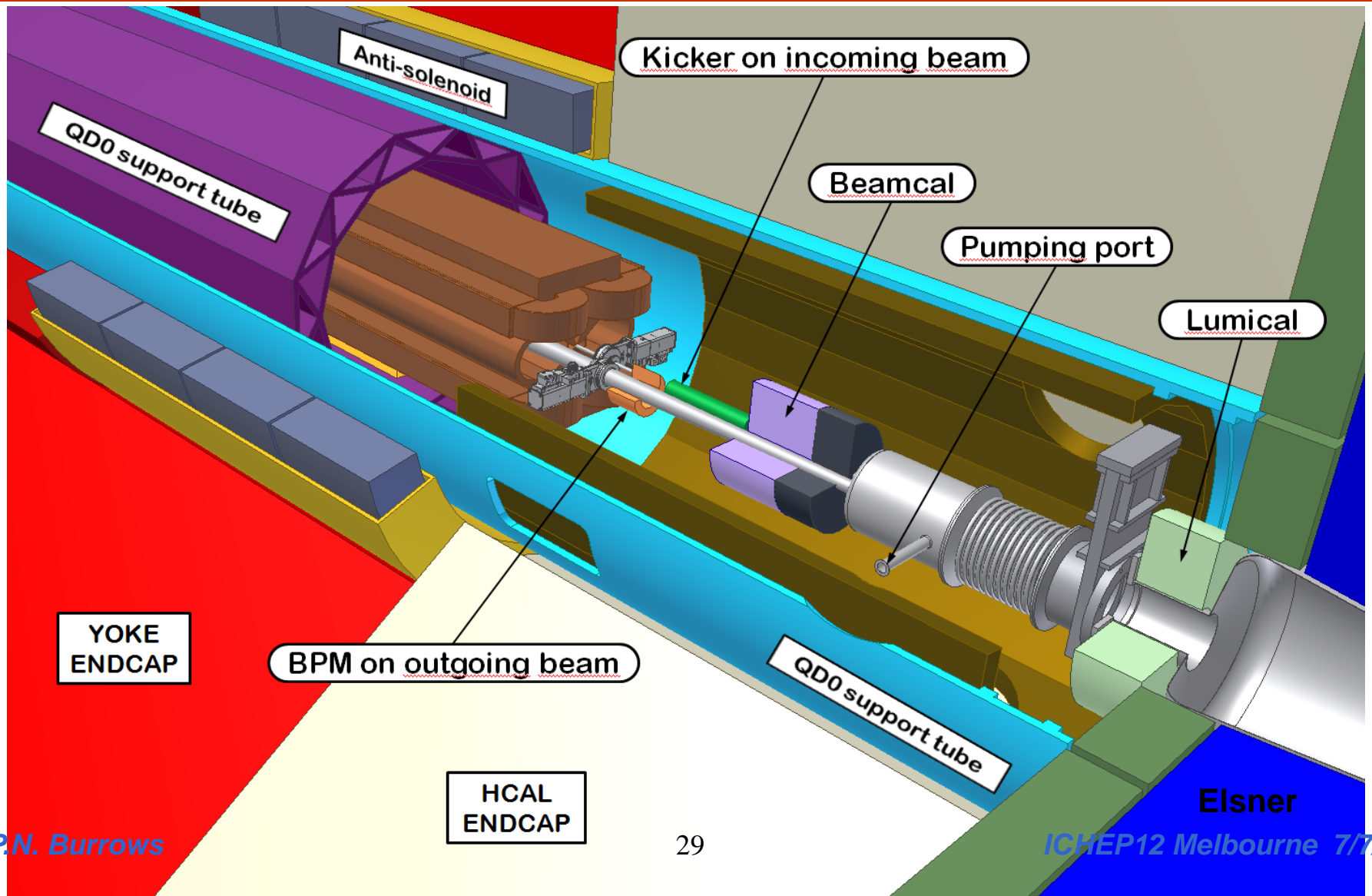
NB primary method for control of beam collision overlap is via vibration isolation of the FF magnets, and dynamic correction of residual component motions

IP position feedback:

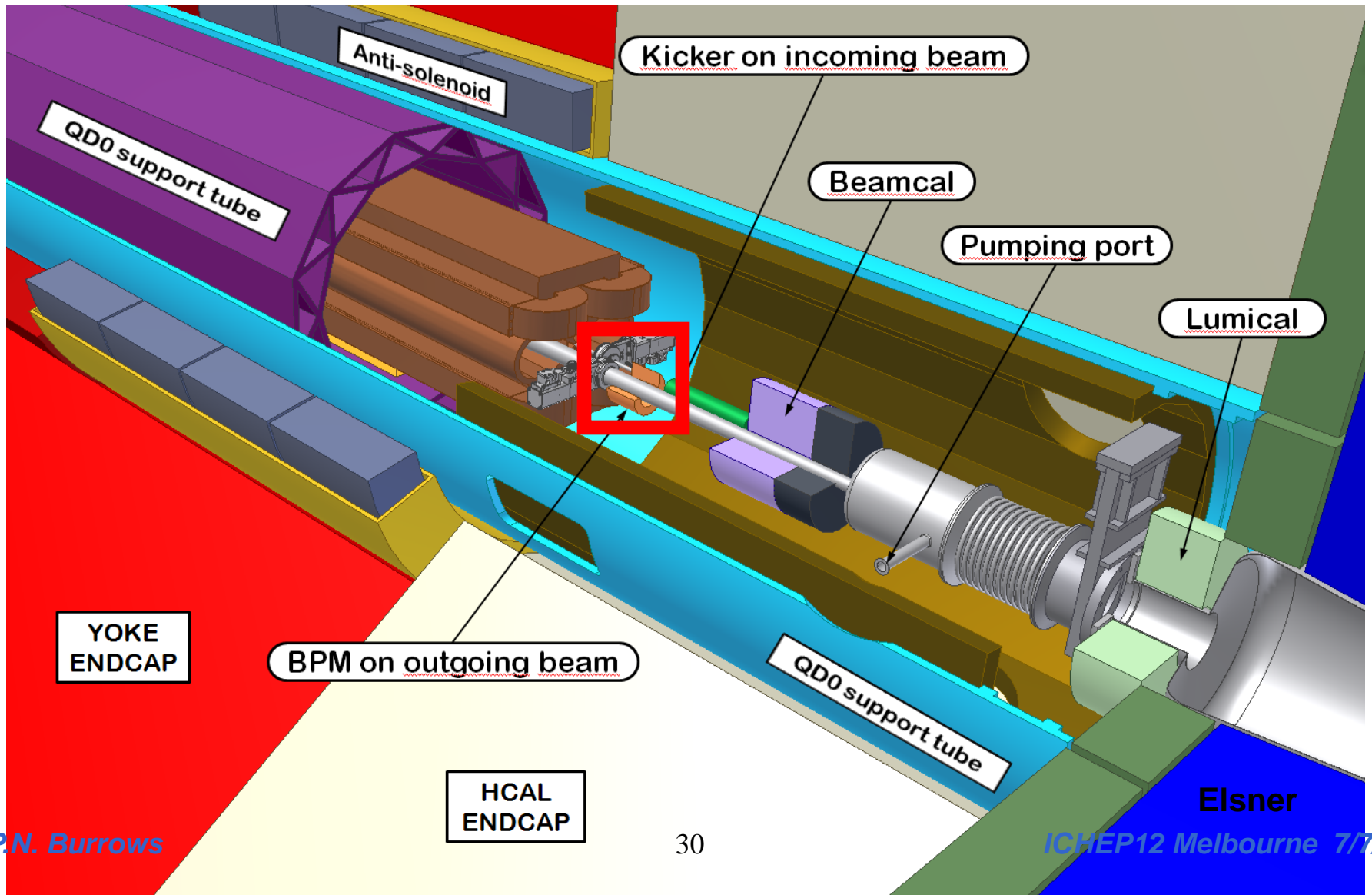
beam position correction up to ± 50 nm vertical at IP

More realistic engineering design can be developed in next project phase

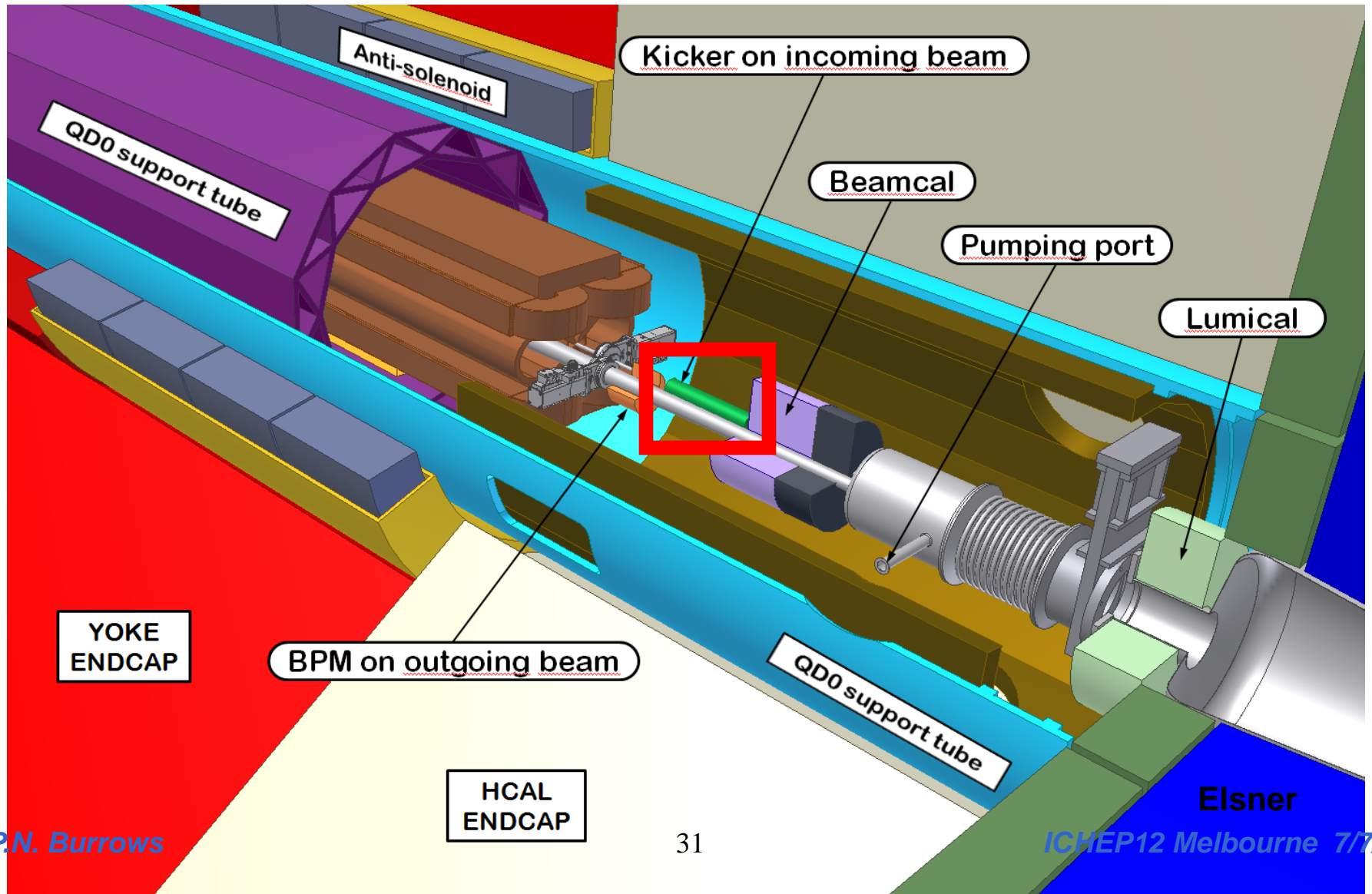
CLIC Final Doublet Region



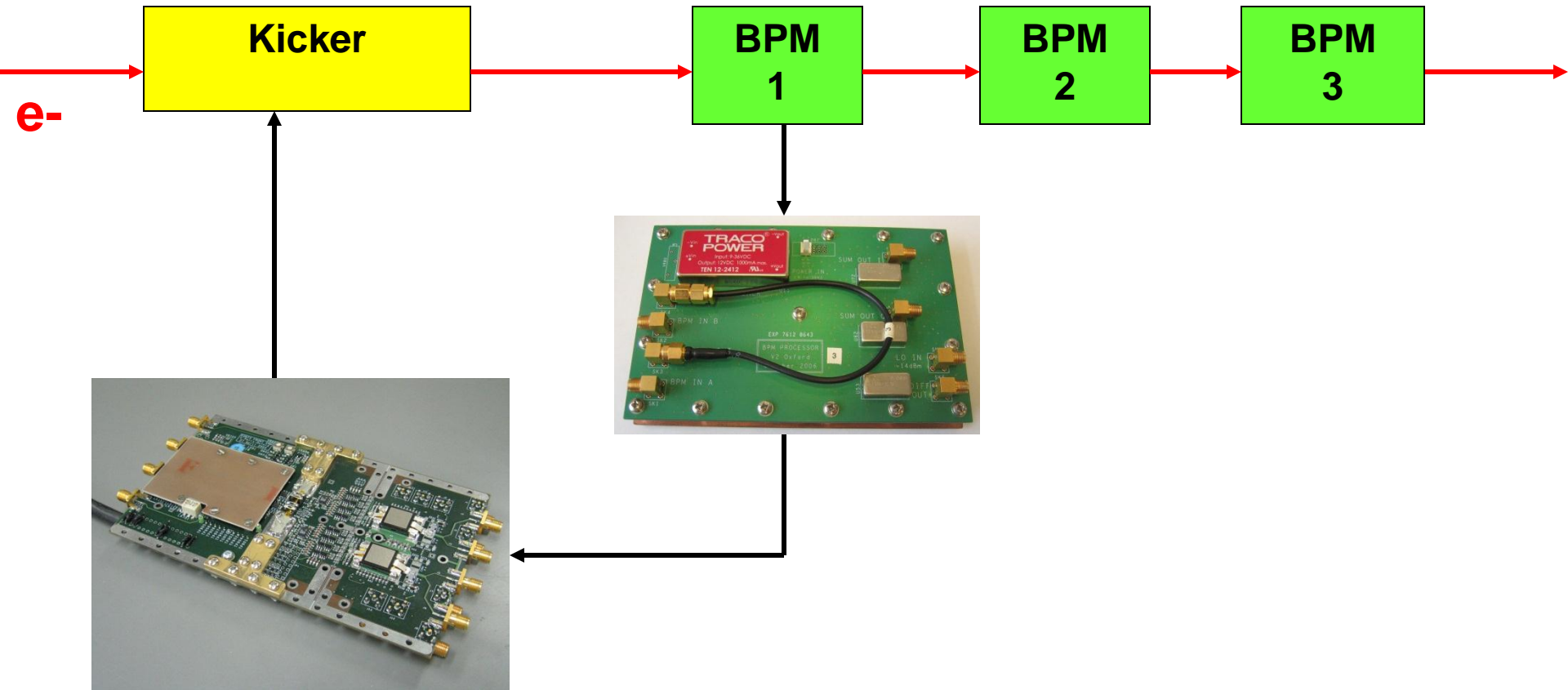
CLIC Final Doublet Region



CLIC Final Doublet Region



CLIC prototype: FONT3 at KEK/ATF



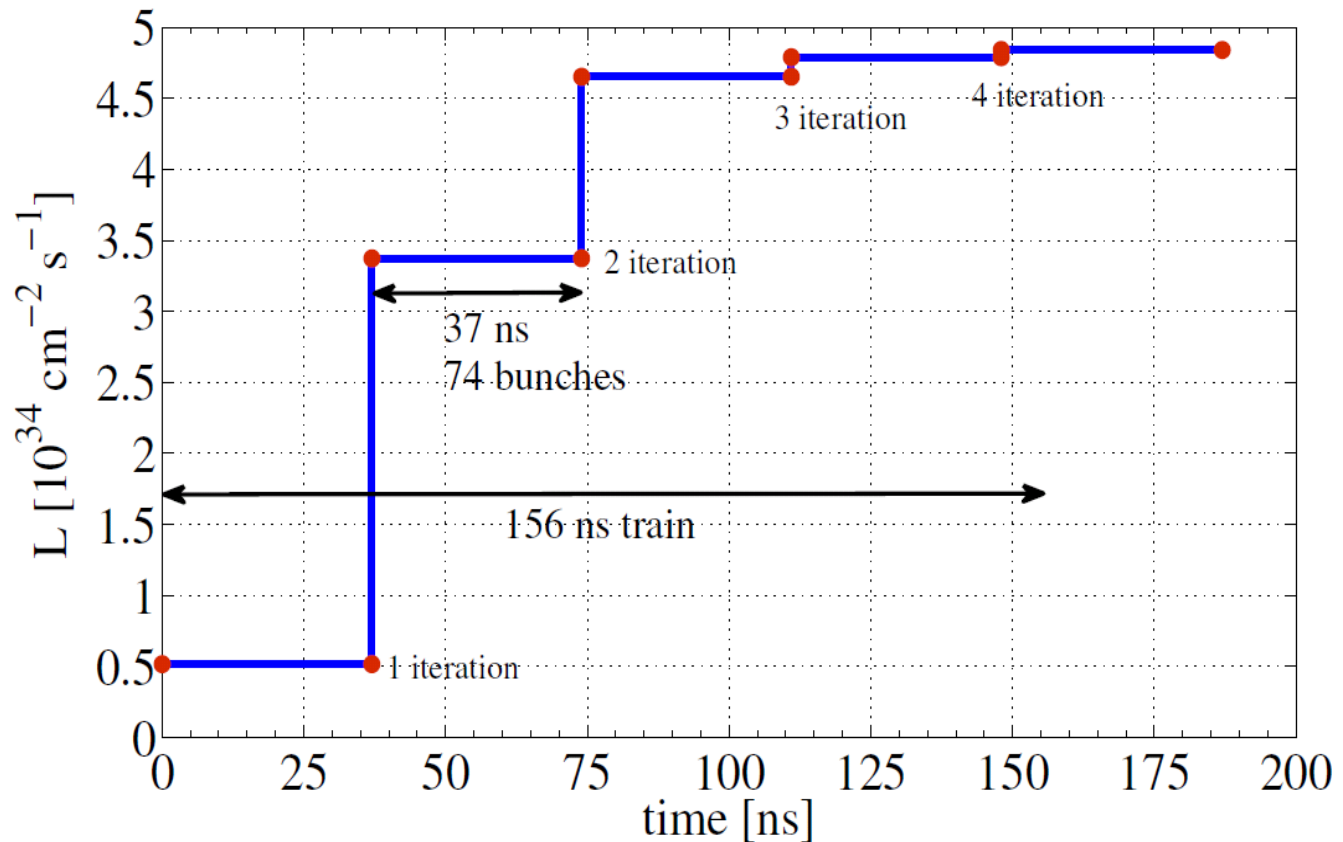
CLIC prototype: FONT3 at KEK/ATF



Electronics latency ~ 13ns
Drive power > 50nm
@ CLIC

CLIC IP FB performance

Single random seed of GM C

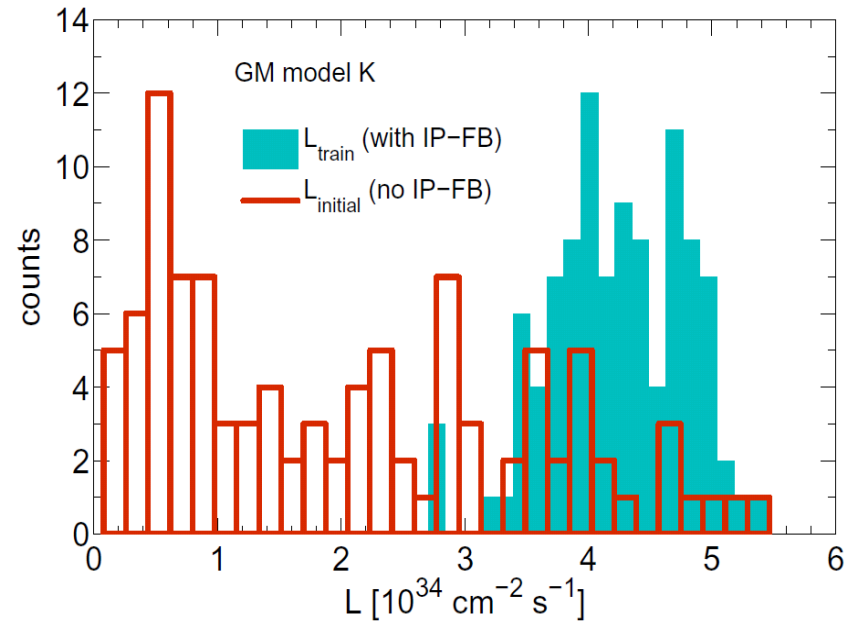
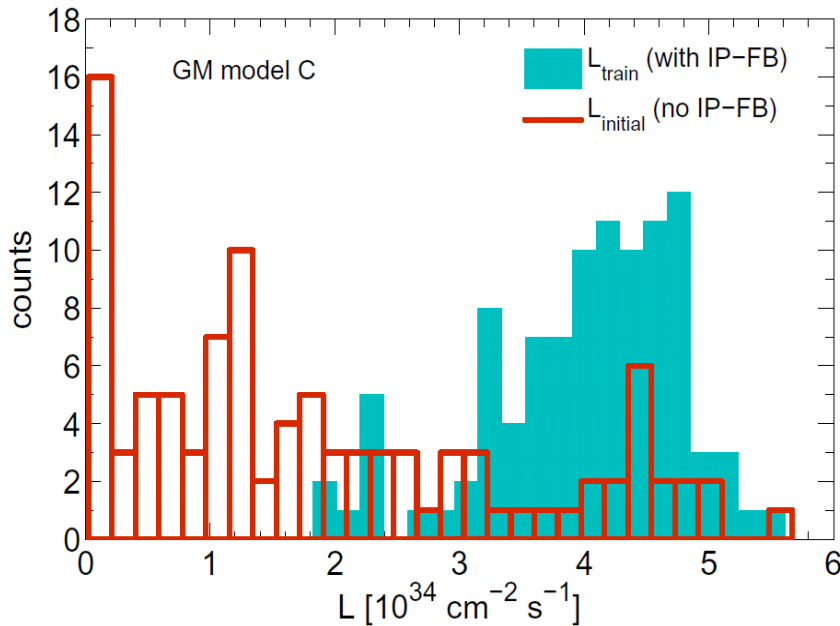


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CLIC IP FB performance

For noisy sites:



→ factor 2 - 3 improvement

Outstanding Technical Issues

- **Component designs optimised for tight spatial environment**
- **Routing of cables**
- **Operation of (ferrite) devices in large, spatially-varying B-field**
- **Further studies of radiation environment**
- **Electronics location, rad hardness, shielding**
- **RF interference: beam \leftrightarrow FB electronics**
kicker \leftrightarrow detector

Summary

- **Well developed IP collision FB system designs for both ILC and CLIC**
- **Simulations demonstrate luminosity recovery capability**
- **Demonstrated prototypes with required performance parameters**
- **Progress on designing customised beamline components (ILC)**