The DEPFET pixel vertex detector for the Belle II experiment at SuperKEKB

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on behalf of the DEPFET Collaboration

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- University of Bonn
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- University of Göttingen
- University of Karlsruhe

www.depfet.org
• The SuperKEKB project

• The DEPFET concept

• The DEPFET-PXD
  • Mechanical engineering
  • Cooling
  • Module concept
  • Data acquisition

• Outlook
SuperKEKB is the successor of the KEKB accelerator currently holding the world record of integrated luminosity of 1024fb$^{-1}$

- Asymmetric e+/e- collider 10.4GeV @ Y(4S) resonance
- Nano beam option + increased current

Target: $8 \times 10^{35}$ 1/cm$^2$s, aiming for 50ab$^{-1}$
- Upgrade of data acquisition, trigger and sub detectors
- Inner detector:
  - Silicon strip detector suffers from high occupancy
  - Two layers of pixel detector (PXD)
- Requirements for the PXD:
  - High hit density ~8MHz/cm$^2$
  - Radiation hardness ~ 2 MRad/y
  - Low momentum tracks (<1GeV)
  - Acceptance 17 -155°

→ Goal: Pixel detector should not only withstand the harsh environment but also improve the performance of the inner detector
**The DEPFET Active Pixel Detector**

**Depleted Field Effect Transistor baseline for the BELLE II PXD**

- In pixel amplification of charge
- Potential minimum under gate
- Electrons modulate current in FET
- Charge is removed via clear

- Low input capacity
- Fully depleted operation - high sensitive volume
- Charge collection always active

→ DEPFET allows to build low mass, high S/N detector
DEPFET matrix operation

- DEPFET pixel cells arranged on grid
- Readout via rolling shutter mode
  - Select row
  - Read current
  - Reset row

→ Column parallel readout – fast readout
→ Low power dissipation in active area

- Three different ASICS needed:
  - Switcher
  - DCD (Drain Current Digitizer)
  - DHP (Data Handling Processor)

- PXD: frame time 20μs – 92ns row processing time
DEPFET pixel cell development and characterization

- Belle II pixel cell
  - Pixel size $50\mu m^2$, $50\times75\mu m^2$
  - Optimized for
    - Fast charge collection
    - Fast clear

- Test beam characterization
  - Belle pixel cell
  - $50\mu m$ thin DEPFETS
  - 100ns row processing time

→ SNR for MIPs of 20-40
→ Resolution: 12.4µm
DEPFET is developed and produced at MPI - Semiconductor lab (HLL) in Munich:

- Double sided process on high resistivity silicon
- Detectors on wafer scale
- Compatible thinning technology
  - Low multiple scattering
  - Flexible device size

→ PXD baseline: 75 µm – 0.2%X₀
The first DEPFETs on thin substrate
DEPFET module

- All silicon, mechanically self sustained module
- Incorporating all necessary electronics
  - Switcher for control
  - DCDB for digitization and DHP for data processing and transmission
• Tight mechanical constraints:
  • Beampipe @ 12mm radius
  • PXD @ 14/22mm
  • SVD @ 38mm radius

• Design of PXD incorporates:
  • Stable mounting allowing thermal expansion
  • Thermal management
  • Services for power and data transmission and cooling

• Detailed 3d design of the PXD ready
...with real thinned Si ladders

beam pipe support and cable stress relief

mechanical support and CO2 evaporator
Cooling

- 360W power dissipation while operation
  - Dominated by readout ASICs outside of the acceptance
  - Power consumption in active area \( \sim 0.4\text{W/cm}^2 \)

- Active area cooled by cold air

- Modules mounted directly on cooled mounting block
  \( \rightarrow \) Direct thermal contact

- Cooling of PXD demonstrated
On module digitization and zero suppression

- Rate ~4.6Gbit/s (550MB/s) per module @ 3% occupancy
- Would dominate complete BELLE II data

- Online Pattern recognition with the strip detector to identify physics hits
- Further data reduction to 1/30
Performance of the Belle II PXD

- Expected performance including the 4 layer strip detector:

  • PXD in a nutshell:
    - Two layers: at 14,22mm radius
    - Pixel size: 50x50µm², 50x75µm²
    - Thickness: 75µm
    - Material budget: 0.2% X₀
    - Pixel: 8M
    - Radiation hardness: 10MRad
    - Frame time: 20µs

  ➔ DEPFET PXD will significantly improve z-vertex resolution of the inner detector
The SuperKEKB upgrade aims for a peak luminosity of $8 \times 10^{35}$/cm$^2$s

A 2 layer pixel detector based on DEPFET will be installed

The PXD will improve the IP resolution even in an environment with significantly increased background

Design of PXD is well advanced

- Pixel cell
- Mechanical design and cooling
- Readout electronics and data acquisition
- Module design

PXD ready by mid 2015
Backup
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<th>2016</th>
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<td>Summer Shutdown</td>
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<td>July 2014</td>
<td>machine ready with QCS</td>
<td>Roll-in GCR Contrac COMP ready by Oct. 1</td>
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<td>Belle roll-in (no TOP/A-RICH/PXD/SVD/CDC)</td>
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From half-ladder to module

- Half modules must be mechanically connected to form a complete PXD module
- Face to face gluing
- Reinforcement with 3 ceramic inserts
- Resilient to bow up to 1mm and a tension of ~40N
Material budget within acceptance

→ 0.19 %$X_0$ in total

Silicon contribution (0.15%)
Backgrounds:

- Touschek scattering (intra-bunch scattering)
- Synchrotron radiation
- Beam-gas scattering

- Radiative Bhabha
- 2-photon process generated electrons

- Latest estimate L1/L2: 1.9Mrad/y / 0.6Mrad/y
- Expected PXD occupancy ~0.9%/0.4% inner/outer layer
- Zero suppression on module level
- Online pattern recognition to reject background
- Online silicon only tracking

80Gbit/s
Θ 4Gbit/s
~40cm

4 links @ 1.25Gbit/s