LUDWIG-MAXIMILIANS-UNIVERSITÄT MÜNCHEN

LMU München - Excellence Cluster Universe

The DEPFET pixel vertex detector for the Belle II experiment at SuperKEKB

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DEPFET Collaboration

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- Charles University, Prague
- DESY Hamburg
- IFCA Santander
- IFIC Valencia
- IFJ PAN, Krakow
- IHEP, Beijing
- KEK-PF, Tsukuba
- LMU Munich
- TU Munich
- MPI Munich / HLL
- University of Barcelona
- University of Bonn
- University of Heidelberg
- University of Giessen
- University of Göttingen
- University of Karlsruhe

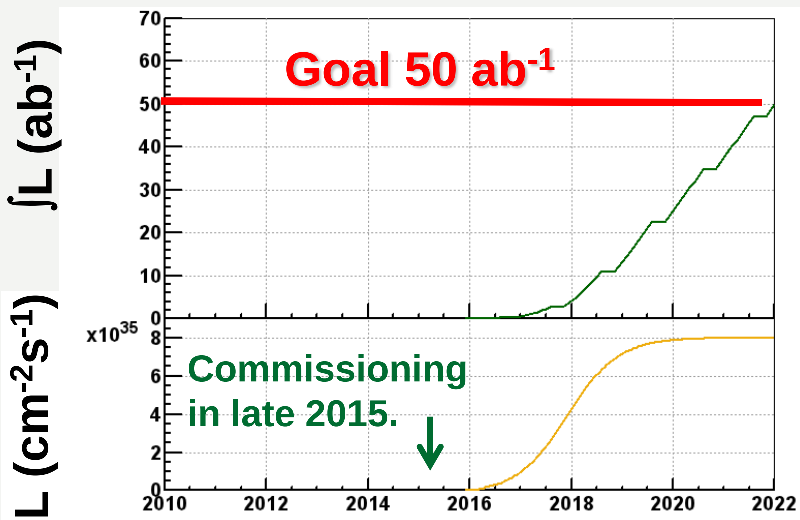
www.depfet.org

Overview

- The SuperKEKB project
- The DEPFET concept
- The DEPFET-PXD
    - Mechanical engineering
    - Cooling
    - Module concept
    - Data acquisition
- Outlook

SuperKEKB accelerator upgrade

- SuperKEKB is the successor of the KEKB accelerator currently holding the world record of integrated luminosity of 1024fb^{-1}
- Asymmetric e+/e- collider 10.4GeV @ Y(4S) resonance
- Nano beam option + increased current



KEKB

	KEKB:	SuperKEKB
Current	1.6/1.2A	2.1/3.7A
Beamsize (V/H)	1/150µm	0.05/10µm
Luminosity	$2x10^{34}$ 1/cm²/s	$8x10^{35}$ 1/cm²/s

→ Target: $8x10^{35}$ $1/cm^2s$, aiming for $50ab^{-1}$

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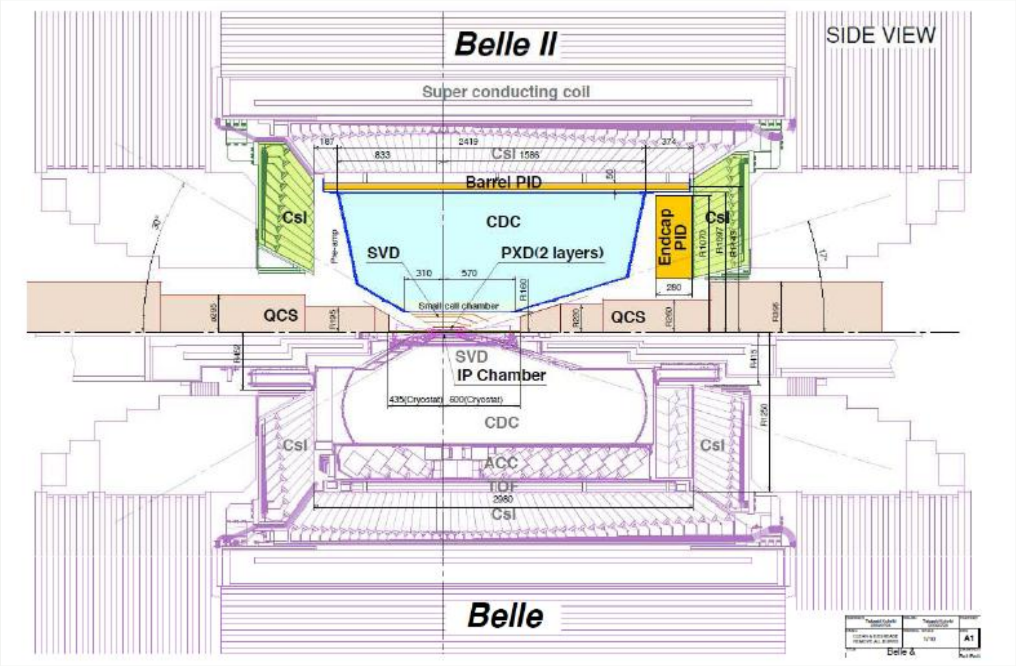
BELLE II upgrade – PXD requirements

- Upgrade of data acquisition, trigger and sub detectors
- Inner detector:
  - Silicon strip detector suffers from high occupancy
  - Two layers of pixel detector (PXD)

- Requirements for the PXD:
  - High hit density ~8MHz/cm^2
  - Radiation hardness ~ 2 MRad/y
  - Low momentum tracks (<1GeV)
  - Acceptance 17 -155°

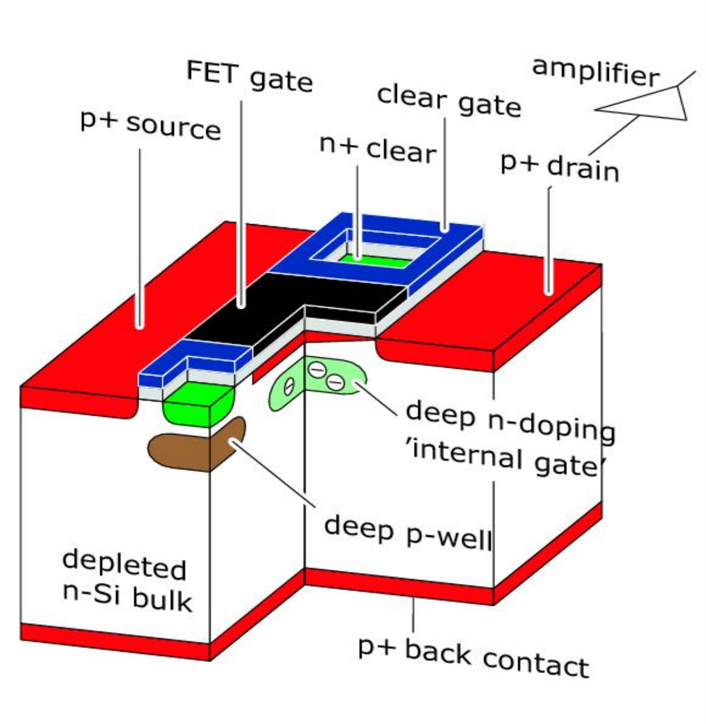


→ Goal: Pixel detector should not only withstand the harsh environment but also <u>improve the performance of the inner detector</u>

The DEPFET Active Pixel Detector

Depleted **F**ield **E**ffect **T**ransistor baseline for the BELLE II PXD

- In pixel amplification of charge
- Potential minimum under gate
- Electrons modulate current in FET
- Charge is removed via clear



- ➢ Low input capacity
- ➢ Fully depleted operation - high sensitive volume
- ➢ Charge collection always active

→ DEPFET allows to build low mass, high S/N detector

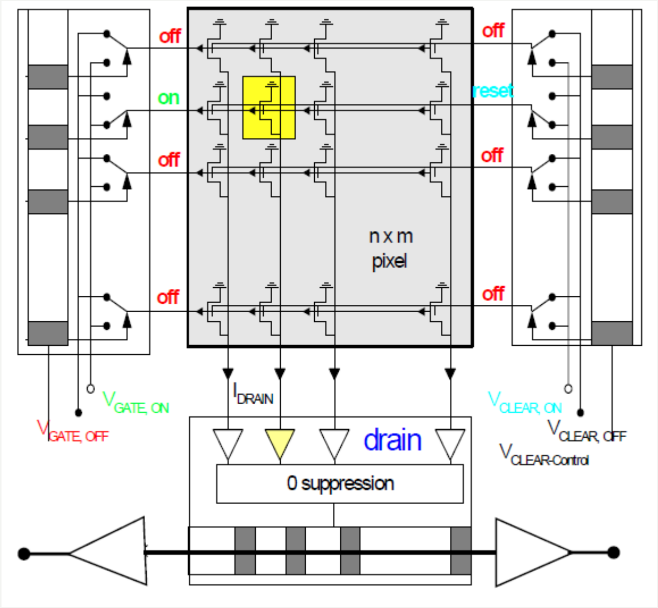
DEPFET matrix operation

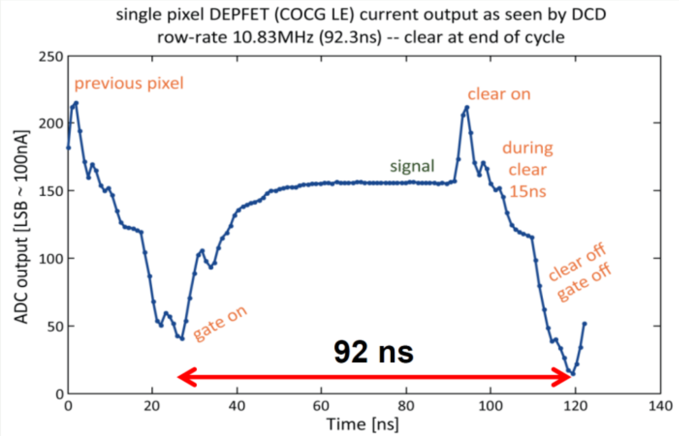
- DEPFET pixel cells arranged on grid
- Readout via rolling shutter mode
  - Select row
  - Read current
  - Reset row

→Column parallel readout – fast readout
→Low power dissipation in active area

- Three different ASICS needed:
  - Switcher
  - DCD (Drain Current Digitizer)
  - DHP (Data Handling Processor)

- PXD: frame time 20µs – 92ns row processing time

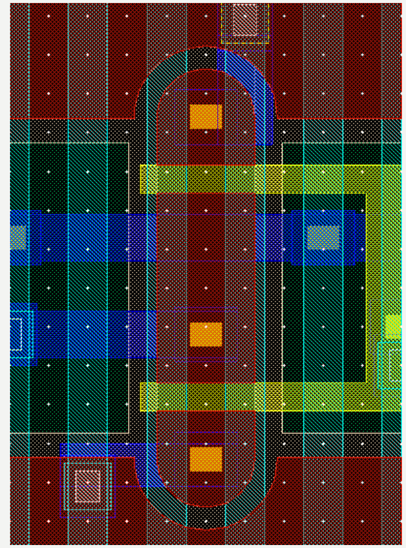


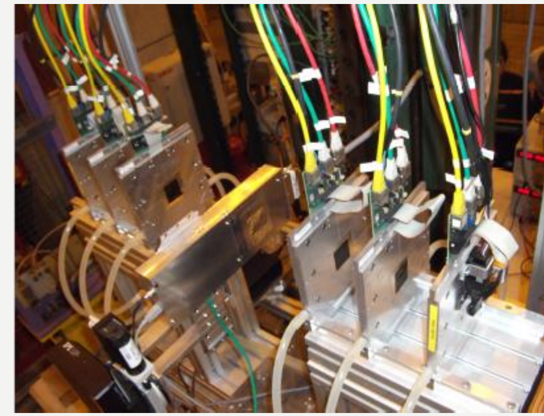


DEPFET pixel cell development and characterization

- Belle II pixel cell
  - Pixel size 50µm^2,50x75µm^2

  Optimized for
  - Fast charge collection
  - Fast clear

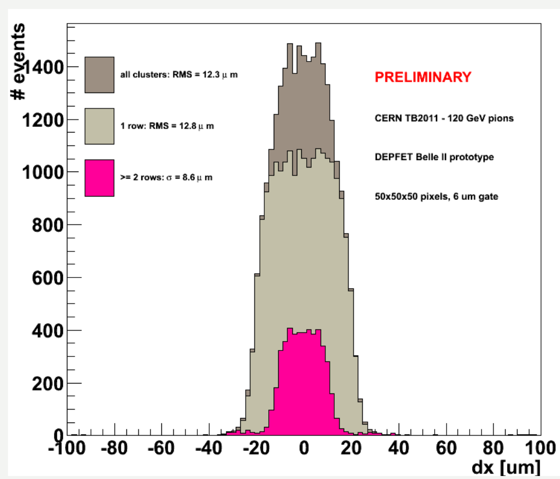


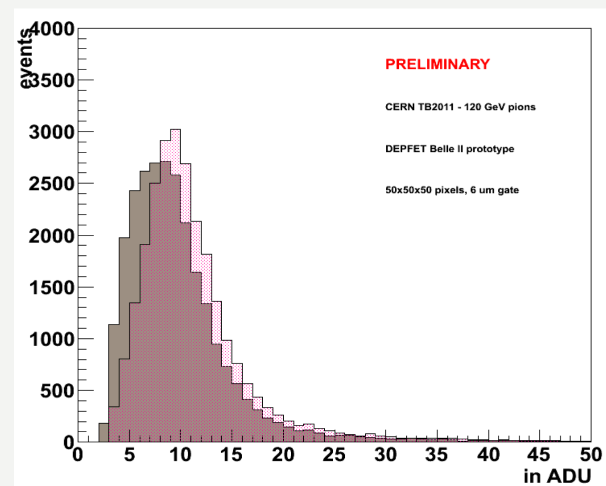


- Test beam characterization
  - Belle pixel cell
  - 50µm thin DEPFETS
  - 100ns row processing time

→ SNR for MIPs of 20-40

→ Resolution: 12.4µm





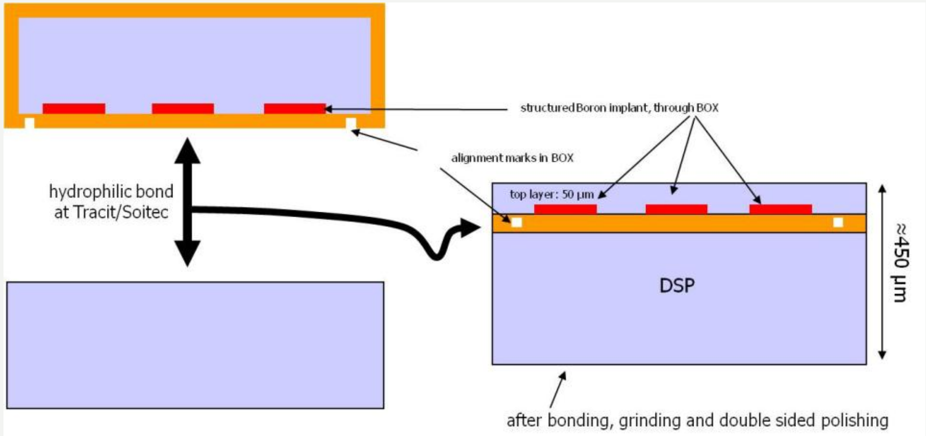
DEPFET Technology

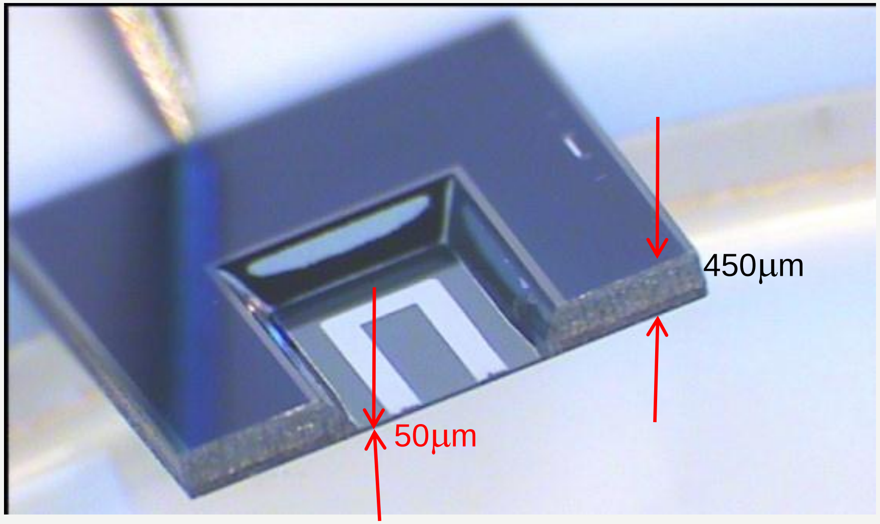
DEPFET is developed and produced at MPI - Semiconductor lab (HLL) in Munich:

- Double sided process on high resistivity silicon
- Detectors on wafer scale
- Compatible thinning technology

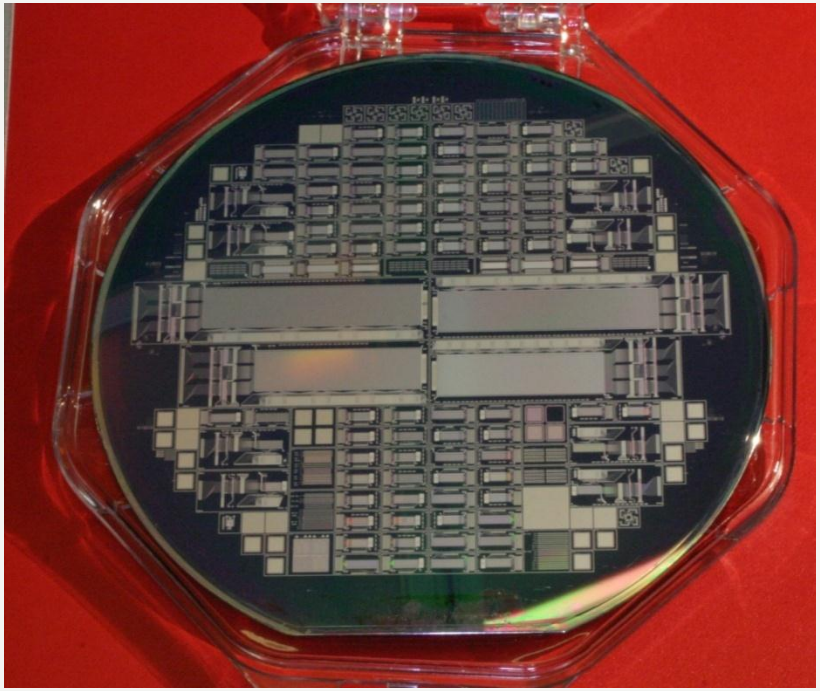
- ➢ Low multiple scattering
- ➢ Flexible device size

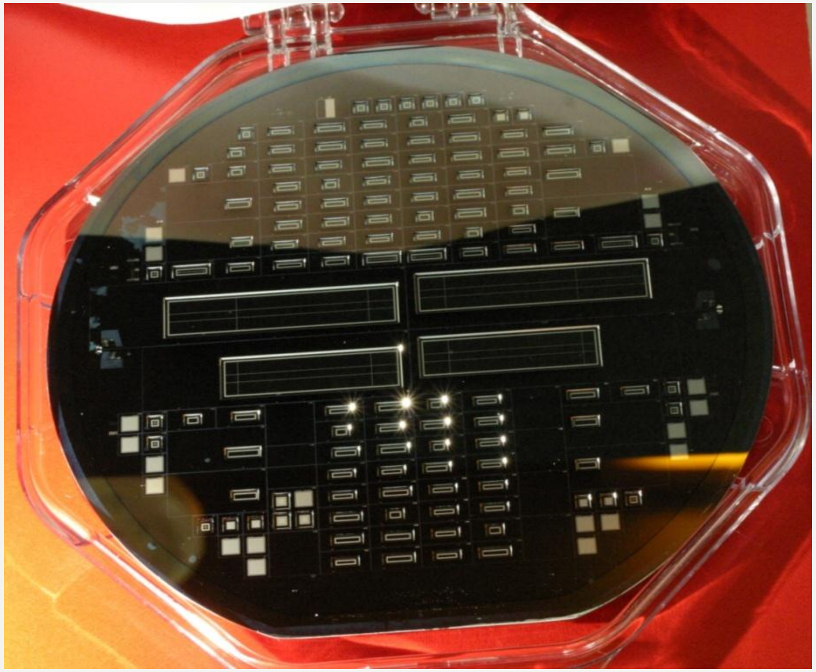
→ PXD baseline: 75 µm – 0.2%X_0





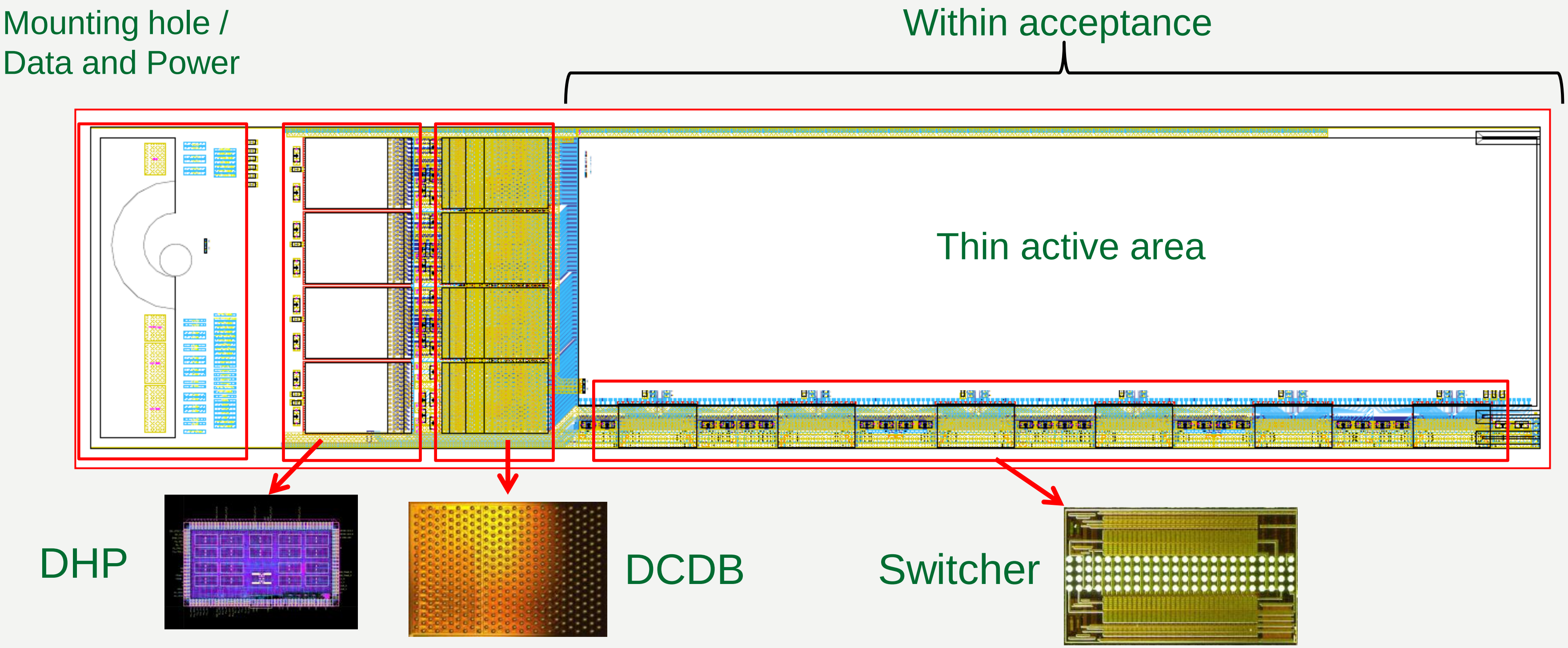
DEPFET Technology





The first DEPFETs on thin substrate

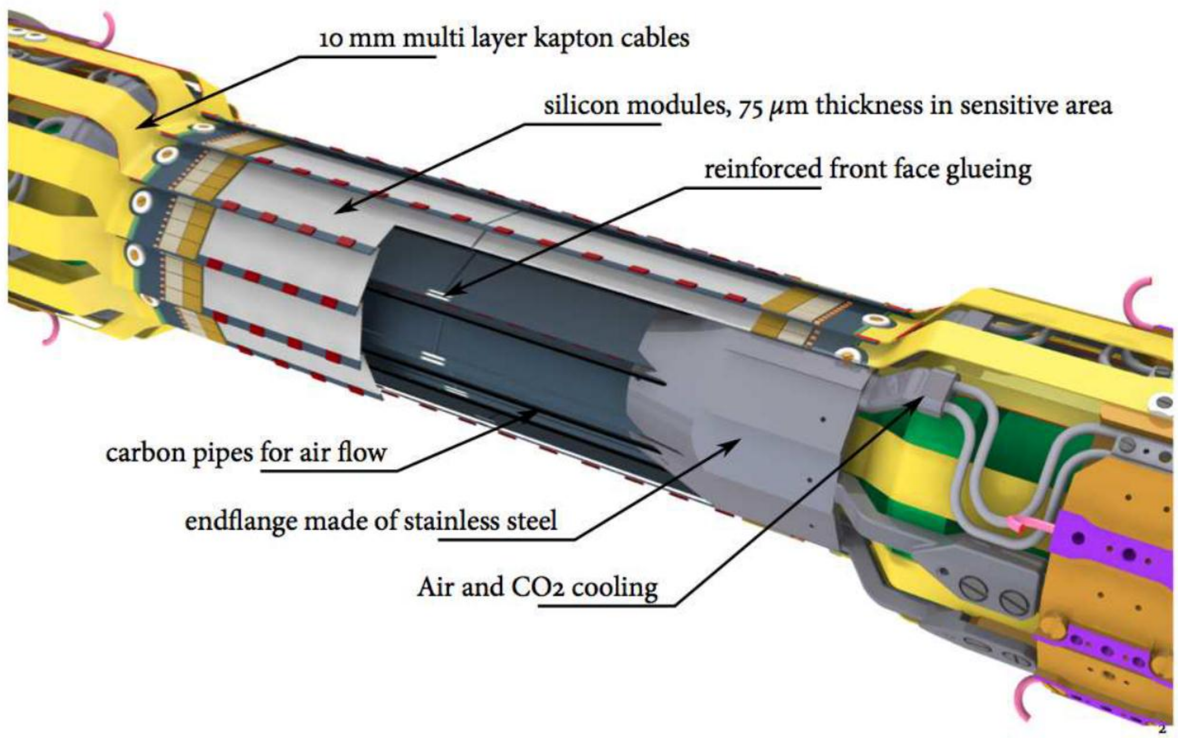
DEPFET module



- All silicon, mechanically self sustained module
- Incorporating all necessary electronics
  - Switcher for control
  - DCDB for digitization and DHP for data processing and transmission

Mechanical Engineering

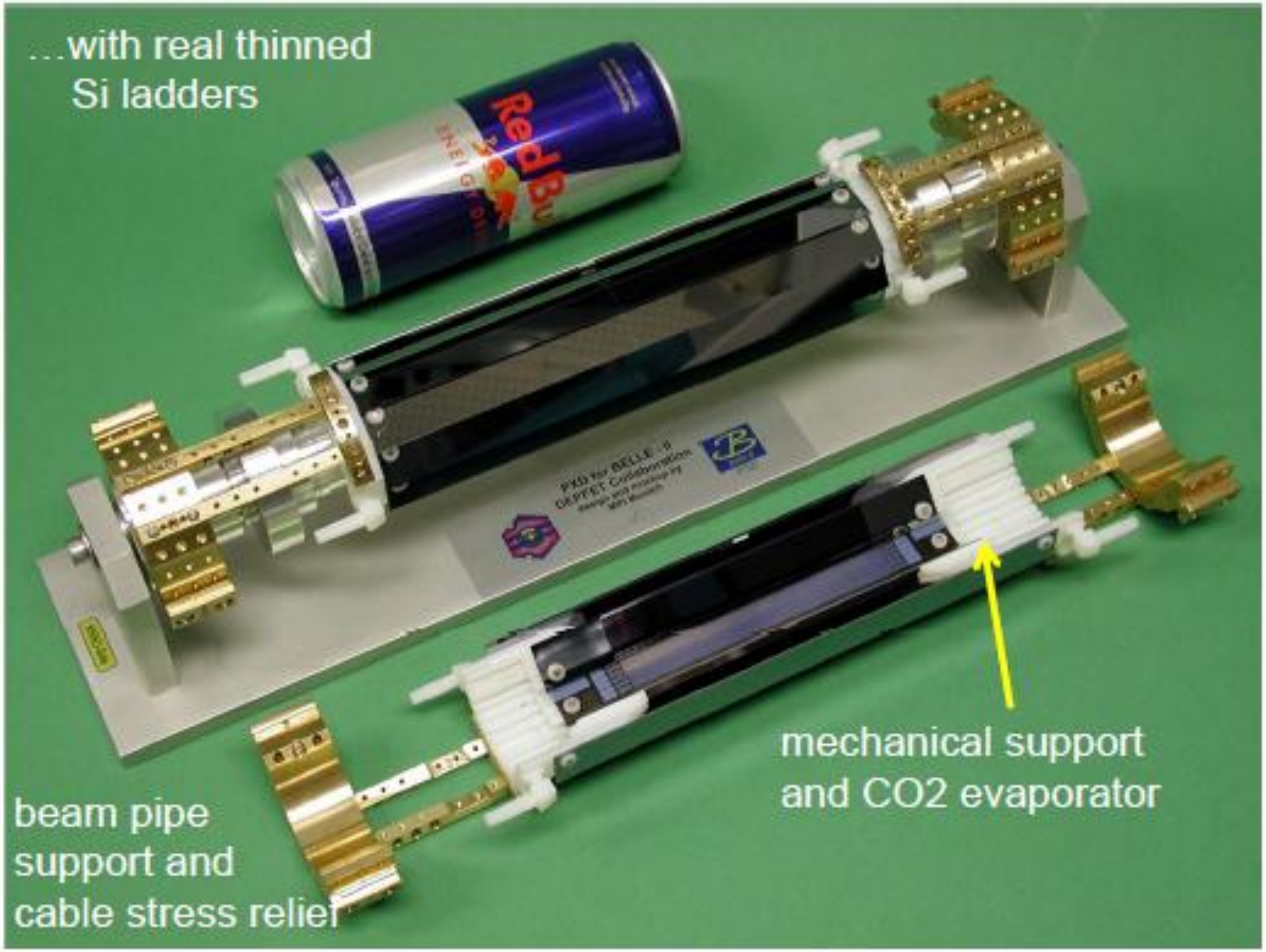
- Tight mechanical constraints:
  - Beampipe @ 12mm radius
  - PXD @ 14/22mm
  - SVD @ 38mm radius



- Design of PXD incorporates:
  - Stable mounting allowing thermal expansion
  - Thermal management
  - Services for power and data transmission and cooling

- Detailed 3d design of the PXD ready

Mechanical Engineering

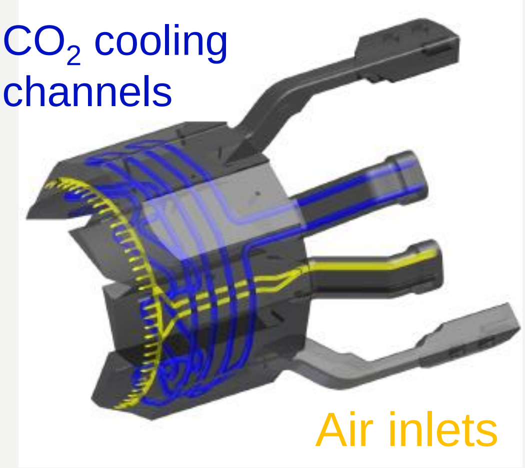


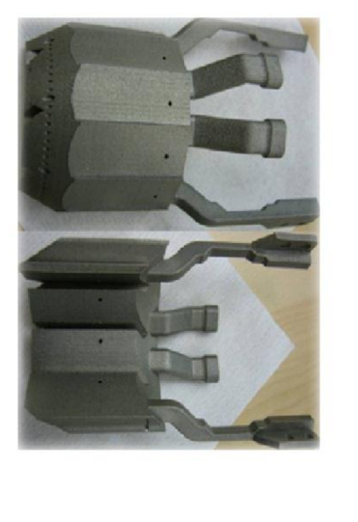
Cooling

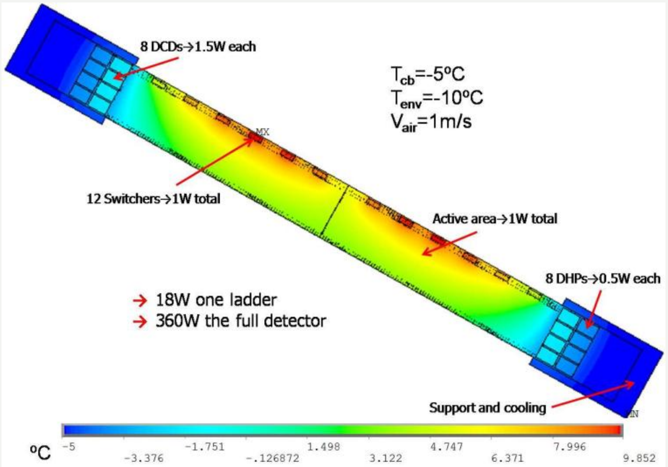
- 360W power dissipation while operation
  - Dominated by readout ASICs outside of the acceptance
  - Power consumption in active area ~.4W/cm^2

- Active area cooled by cold air

- Modules mounted directly on cooled mounting block
  → Direct thermal contact

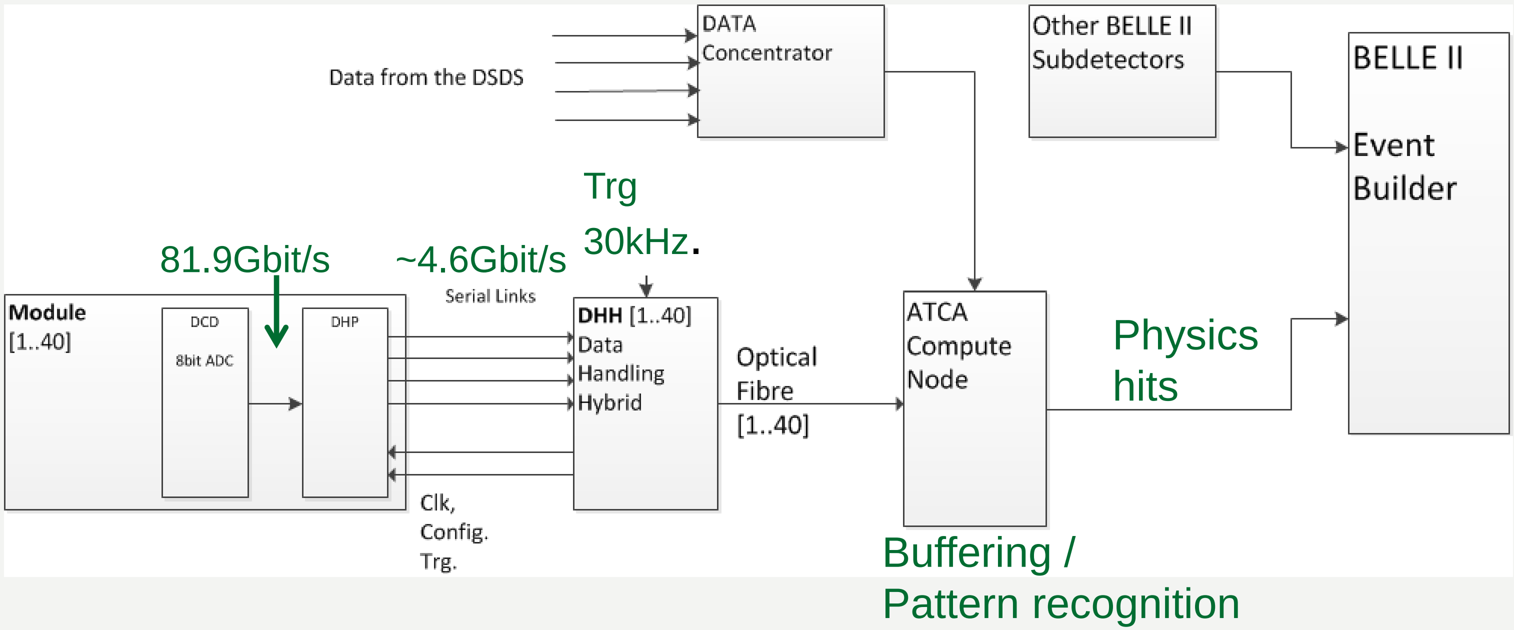






- Cooling of PXD demonstrated

Data Acquisition and processing



- On module digitization and zero suppression

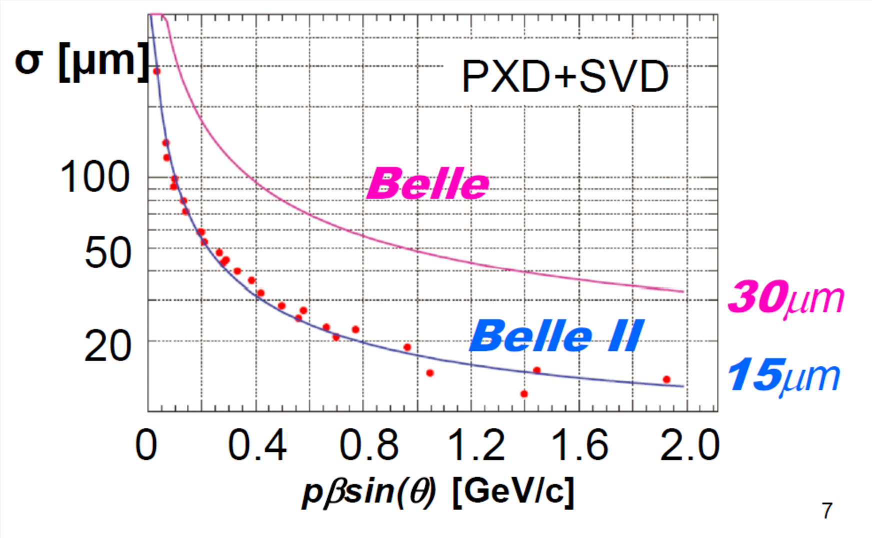
→ Rate ~4.6Gbit/s (550MB/s) per module @ 3% occupancy

→ Would dominate complete BELLE II data

- Online Pattern recognition with the strip detector to identify physics hits
- Further data reduction to 1/30

Performance of the Belle II PXD

- Expected performance including the 4 layer strip detector:



BELLE II Silicon: 2 + 4 Layers, Pixel + Strips

PXD in a nutshell:

- Two layers: at 14,22mm radius
- Pixel size 50x50µm², 50x75µm²
- Thickness: 75µm
- Material budget: 0.2% X_0
- Pixel: 8M
- Radiation hardness: 10MRad
- Frame time: 20µs

→ DEPFET PXD will significantly improve z-vertex resolution of the inner detector

Summary

- The SuperKEKB upgrade aims for a peak luminosity of $8x10^{35}/cm^2s$
- A 2 layer pixel detector based on DEPFET will be installed
- The PXD will improve the IP resolution even in an environment with significantly increased background
- Design of PXD is well advanced
  - Pixel cell
  - Mechanical design and cooling
  - Readout electronics and data acquisition
  - Module design
- PXD ready by mid 2015

Backup

Schedule

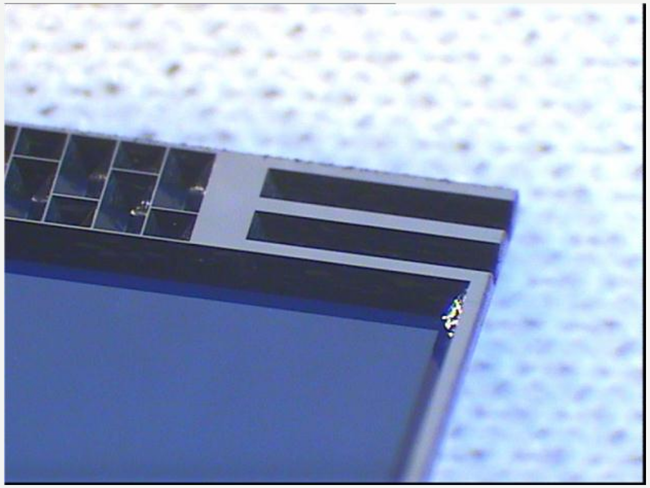
2014			2015								
10	11	12	1	2	3	4	5	6	7	8	9
	BEAST 2							Summer Shutdown			
machine ready **with** QCS					Belle Roll-out					PXD ready	VXD Integration
Belle roll-in (no TOP/A-RICH/PXD/SVD/CDC)									Roll-In	GCR Contract over	COMP ready by Oct. 1
July 2014						install					
						TOP/RICH/CDC					
2015			2016								
10	11	12	1	2	3	4	5	6	7	8	9
VXD Comm.									Summer Shutdown		
	VXD inst.	Physics Run									

From half-ladder to module

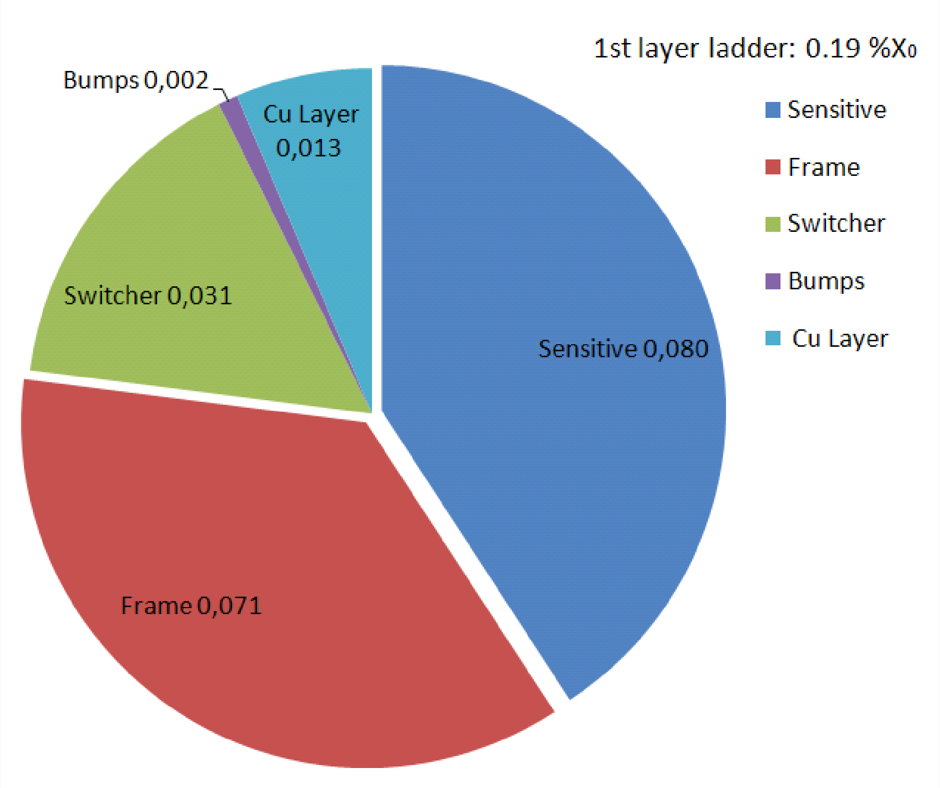
- Half modules must be mechanically connected to form a complete PXD module

- Face to face gluing
- Reinforcement with 3 ceramic inserts

- Resilient to bow up to 1mm and a tension of ~40N



Material budget within acceptance



→ 0.19 %X_0 in total

Silicon contribution (0.15%)

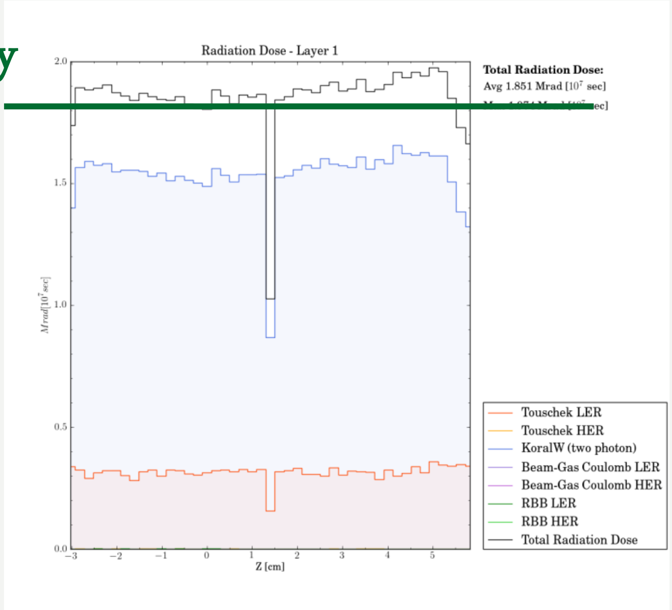
Background and Radiation

Backgrounds:

- Touschek scattering (intra-bunch scattering)
- Synchrotron radiation
- Beam-gas scattering

- Radiative Bhabha
- 2-photon process generated electrons

1.9Mrad/y



All backgrounds / Layer 1

- Latest estimate L1/L2: 1.9Mrad/y / 0.6Mrad/y
- Expected PXD occupancy ~0.9%/0.4% inner/outer layer

System layout

- Zero suppression on module level
- Online pattern recognition to reject background
- Online silicon only tracking