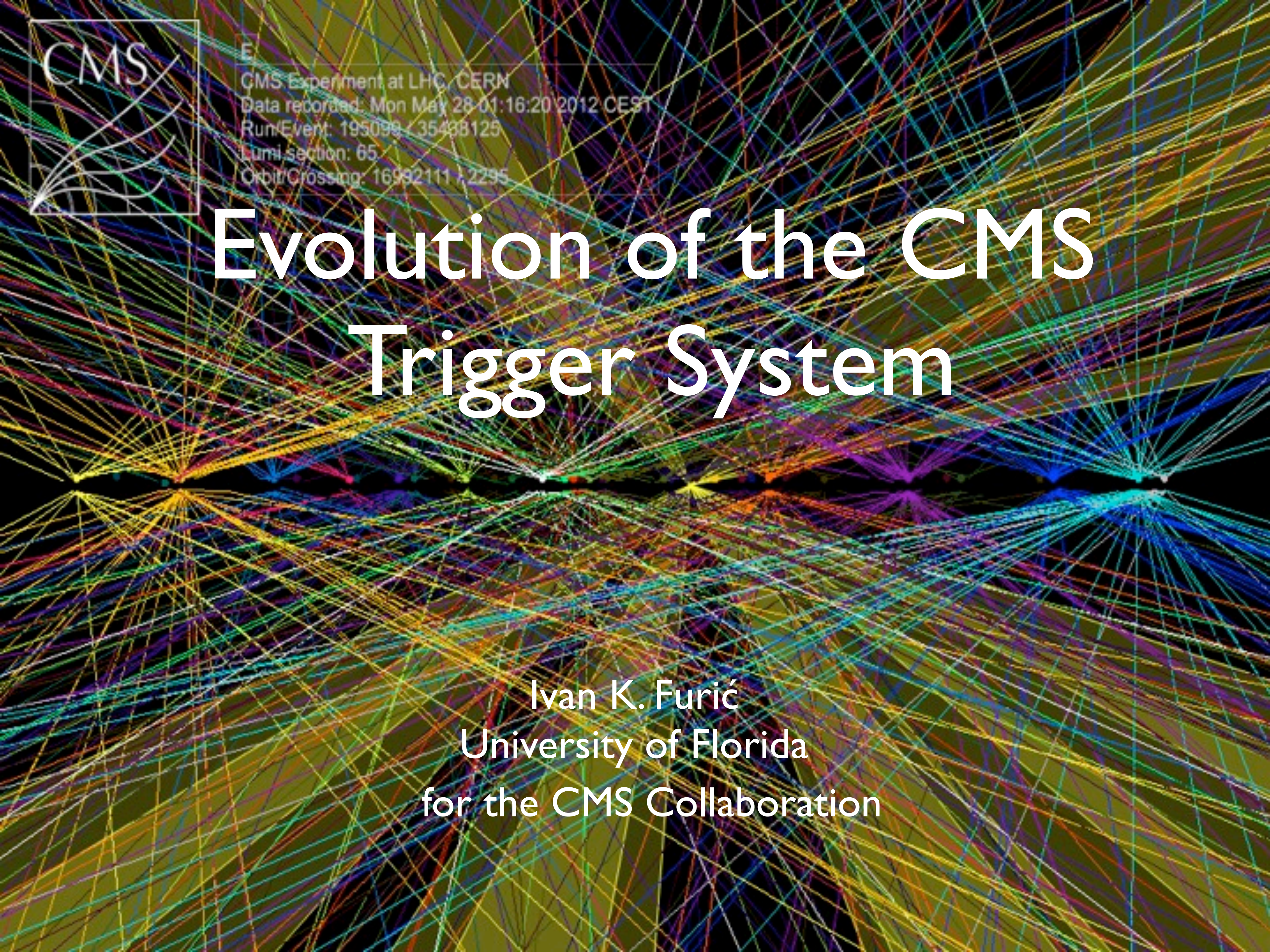


Evolution of the CMS Trigger System

Ivan K. Furić
University of Florida
for the CMS Collaboration

Why upgrade the trigger?

- need more data to measure Higgs properties and make further discoveries, the LHC will deliver this
- constrained with the same trigger rates in the near future
- simply raising thresholds is a bad strategy, cuts into phase space for the studies and negates effect of extra luminosity
- need to have better algorithms and more flexibility in combining requirements, eventually add tracker to trigger
- maintenance and obsolescence - electronics have advanced since the original trigger system was designed and built
    - can build something simpler and easier to maintain now

LHC / CMS schedule

- 2013-2014 first "long shutdown" ("LS 1")
  - start upgrading part of trigger electronics
- 2015-2017 data taking @ ($\sqrt{s}$ = 14 TeV)
  - LHC may exceed design luminosity (10^{34} $cm^{-2}s^{-1}$) and run at higher than design pile-up ! (original design: ~20 interactions per bunch crossing)
  - during this period evolve to improved system (pixel detector upgrade ?)
- 2018-2019 second "long shutdown" ("LS 2")
- 2022-2023 third "long shutdown" ("LS 3")
  - silicon strip tracker upgrade
  - plans to use tracker in Level-1 Trigger
- schedule may change over time

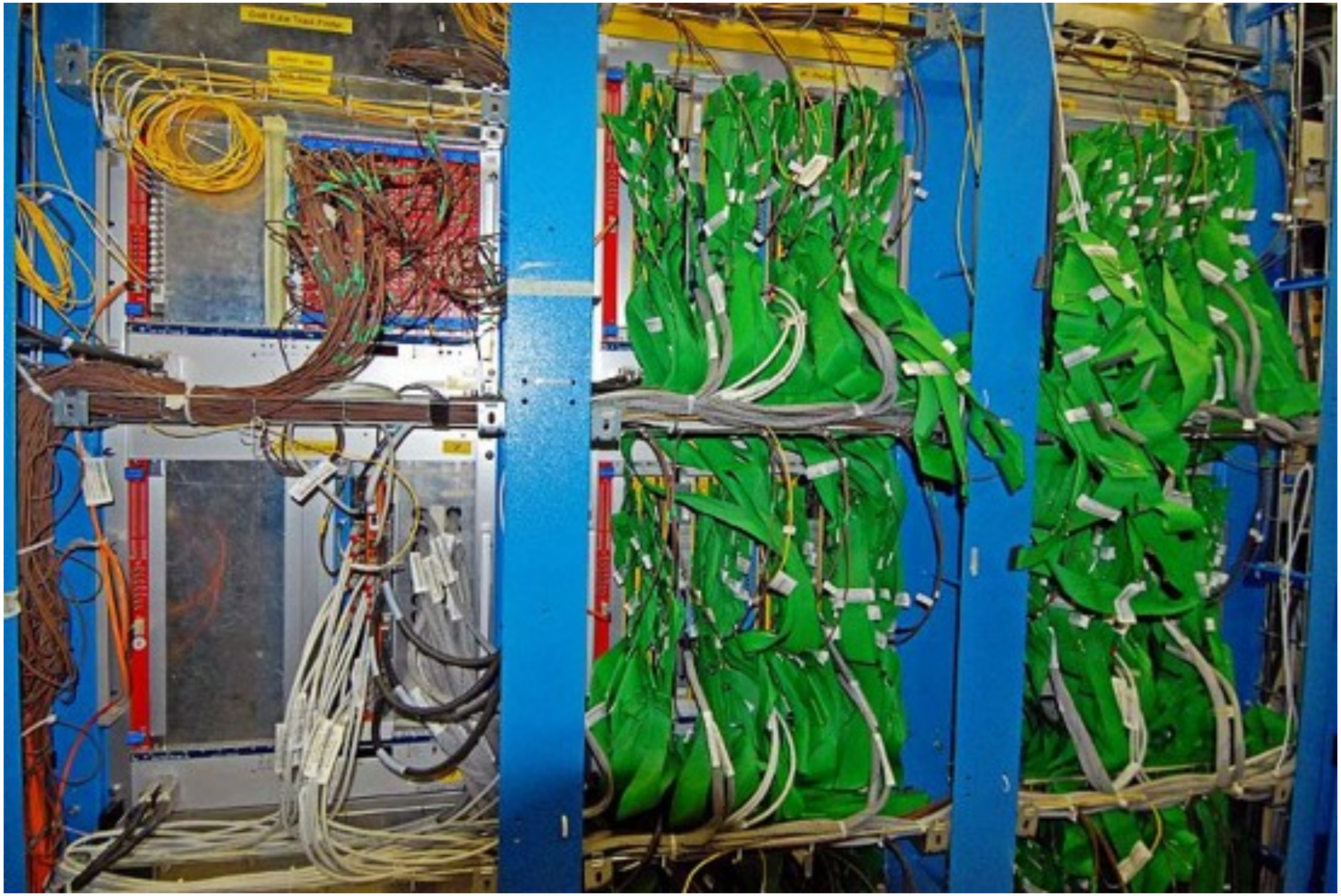
Phase-1 upgrade strategy

- calorimeter trigger
  - higher precision in transverse energy (E_T), (η, φ)
  - flexibility for more complex algorithms (pile-up subtraction, τ-jets etc.)
  - more candidate objects
- muon trigger
  - higher precision in transverse momentum (p_T), (η, φ)
  - more candidate objects
- global trigger
  - more (sophisticated) algorithms (current limit: 128)
  - now: multiple objects, simple angular correlations
  - future: mass (invariant + transverse), more complex correlations

Phase-1 upgrade technology

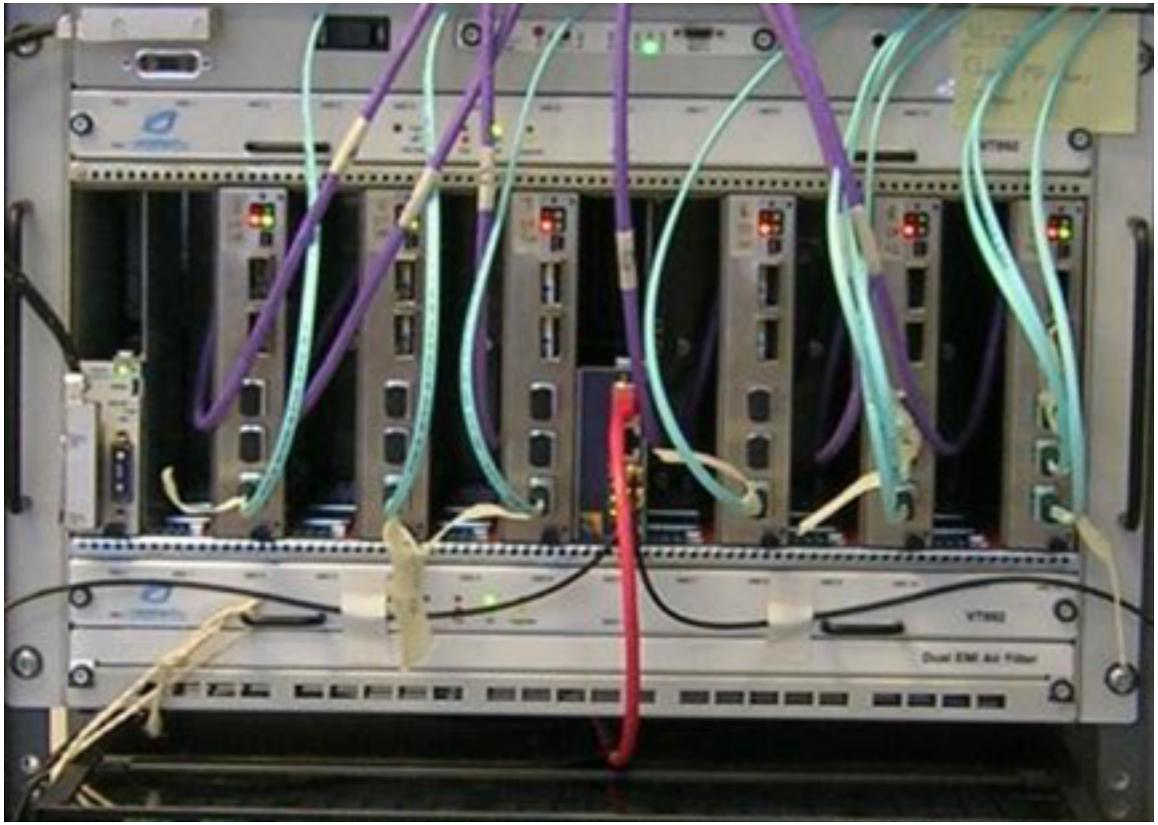
- system consists of many different custom electronics modules
  - VME based electronics implemented in FPGAs and ASICs
  - maintenance and spare-module management problematic
- in future aim for higher integration
  - use larger FPGAs, build system in more compact way (fewer, more generic / interchangeable boards)
- use standardized electronics where possible
  - custom built but same for many systems
  - partly also COTS (Commercial off-the-shelf) components
  - new form factor: μTCA (Micro Telecommunications Computing Architecture)
- use optical links
  - higher data rates (higher precision, more trigger objects)
  - less space for connectors (μTCA instead of 9U-VME)

Many parallel galvanic connections

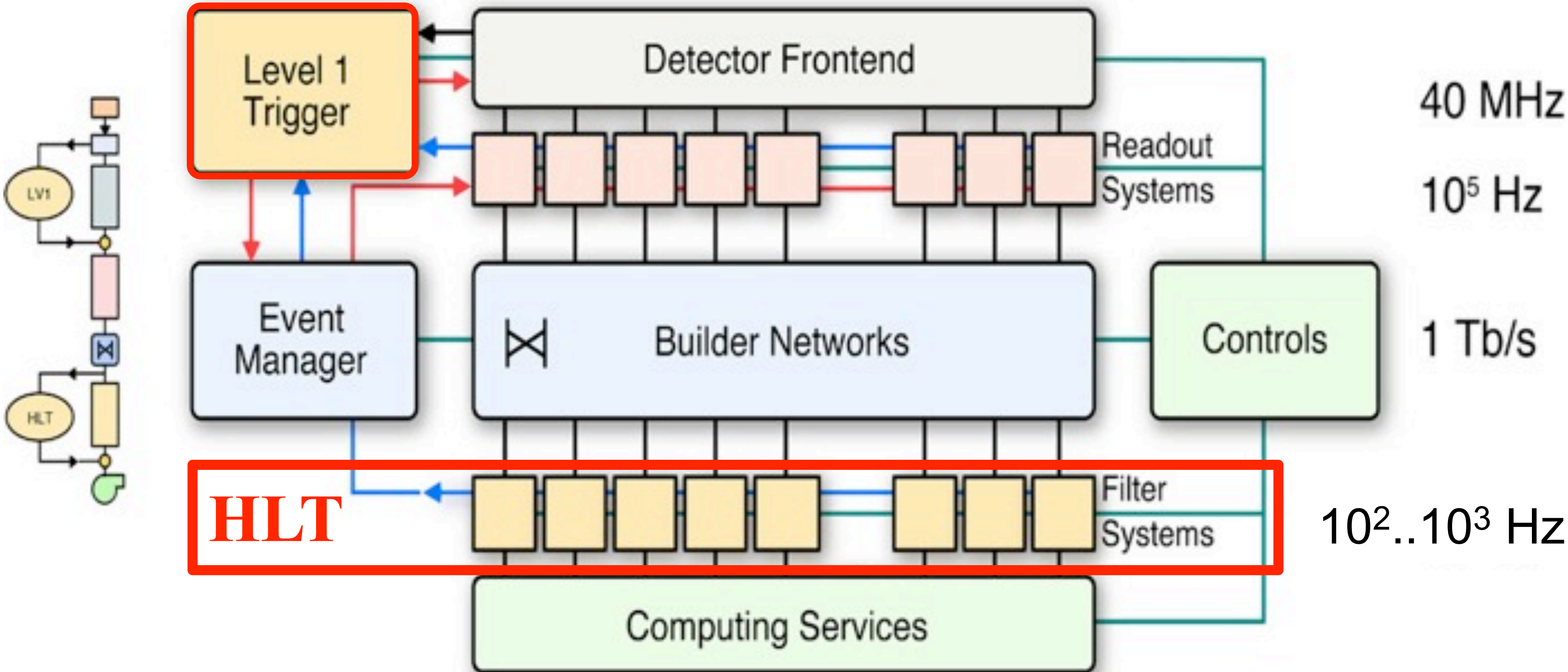


Example: Drift Tube Track Finder (part of muon trigger)

µTCA crate and module



Reminder: CMS Trigger & DAQ



- L1 design and performance - see Jim Brooke's talk earlier
- HLT performance - see Stéphanie Beauceron's talk earlier

Level-1 Trigger latency

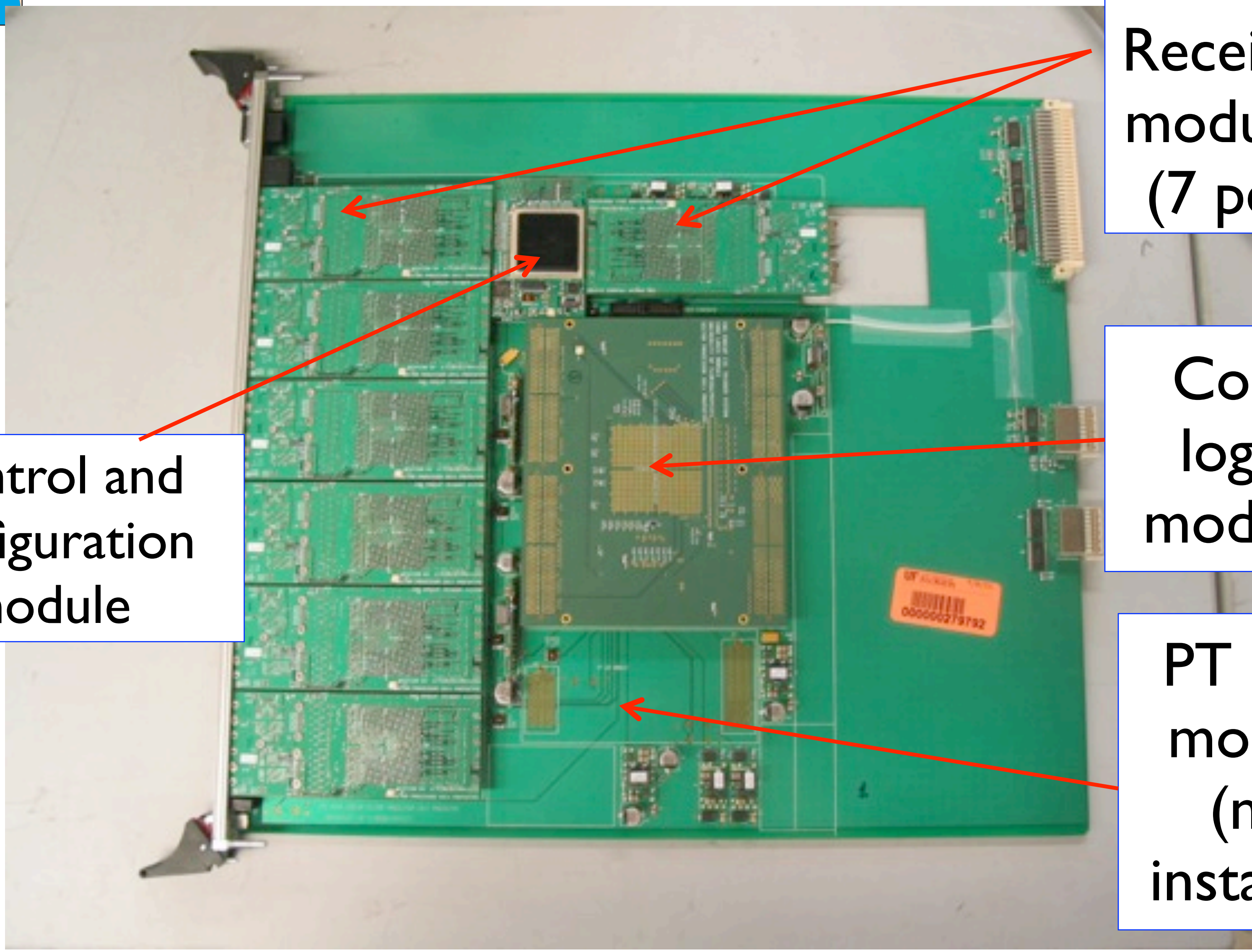
- presently ~ 4 μs (~ 160 LHC bunch crossings), due to tracker pipeline length
- will be increased only during tracker upgrade ("Long Shutdown 3", ~2023)

- trigger upgrade will have to fit into same latency budget
- challenge because of optical links (parallel-serial conversion increases latency)
- we have some reserve latency in the pipeline

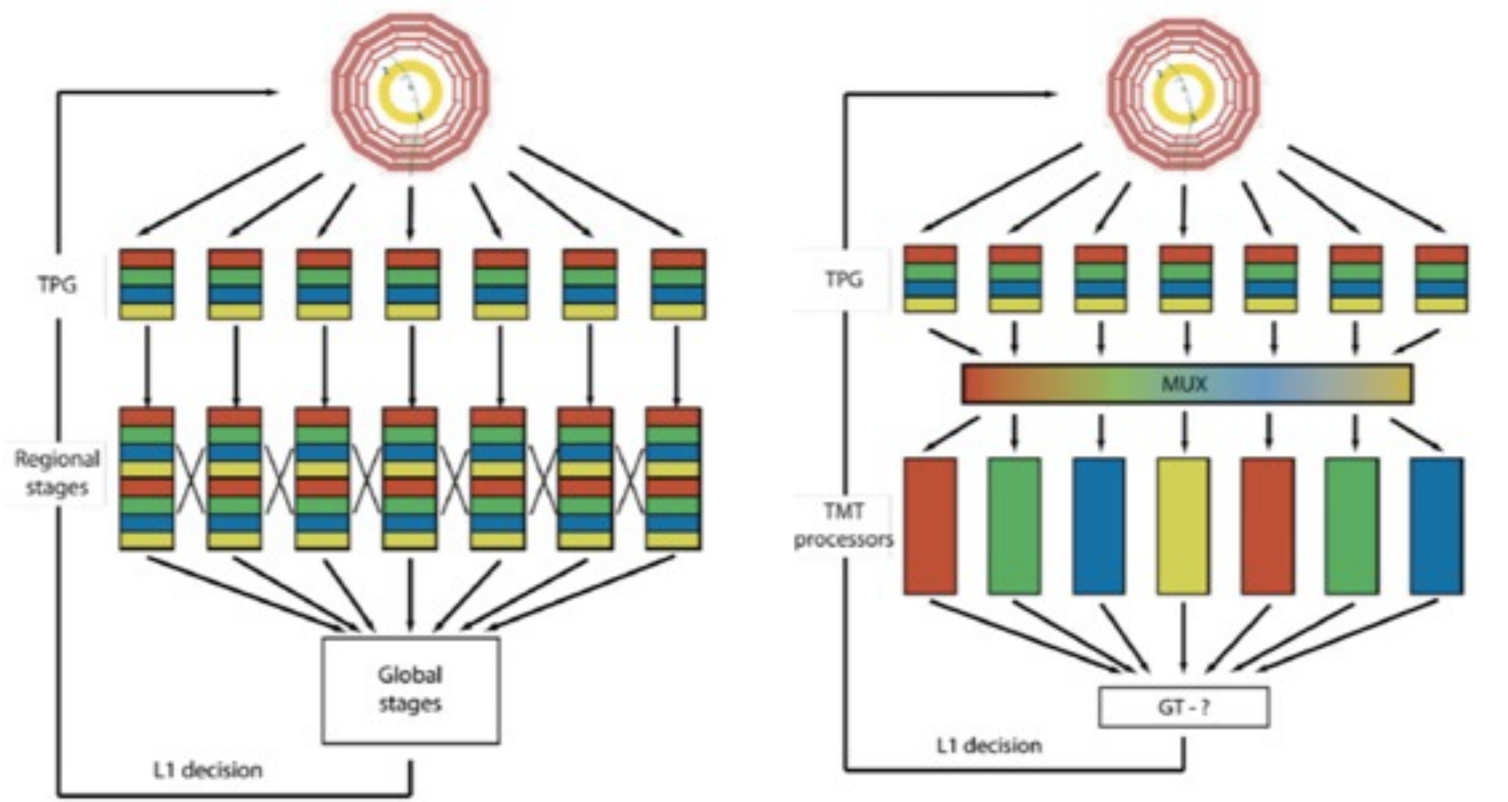
Muon trigger upgrade

- Cathode Strip Chambers (CSC) trigger
  - outermost chambers to be added in 2013-2014
  - improve p_T resolution and thus reduce rate
  - increasing rate of trigger primitives
  - current design ($\Delta\varphi$ comparisons) does not scale well
  - switch to pattern matching system to accommodate higher occupancy
- Drift Tube (DT) trigger
  - move front-end electronics ("sector collectors") from experimental cavern to electronics cavern (2013)
  - all trigger electronics close to Global Trigger, always accessible in radiation-safe area
  - later: performance upgrade (higher resolution)

CSC Sector Processor VME Prototype



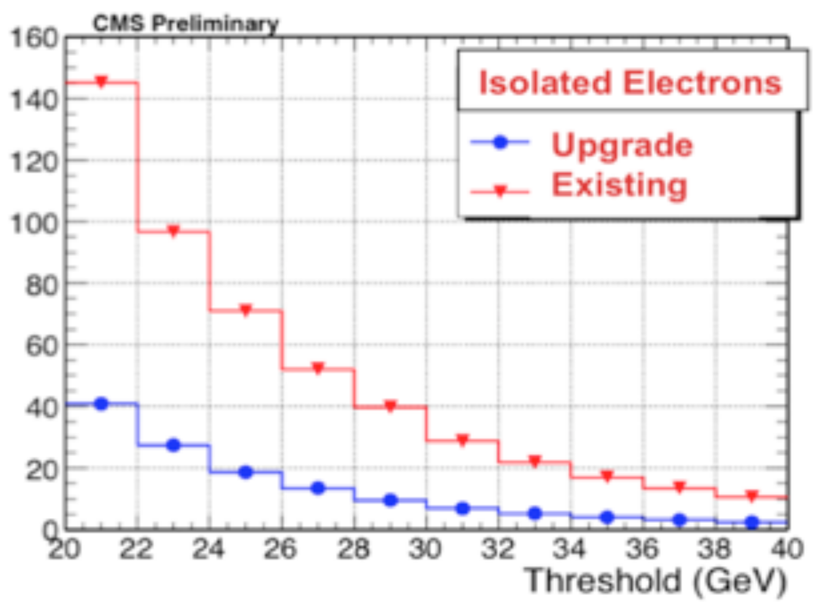
Calorimeter trigger

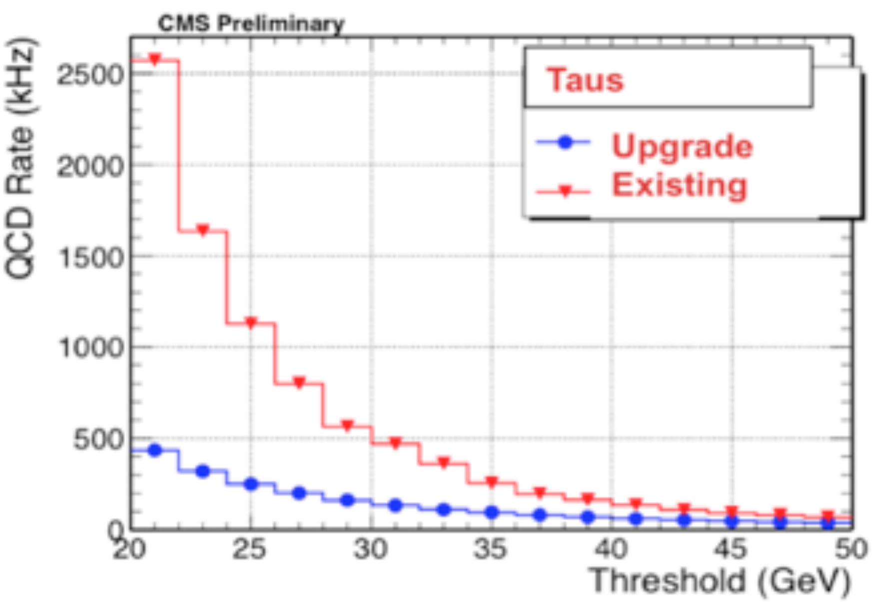


- two alternative architectures being proposed
- parallel triggering systems vs. time-multiplexed trigger
- similar hardware, different connections

Calorimeter trigger upgrade

- improve resolution in coordinates
  - azimuth φ and pseudorapidity η
- improve identification of tau jets
  - better isolation criteria
- further improve e/gamma isolation determination





Global Trigger Upgrade

- continue centralizing all final decision taking in one crate
- Global Muon Trigger receives inputs from the three muon systems
- Global Trigger Logic and Trigger Control System combined in one μTCA module
- use of big FPGAs will allow much more complex logic
  - large number of high-speed IO links and logic cells
  - big lookup tables, floating-point operations in DSPs
- first step: port existing functionality into new electronics
- then: gradually improve functionality and increase complexity through firmware updates

Level-1 Global Trigger Upgrade

- optical connection from calorimeter trigger system to global trigger installed - first application of upgrade links

High Level Trigger (HLT)

- now: ~ 13 000 CPU cores, ~ 20 000 event processors
- more and faster computers will allow for more calculation time, more complex algorithms
  - ~160 → ~500 (1000) ms per event for 100 (200) PU

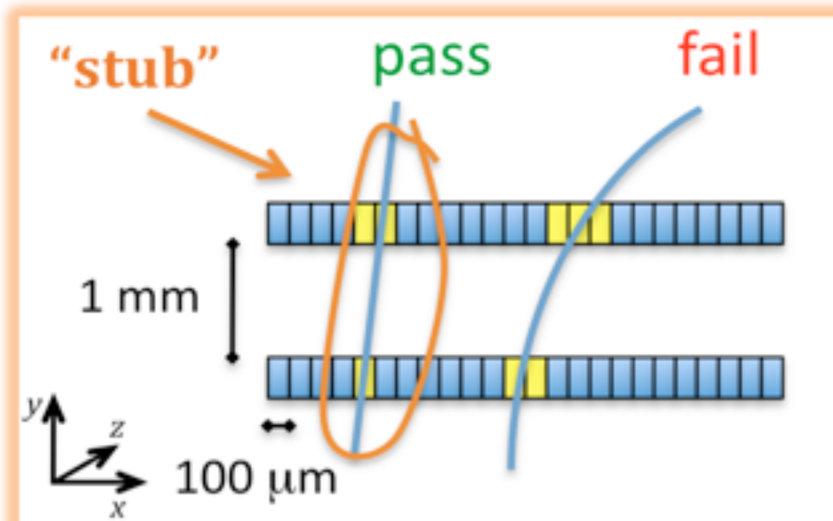
- currently using shared memory
  - possibly replace by message queues
  - data exchange between applications by posting and retrieving from queue

- isolate HLT trigger algorithms from DAQ software
  - move to file-based processing, using SSD's
  - run offline code directly in High-Level Trigger

more distant future:

Level-1 Tracker trigger

- at present, Tracker is used only in High-Level Trigger
- plan to use in Level-1 Trigger after replacement (2022-23)
- aim for higher tracker pipeline latency (3.2 → 6 μs)
  - "push" and/or "pull" architecture
  - tracker information available at HLT as "seeds"
- idea: select high-momentum tracks at local level
  - look for low bending in adjacent strip modules
  - track selection by ASICs mounted on sensors
  - several technical solutions are being investigated

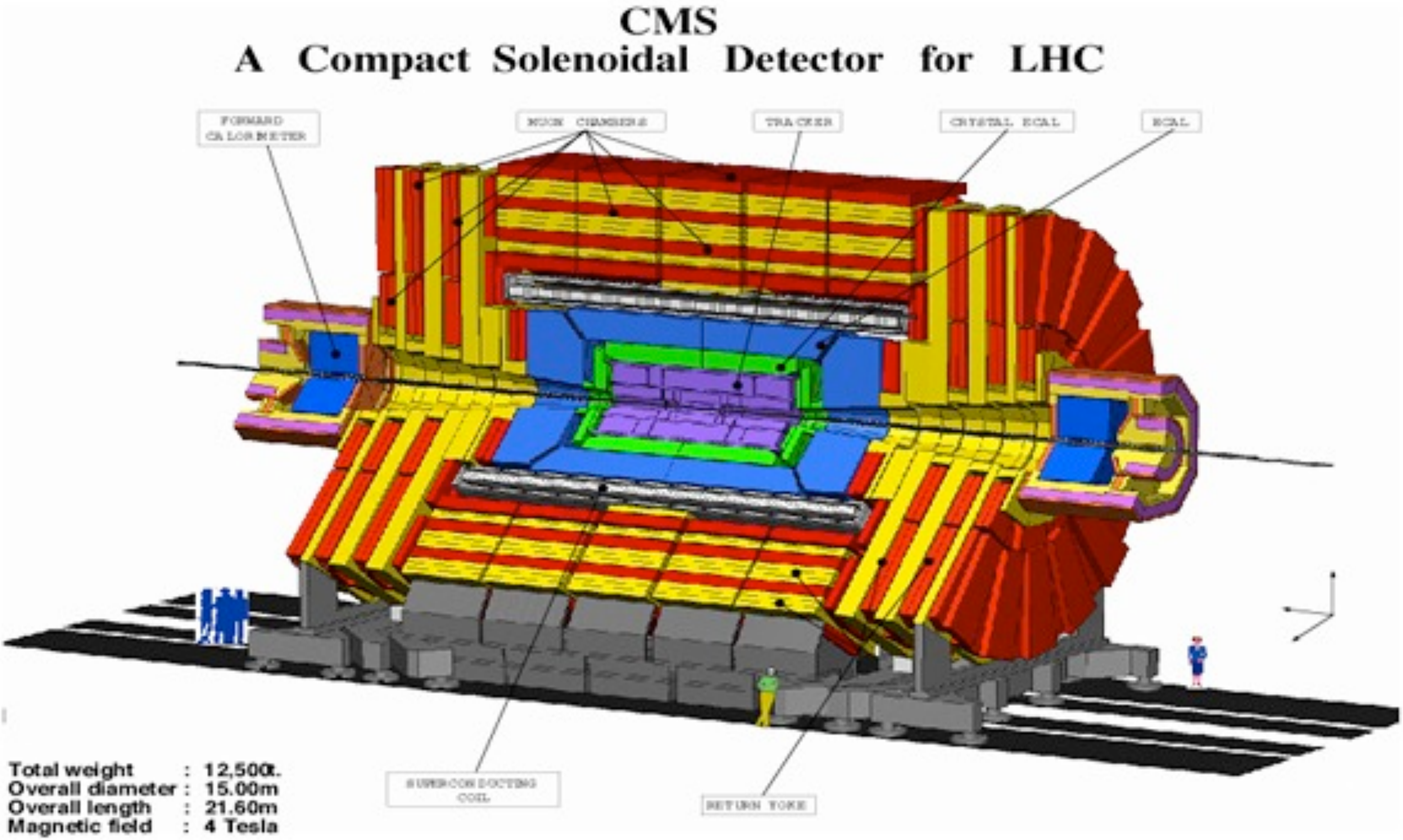


Conclusions

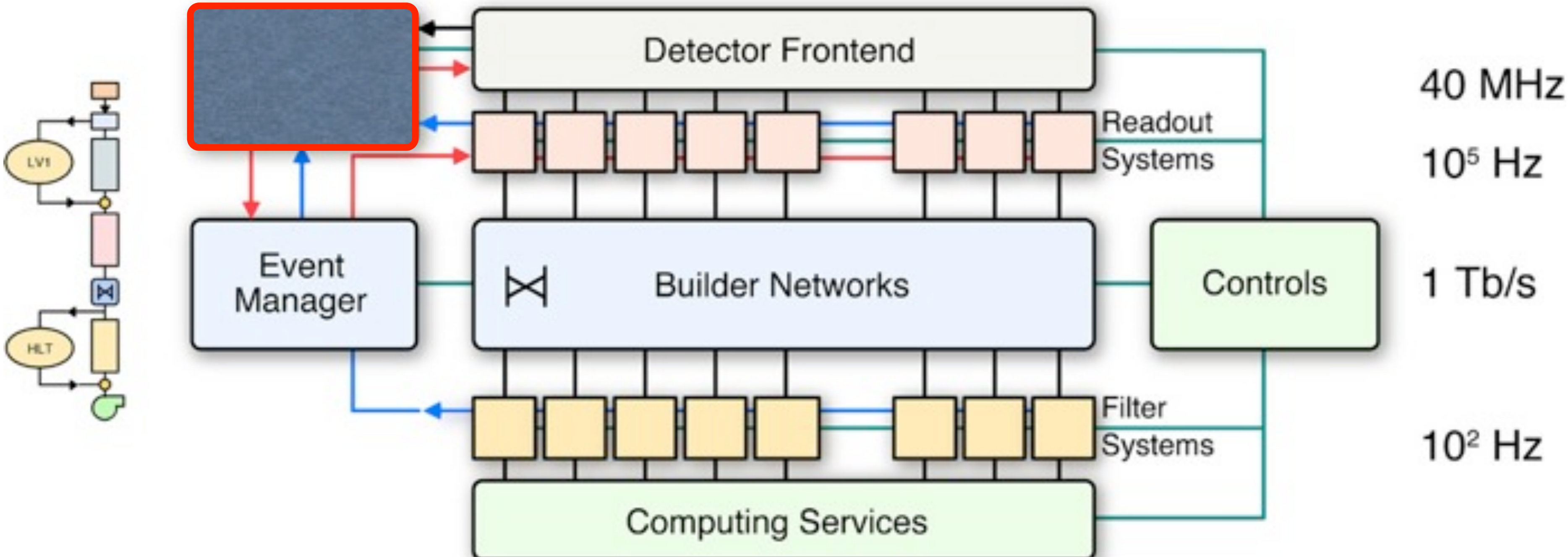
- LHC beam intensity development makes trigger upgrade work mandatory
  - otherwise we lose much of the data
- gradual process over significant time span (debug new systems without risking physics data loss)
- physics studies and R&D under way
- Technical Design Report to be ready early next year
- first steps commence next year (2013)

BACKUP

The Compact *MUON*



CMS Trigger & DAQ



- LHC beam crossing rate is 40 MHz & at full Luminosity of 10^{34} cm^{-2}s^{-1} yields 10^9 collisions/s
- Reduce to 100 kHz output to High Level Trigger and keep high-P_T physics
- Pipelined at 40 MHz for dead time free operation
- Latency of only 4 μsec for collection, decision, propagation

Signals used by the first-level trigger

- muons
  - tracks
  - several types of detectors (different requirements for barrel and endcaps):
  - in ATLAS:
    - RPC (Resistive Plate Chambers): barrel
    - TGC ("Thin Gap Chambers"): endcaps
    - not in trigger: MDT ("Monitored Drift Tubes")
  - in CMS:
    - DT (Drift Tubes): barrel
    - CSC (Cathode Strip Chambers): endcaps
    - RPC (Resistive Plate Chambers): barrel + endcaps
- calorimeters
  - clusters
  - electrons, jets, transverse energy, missing transverse energy
  - electromagnetic calorimeter
  - hadron calorimeter
- only in high-level trigger: tracker detectors
  - silicon strip and pixel detectors, in ATLAS also straw tubes
  - cannot be read out quickly enough

How does the trigger actually select events ?

- the first trigger stage has to process a limited amount of data within a very short time
  - relatively simple algorithms
  - special electronic components
    - ASICs (Application Specific Integrated Circuits)
    - FPGAs (Field Programmable Gate Arrays)
  - something in between "hardware" and "software": "firmware"
    - written in programming language ("VHDL") and compiled
    - fast (uses always same number of clock cycles)
    - can be modified at any time when using FPGAs
- the second stage ("High-Level Trigger") has to use complex algorithms
  - not time-critical any more (all detector data have already been retrieved)
  - uses a "computer farm" (large number of PCs)
  - programmed in high-level language (C++)

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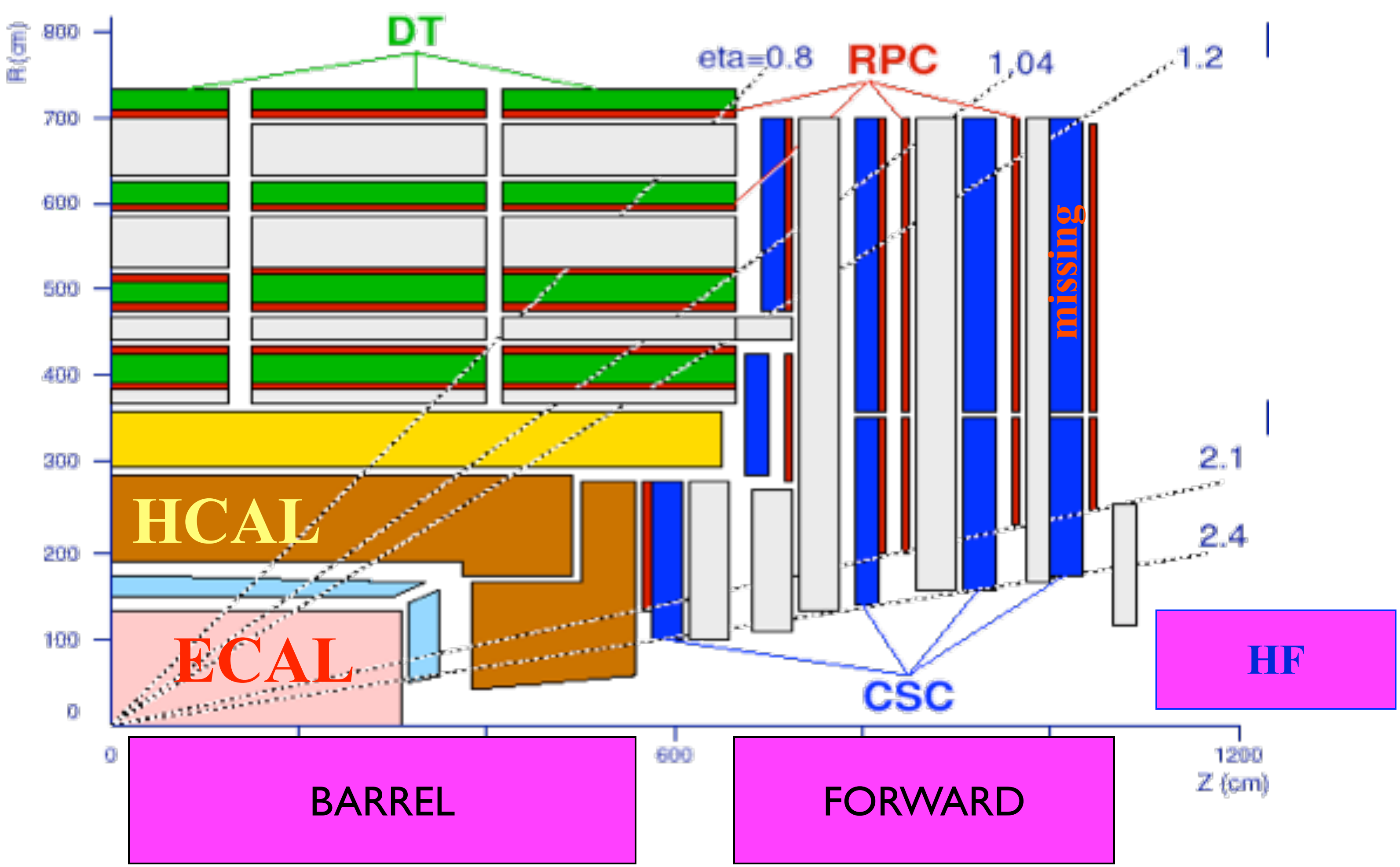
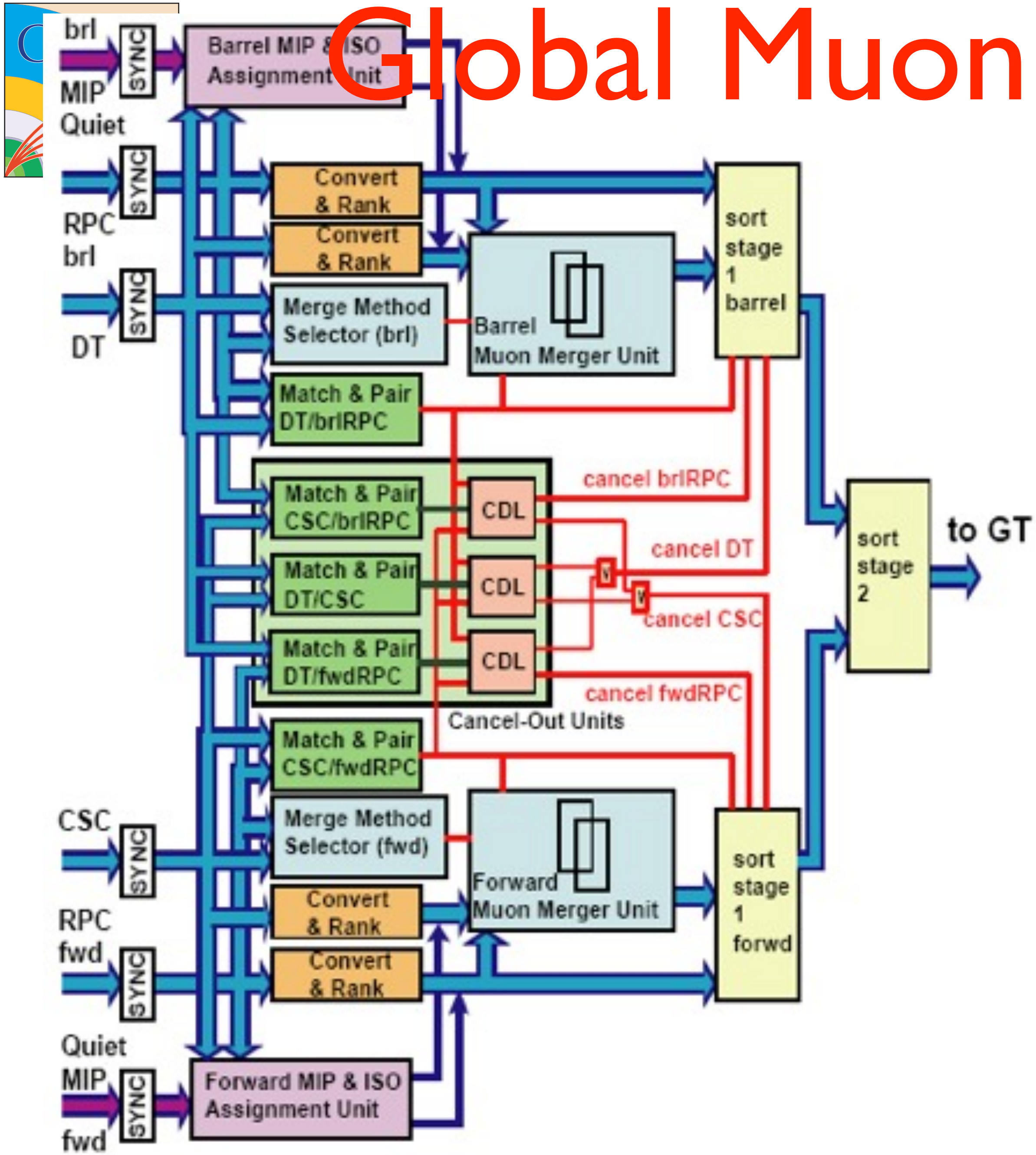
```
pre_algo_a(54) <= tau_2_s(2);
pre_algo_a(55) <= tau_2_s(1);
pre_algo_a(56) <= muon_1_s(10) AND ieg_1_s(2);
pre_algo_a(57) <= muon_1_s(6) AND ieg_1_s(28);
pre_algo_a(58) <= muon_1_s(8) AND (ieg_1_s(25) OR eg_1_s(7));
pre_algo_a(59) <= muon_1_s(9) AND (jet_1_s(9) OR fwdjet_1_s(5) OR tau_1_s(26));
pre_algo_a(60) <= muon_1_s(4) AND (jet_1_s(8) OR fwdjet_1_s(4) OR tau_1_s(25));
pre_algo_a(61) <= muon_1_s(7) AND (jet_1_s(4) OR fwdjet_1_s(20) OR tau_1_s(16));
pre_algo_a(62) <= muon_1_s(3) AND (jet_1_s(20) OR fwdjet_1_s(15) OR tau_1_s(10));
pre_algo_a(63) <= muon_1_s(2) AND tau_1_s(9);
pre_algo_a(64) <= muon_1_s(1) AND tau_1_s(20);
pre_algo_a(65) <= ieg_1_s(26) AND (jet_1_s(7) OR fwdjet_1_s(3) OR tau_1_s(24));
pre_algo_a(66) <= ieg_1_s(24) AND (jet_1_s(19) OR fwdjet_1_s(14) OR tau_1_s(8));
pre_algo_a(67) <= ieg_1_s(10) AND (jet_1_s(5) OR fwdjet_1_s(1) OR tau_1_s(19));
```

TRIGGER

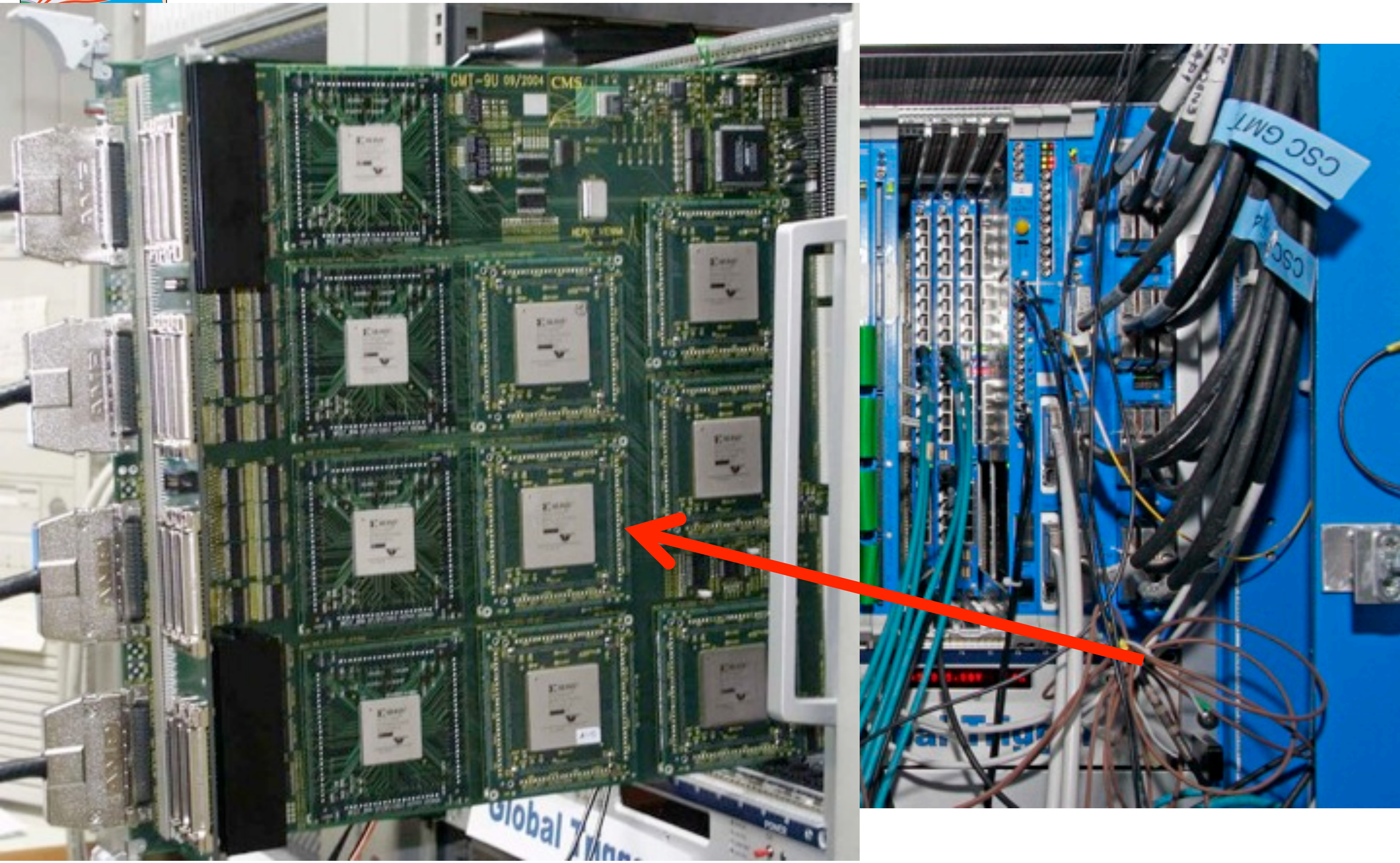

DT
eta=0.8
RPC
1.04
1.2
R (cm)
800
700
600
500
400
300
200
100
0
missing
2.1
2.4
HCAL
ECAL
CSC
HF
0
600
1200
Z (cm)
BARREL
FORWARD

Global Muon Trigger



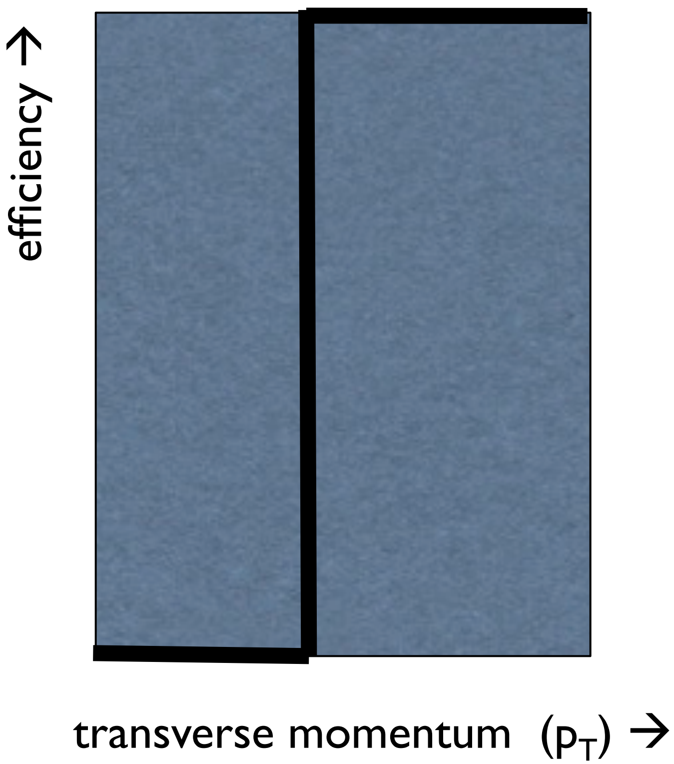
- match & merge
  - barrel: DT-RPC
  - endcap: CSC-RPC
- cancel duplicates
  - overlap region: DT-CSC
- sort by momentum and quality

Level-1 muon trigger

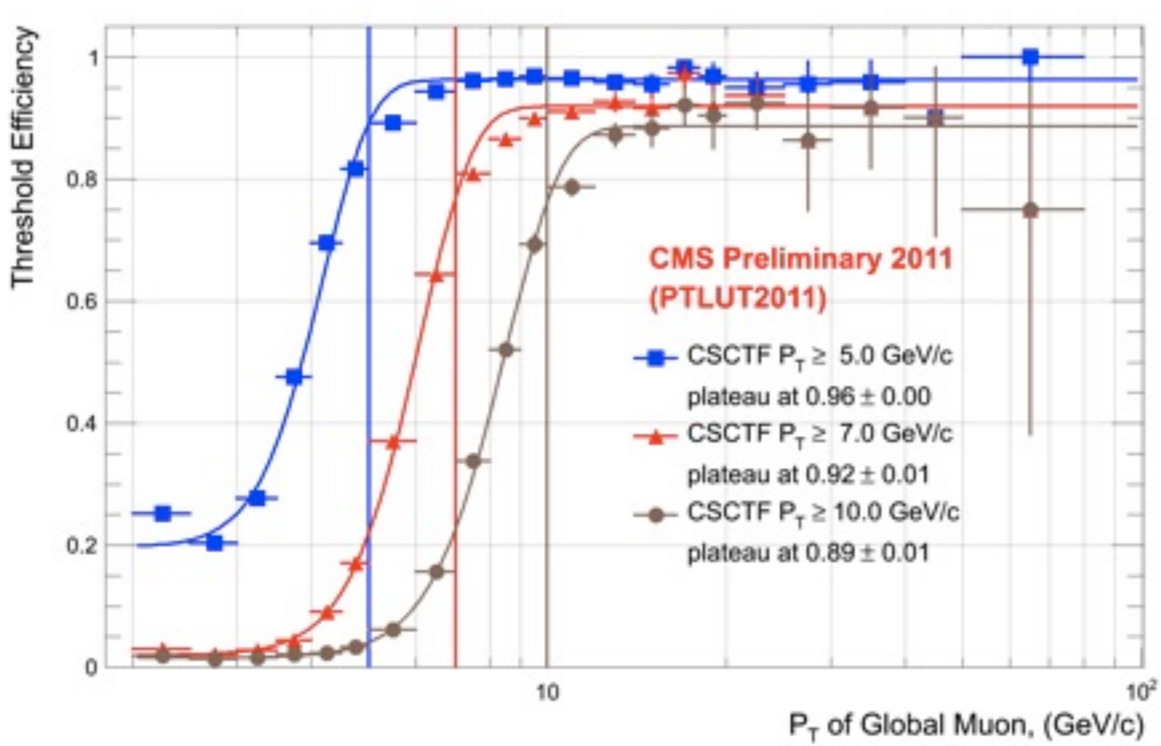


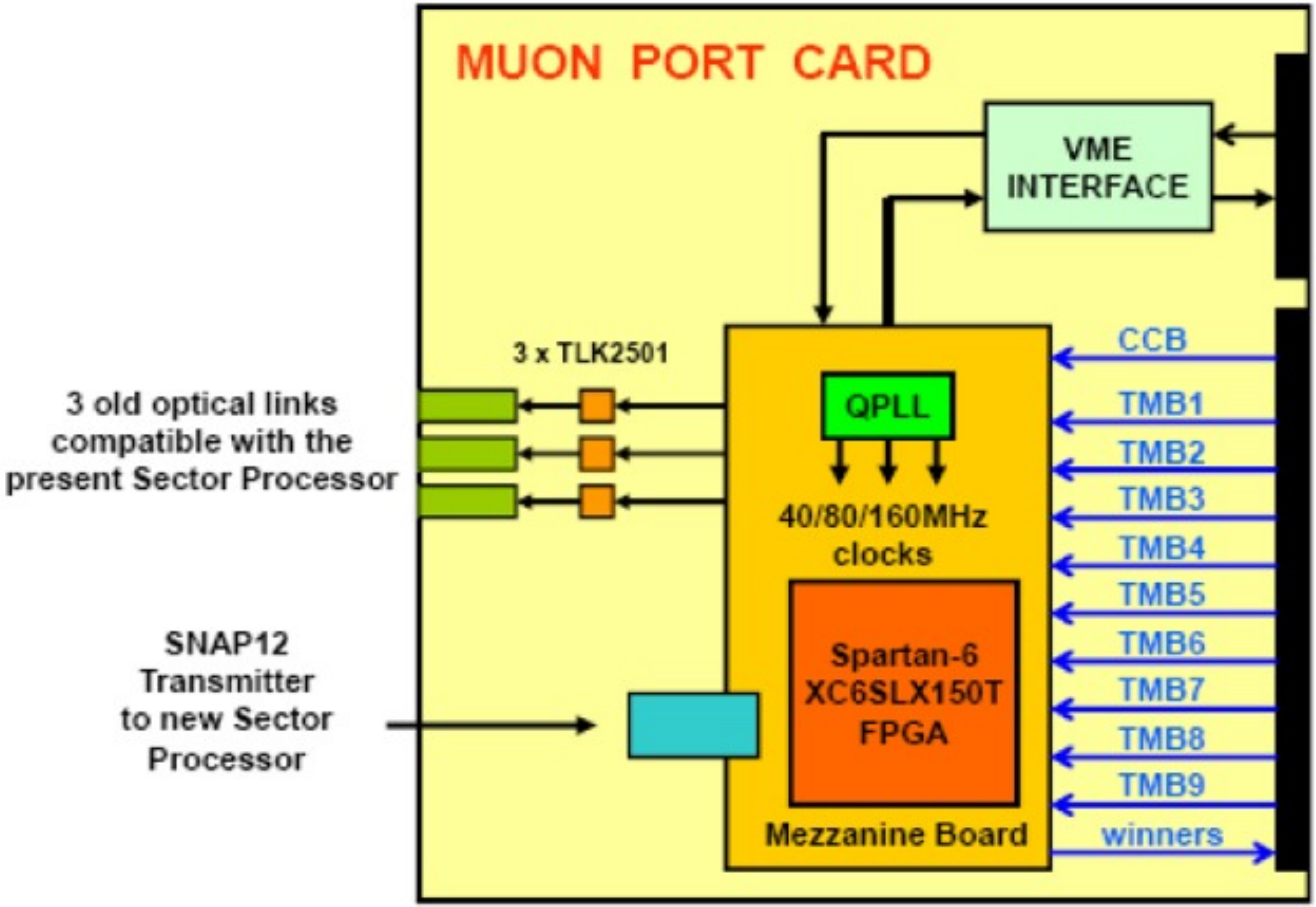
turn-on curves

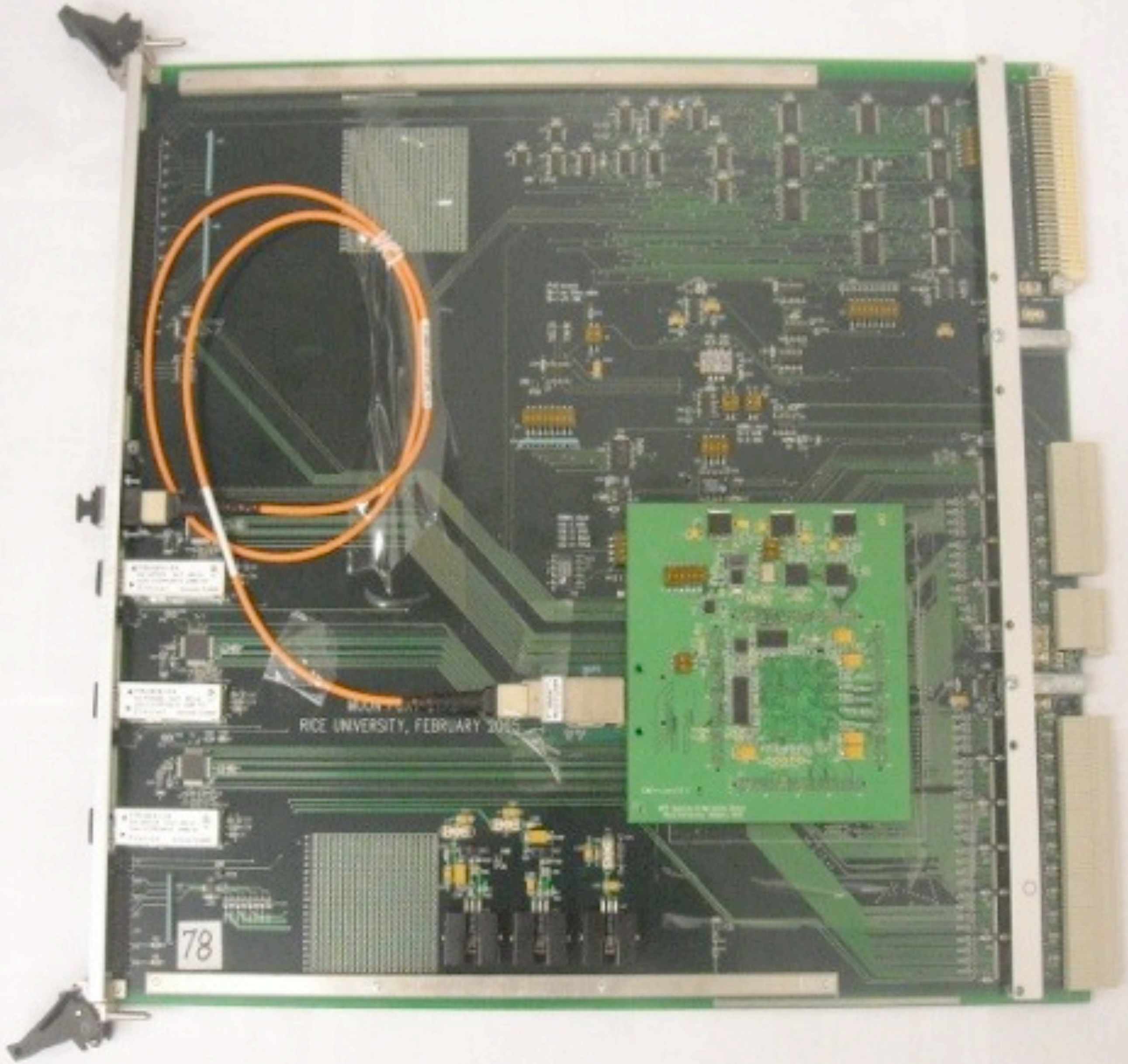
ideal:

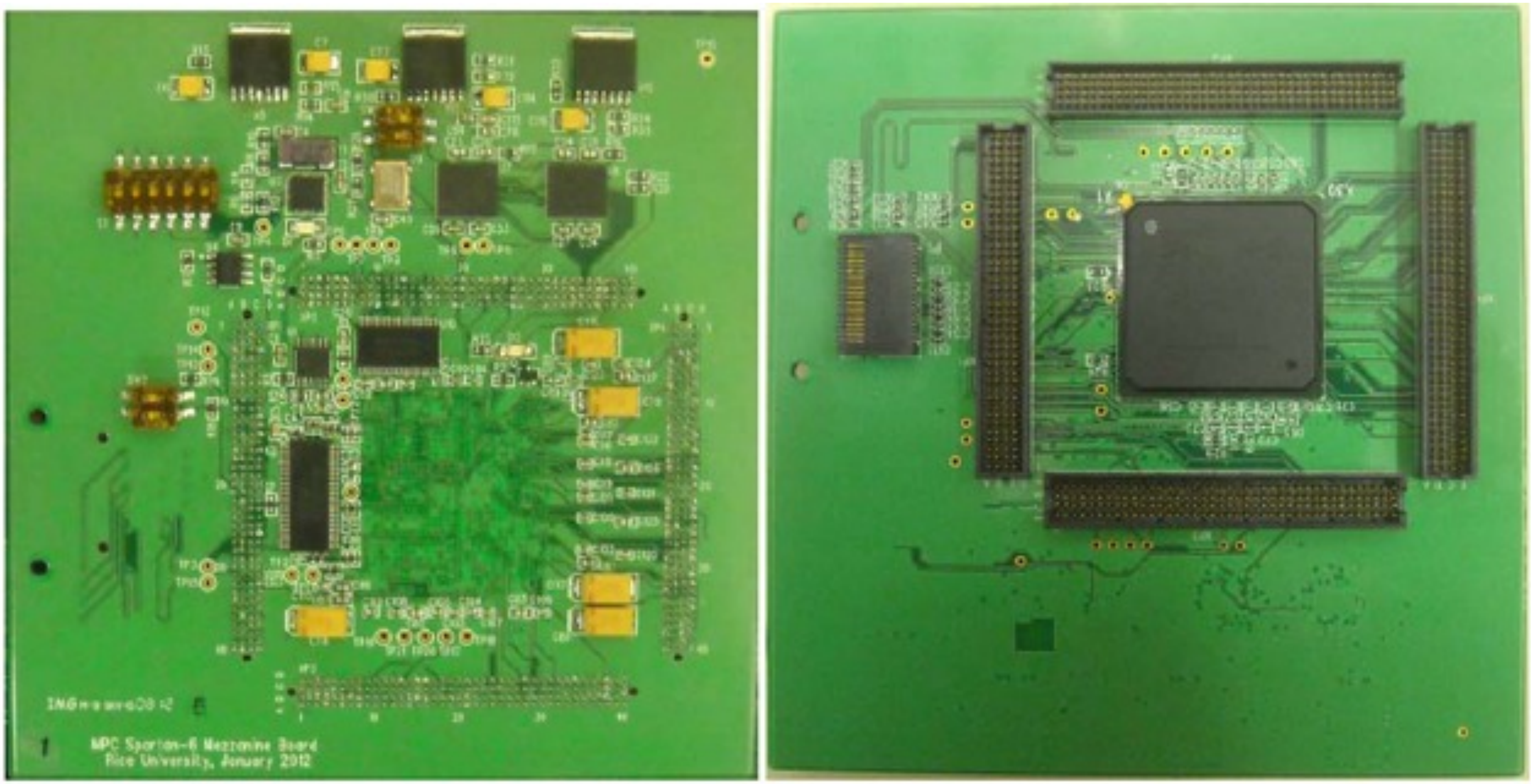


reality:




MUON PORT CARD
VME
INTERFACE
3 x TLK2501
3 old optical links
compatible with the
present Sector Processor
QPLL
40/80/160MHz
clocks
SNAP12
Transmitter
to new Sector
Processor
Spartan-6
XC6SLX150T
FPGA
Mezzanine Board
CCB
TMB1
TMB2
TMB3
TMB4
TMB5
TMB6
TMB7
TMB8
TMB9
winners


RICE UNIVERSITY, FEBRUARY
78


MPC Spartan-6 Mezzanine Board
Rice University, January 2012

Test of MPC to SP10 communication. 8 fibers, 3.2 Gbps each, no errors

MPC prototype (Rice) Based on Spartan-6

SP10 prototype (Florida)

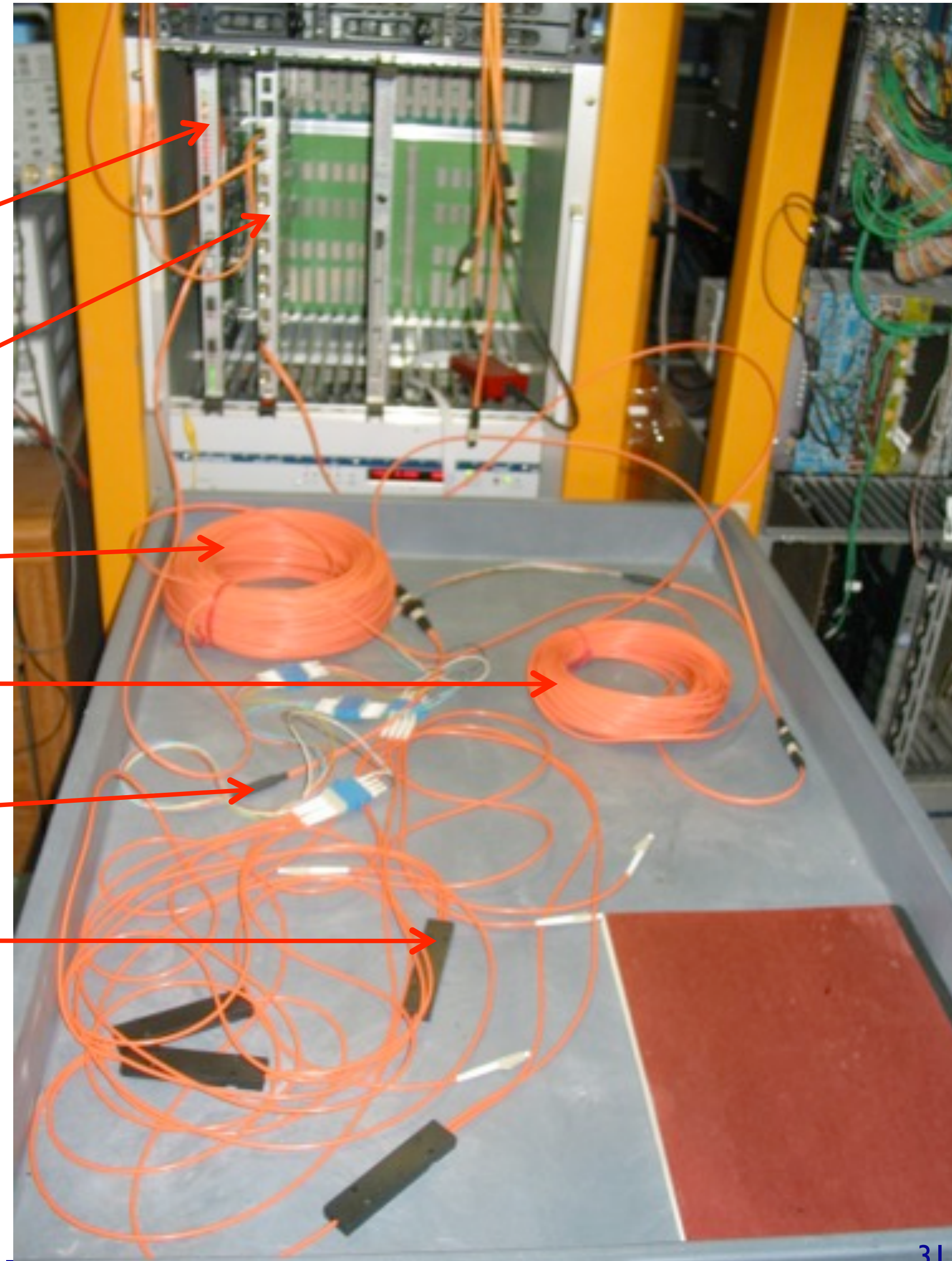
100 meter fiber (12-core)

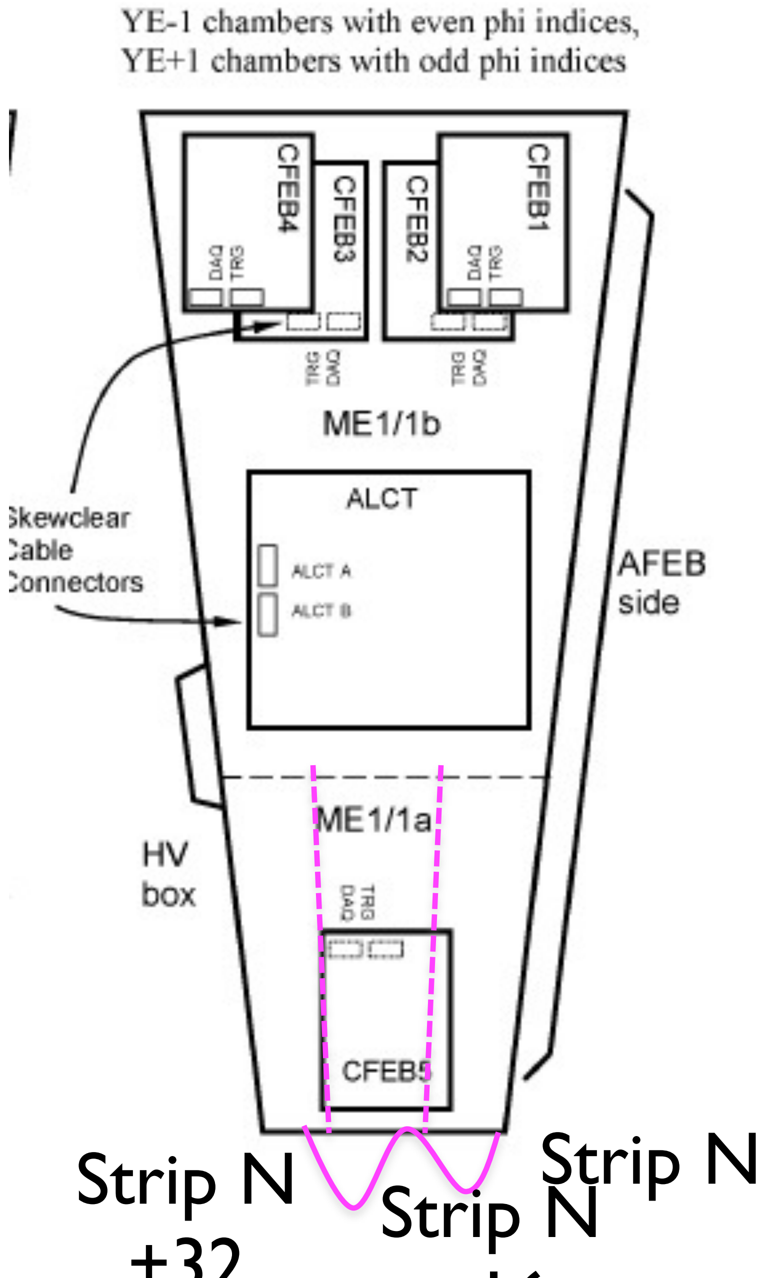
25 meter fiber (12-core)

12-core fiber fanout (2 pcs)

50/50% optical splitter (4 pcs)

Total optical path length: 125 meters + fanouts and splitters




YE-1 chambers with even phi indices,
YE+1 chambers with odd phi indices
CFEB4
CFEB3
CFEB2
CFEB1
DAQ
TRG
ME1/1b
ALCT
ALCT A
ALCT B
kewclear
able
onnectors
AFEB
side
ME1/1a
HV
box
CFEB5
Strip N
+32
Strip N
+16
Strip N

ME11a structure

ME1/1 view (from CMS IN-2007/024)

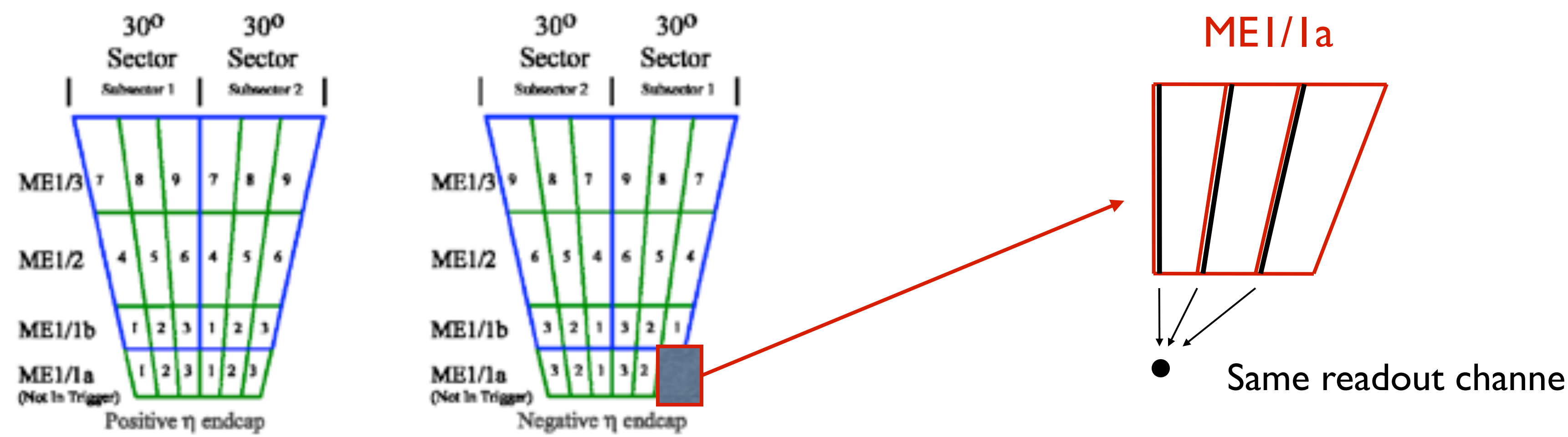


Figure 9. Numbering of CSC chambers within ME1 trigger sectors, as viewed from the IP.

- The 48 strips of ME1/1a are ganged 3:1 in 16 readout channels
- e.g. strips 1 (2), 17 (18) and 33 (34) are ganged together into the 1st (2nd) readout channel
- In the CSCTF LUTs the ϕ value is shifted to the middle of the CFEB
- We will mistake the ϕ assignment at most by 1/3 (with the older assignment up to 2/3)

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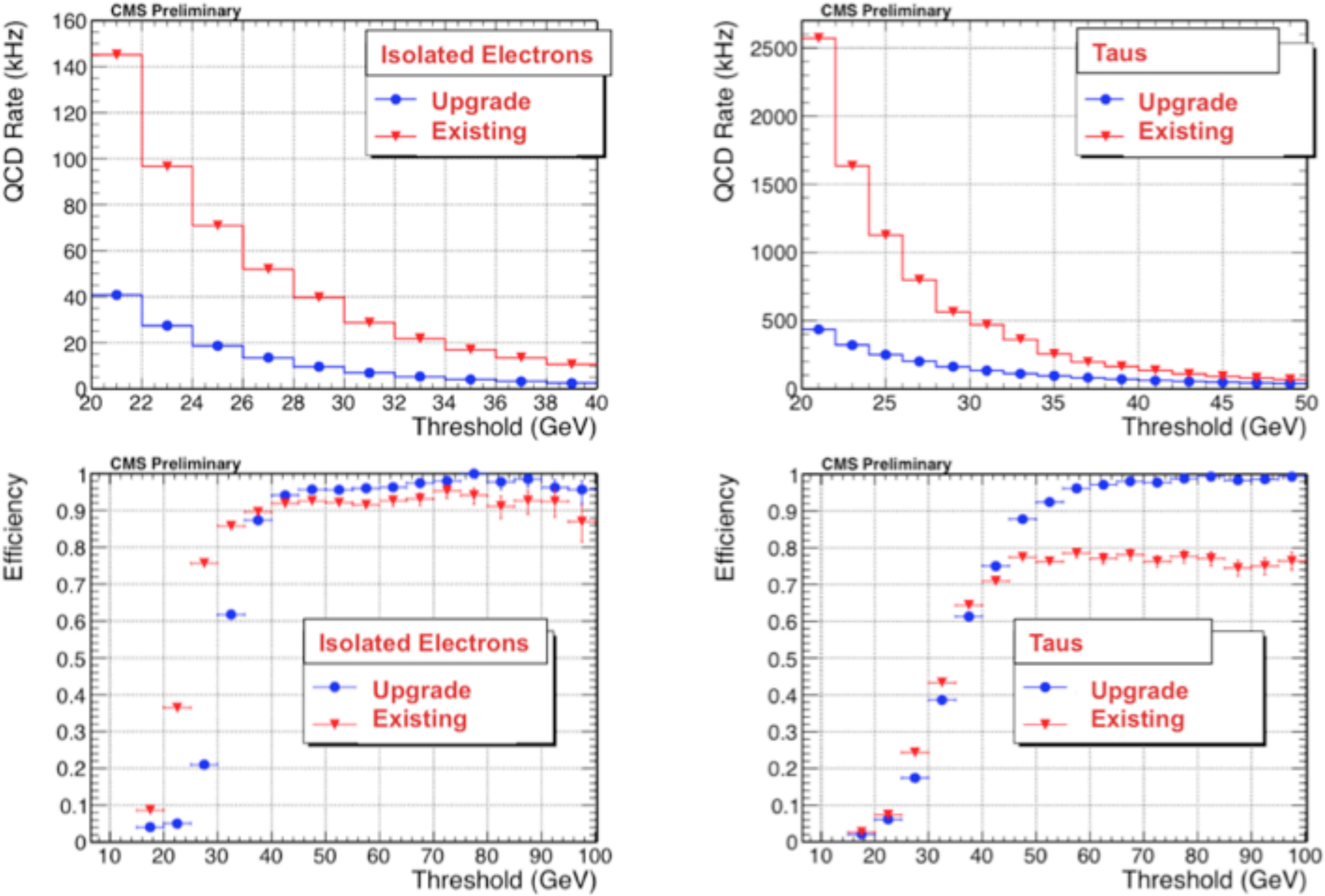
Rates and efficiencies of current and upgraded calorimeter trigger



Parallel running of old

- new trigger systems cannot be commissioned by 2014
  - end of "Long Shutdown 1"
- plan running "old" and "new" systems in parallel
  - trigger with old system
  - record decision proposed by new system
- study and debug new system
- switch to new system during short shutdown
  - Christmas stop
- upgrade work must not jeopardize data taking!

µTCA crate