IReS MAPS Test And Characterization Tools

Why ?

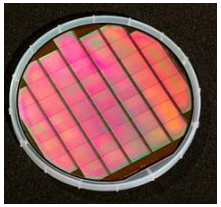
- We must Test & Characterize MAPS Devices – 15 Prototypes in 5 years
- We need a system with on-line monitoring (at least RAW data display)
- No ready DAQ available => Developpment from scratch

How ?

- MAPS Test Benchs + DAQ : Laboratory & Beam Test
- VME Based DAQ System – Used since 2000
- New USB DAQ System – Under developpement (HW – SW)

MAPS Test And Characterization Steps

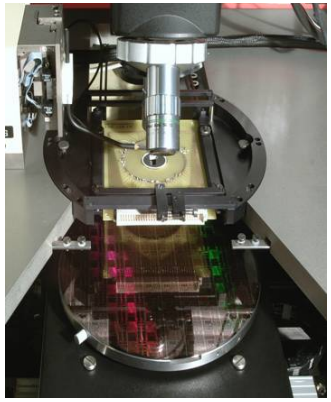
Functionnal Test – Leakage Current
Production Yield [%]

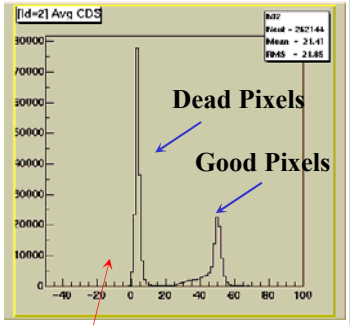


Wafer 6 Inchs
33 MAPS

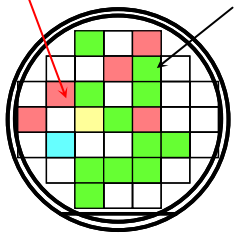
↓

Probe Station



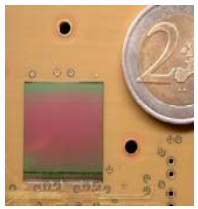


Monitoring



Wafer map

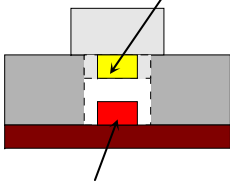
Sensor Calibration – X Photons
Pixel Gain [µV/e-]



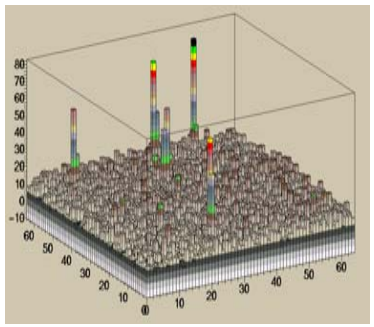
MAPS
&
Source

↓

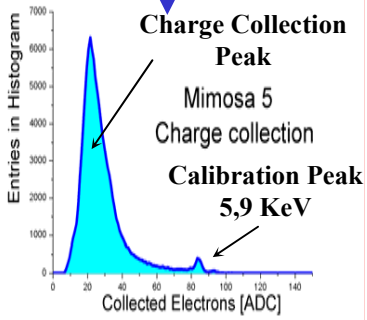
Fe55
Source



MAPS Device

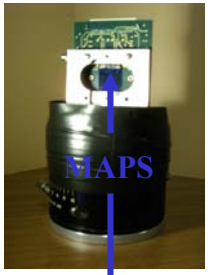


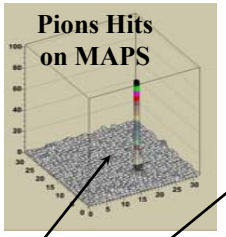
Monitoring

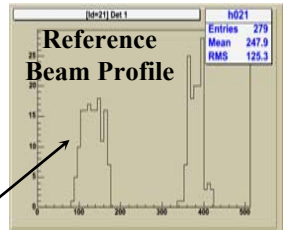


Off-line Analysis

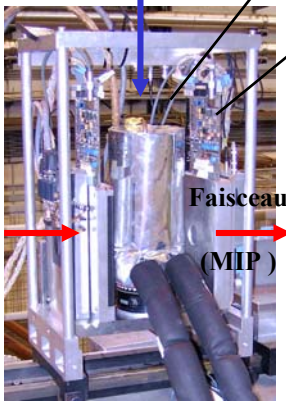
Tracking Performances – Beam Tests
Charge Collection [e-] - Resolution [µm]
Detection Efficiency [%]



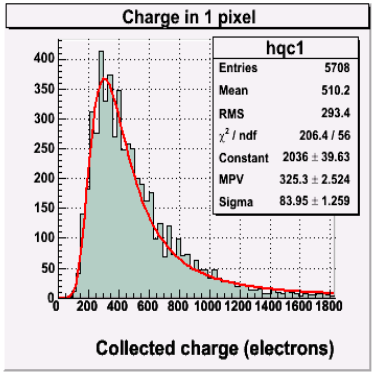




Monitoring



Telescope
Resolution ~ 1 um



Off-line Analysis

- Stat 20 events, 80 Mo, 40 s / MAPS
- 660 Mimosa 5 prototypes tested

- Stat 10^3 events, 4 Go, 40 min/ Run
- Few 10^3 RUNs last 5 years

- Stat 10^4 images, 40 Go, 20 Heures
- Few 10^2 RUNs last 5 years – 4 weeks / year

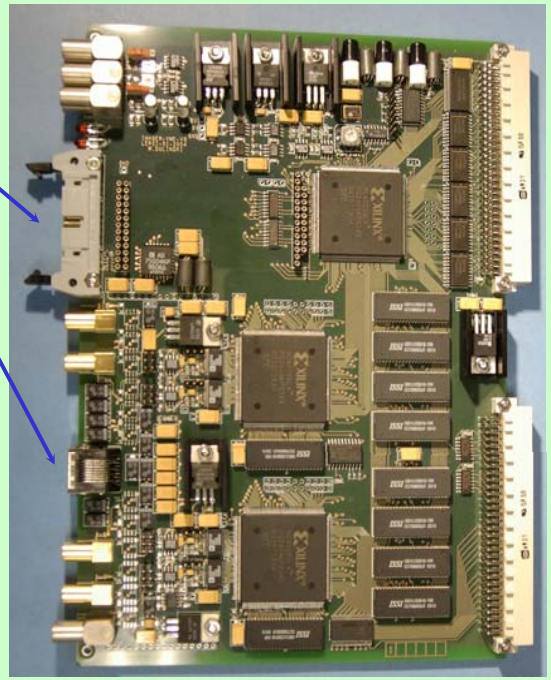
One and Only One DAQ SYSTEM – Common DAQ for ALL Test Benchs

2 Lab Test Bench – 2 Beam Telescope DAQ (IReS + DESY)

MAPS VME DAQ - HW

VME
Sequencer & ADC Board

- **MAPS Ctrl signals**
- **4 Inputs**
- **Up to 256 k pixels / Input**
- **Readout 1-20 Mhz**
- **Dynamic 2000 mV**
- **Resolution 512 µV**
- **Noise 400 µV**
- **Linearity ~ 0,3 %**



Analog

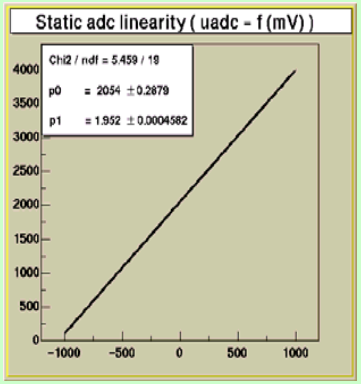
- **Up to 16 ADC 12 bit 20 Mhz**

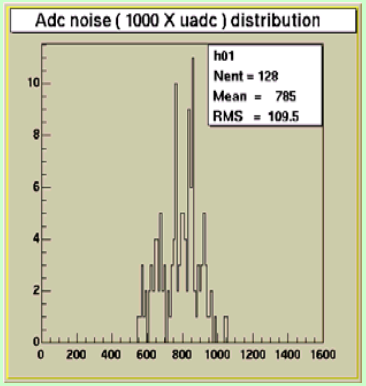
Digital

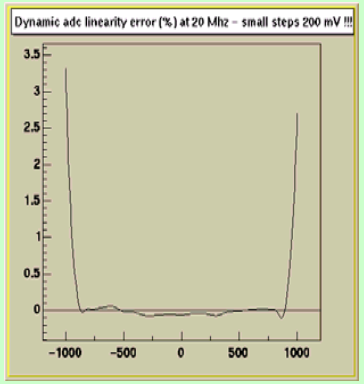
- External **Trigger** handling
- **Pattern** Generator

Daq : PC & VME

- **4 Mo / s VME** bus - Ethernet **6 Mo / s**

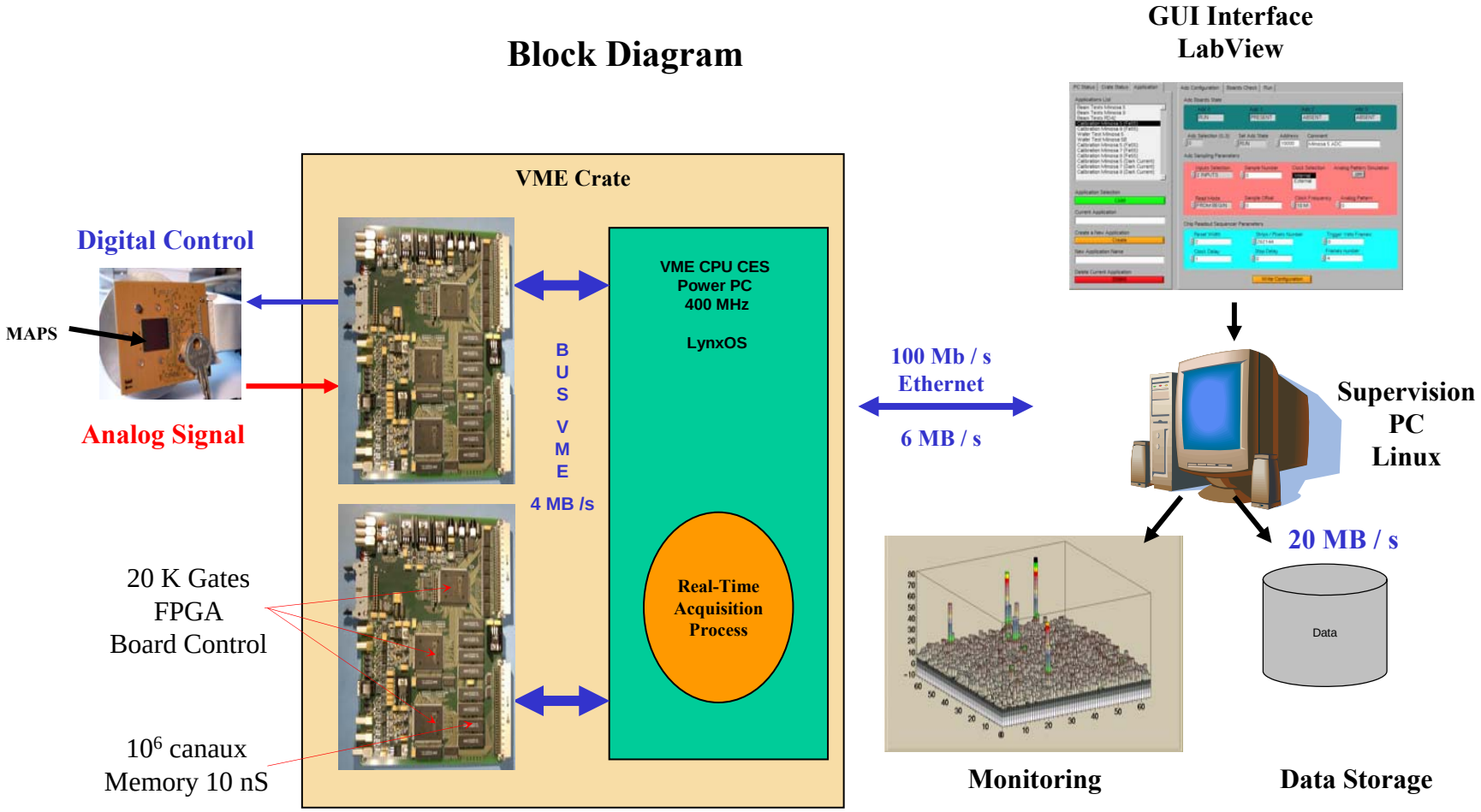






MAPS VME DAQ - SW

Block Diagram



DAQ Architecture : Supervision PC – Acquisition VME

- **Supervision** ▶ **PC – Linux – Monitoring Root**
- **Acquisition** ▶ **RIO2 PPC 400 MHz – LynxOS**
- **MAPS Ctrl & Readout** ▶ **Cartes Séquenceur & ADC VME**

MAPS USB 2.0 DAQ SYSTEM

Why a New DAQ ?

- **Very Low Data Bandwidth 4 MB/s**
- **MAPS Digital outputs – No way**
- **Readout frequency Max 20 Mhz**
- **On Board Data Sparcification – No way**
- **More generic sequencer (MAPS Digital Ctrl)**
- **Software … Linux … Windows …**

Status ?

- **Board Ready**
- **Lab MAPS test bench operationnal (Summer 2005)**
- **Final IReS USB DAQ Software for Summer 2006**
  - **Multiple boards … USB bandwidth …**
  - **Dynamic Variable Size event data format**
  - **Windows ROOT monitoring**
- **Generic sequencer for end of Summer 2006**

DAQ USB 2.0

Analog

- 1-4 ADC 12 bits – 40 Mhz
- 1 ADC 14 bits – 100 MHz
- 10^6 pixels **shared** 1-4 Inputs

Digital

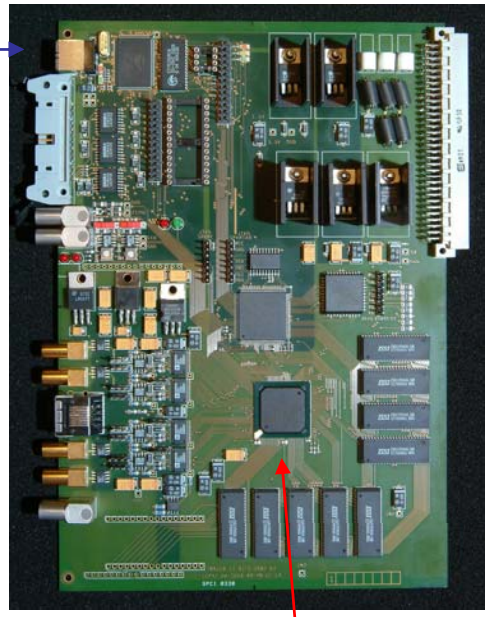
- **Pattern** generator **& Trigger**
- 16 **Digital inputs**

Daq

- Transfer **15 MB/ s USB 2.0**

Firmware (To Be Done)

- CDS Calculation (Done)
- Pedestal substraction
- Data sparcification



USB 2.0 BUS

Virtex 2 FPGA

Supervision PC Windows

Conclusion

Results

- We built a MAPS DAQ System
- Fullfilled our Test and Characterization Requests for last 5 years
- New System – Based on USB – overcome all limitations

But …

- We are NOT DAQ Experts
- We don’t plan to provide EUDET Generic DAQ

What we can do ?

- We can / need provide « Local » DAQ for « EUDET MAPS » Characterization …in Demonstrator
- It can be better to have two DAQ : Final EUDET DAQ & « MAPS Characterization DAQ »
  - Because we can’t wait on final DAQ for MAPS characterization