CMOS-ILC Research Team of IReS

M. Winter

General Features

- National funding agency: CNRS - IN2P3
- Academic host institution: Univ. Louis Pasteur (Strasbourg)
- In ILC since 1998 (TESLA project)
- Develops CMOS sensors for charged tracking since 1999 ($\sim$ 20 pub. in NIM, IEEE-TNS)

Team Composition & Activities

▶ Team Composition:

- ◇ **Micro-circuit designers:** C.Colledani, A.Dorokhov (Post-doc), W.Dulinski, F.Guilloux, S.Heini (Doc.), A.Himmi, Ch.Hu, M.Szelezniak (Doc.), I.Valin
- ◇ **Test system engineers:** G.Claus, M.Goffe, K.Jaaskelainen, M.Pellicioli
- ◇ **Physicists:** J.Baudot, A.Besson, M.Deveaux (Doc.), D.Grandjean (Doc.), A.Shabetaï (Doc.), M.Winter

▶ Activities:

- ◇ **Development of CMOS sensors for:**
  - ○ vertex detectors : STAR-upgrade (RHIC), CBM (GSI), ILC
  - ○ imaging devices: HPD, electronic microscopes, fluorescence microscopes, etc.
- ◇ **Studies of vertex detector geometries:**
  - ○ for ILC ○ for CBM
- ◇ **Physics studies for ILC:**
  - ○ Higgs-top coupling ○ HHH coupling

Expertise and R&D Directions

- **Exploration of manufacturing processes:**
  - ∴ AMS: 0.6μm , 0.35 μm HIGH-RES, 0.35 μm OPTO ,
  - ∴ AMI (former MIETEC): 0.35 μm, ∴ IBM: 0.25 μm, ∴ TSMC: 0.25 μm
- **Design of pixel architectures:**
  - ∴ charge collection systems ∴ CDS with preAMP (in coll. with DAPNIA),
  - ∴ radiation tolerance (vs T) ∴ multi-memory pixels
- **Design of chip (read-out) architectures:**
  - ∴ fast column parallel read-out with integ. ADC & sparsification (in coll. with DAPNIA, LPSC, LPCC),
  - ∴ decoupled integration and read-out architecture,
  - ∴ STAR specific architecture ∴ imaging specific designs
- **Activities related to material budget:**
  - ∴ industrial thinning procedure (wafers, chips)$\mapsto$ yield, etc.
  - ∴ handling of thinned sensors (e.g. bonding)
- **Activities related to radiation tolerance:**
  - ∴ irradiations: 1 MeV neutrons (coll. with Dubna), 10 keV X-Rays, ^{60}Co gammas, 10 MeV e^- (coll. with HH)
  - ∴ R&D on radiation tolerant sensors

- 4 test benches for MIMOSA chips (VME $\mapsto$ USB-2)
  - $\hookrightarrow$ characterisation & calibration of chips (with self made DAS)
- Microstrip telescope (4 pairs of planes $\mapsto$ x,y with $\sim$ 1 μm accuracy in mid-plane)
  - $\hookrightarrow$ characterisation of chips on test beams ($\mapsto$ cluster charge -$>$ epitaxial thickness, ϵ_{det}, σ_{sp})
- Micro-bonding service
- Probe stations

Contributions to EUDET

- **CMOS sensors (4 planes) for demonstrator and final set-up:**
  - **full design (in coll. with DAPNIA, LPSC-Grenoble, LPCC-Clermont)**
  - **full characterisation and performance assessment**

- **CMOS sensor local DAS boards:**
  - **provide boards for demonstrator**
  - **participate to final DAS concept**

- **Participate to overall concept, based on expertise on beam (Si-strip) telescope (W.Dulinski)**