# General Electronics Planning

## FE ASIC

Define electronics system for TP,
Formation of design teams.

ASIC design starts

FE ASIC design team
Approx. 8 man years
of design time
needed.

Submission of FE AISC (VFAT3/GdSP)

## Readout systems

2011 Short Term :

VFAT2 , Turbo hardware and Labview DAQ software

2012

We are here.

Medium Term :

VFAT2 + SRS

Off Detector
uTCA development

2014

Long Term :

2015

Full and final system
On & Off detector electronics.
VFAT3/GdSP + GBT + uTCA system

# Analog Building Blocks

| Module | Task | Status (% done) | Notes | Institute |
|---|---|---|---|---|
| Front End Preamp, Shaper, [Comparator VFAT3] | Specification<br>Schematic & Simulation<br>Layout<br>Post Layout simulation<br>Prototype<br>Varilog AMS model | 70%<br>70%<br>0<br>0<br>0<br>0 | Done : Preamplifier & Shaper, Programmable gain, shaping time, very low power.<br><br>To add : Dynamic range verification, leakage I comp., power pulsing technique | CEA Saclay |
| CBM | Specification<br>Schematic & Simulation<br>Layout<br>Post Layout simulation<br>Varilog AMS model | 80%<br>50%<br>30%<br>0<br>0 | Done : DAC schematic, layout, first sch. Simulations of cal. Pulse (I&V) injection.<br><br>To add :Optimise layout size, Bandgap, ADC, temperature monitoring | INFN- Bari |
| SAR ADC | Specification<br>Schematic & Simulation<br>Layout<br>Post Layout simulation<br>Prototype<br>Varilog AMS model | 70%<br>-<br>-<br>-<br>-<br>0 | Industrial publications get better each year.<br><br>AGH submitted prototype with very similar spec.s<br><br>To do: Adapt AGH prototype to fit layout or buy IP | AGH or bought IP |

In general, the analog blocks are progressing well .

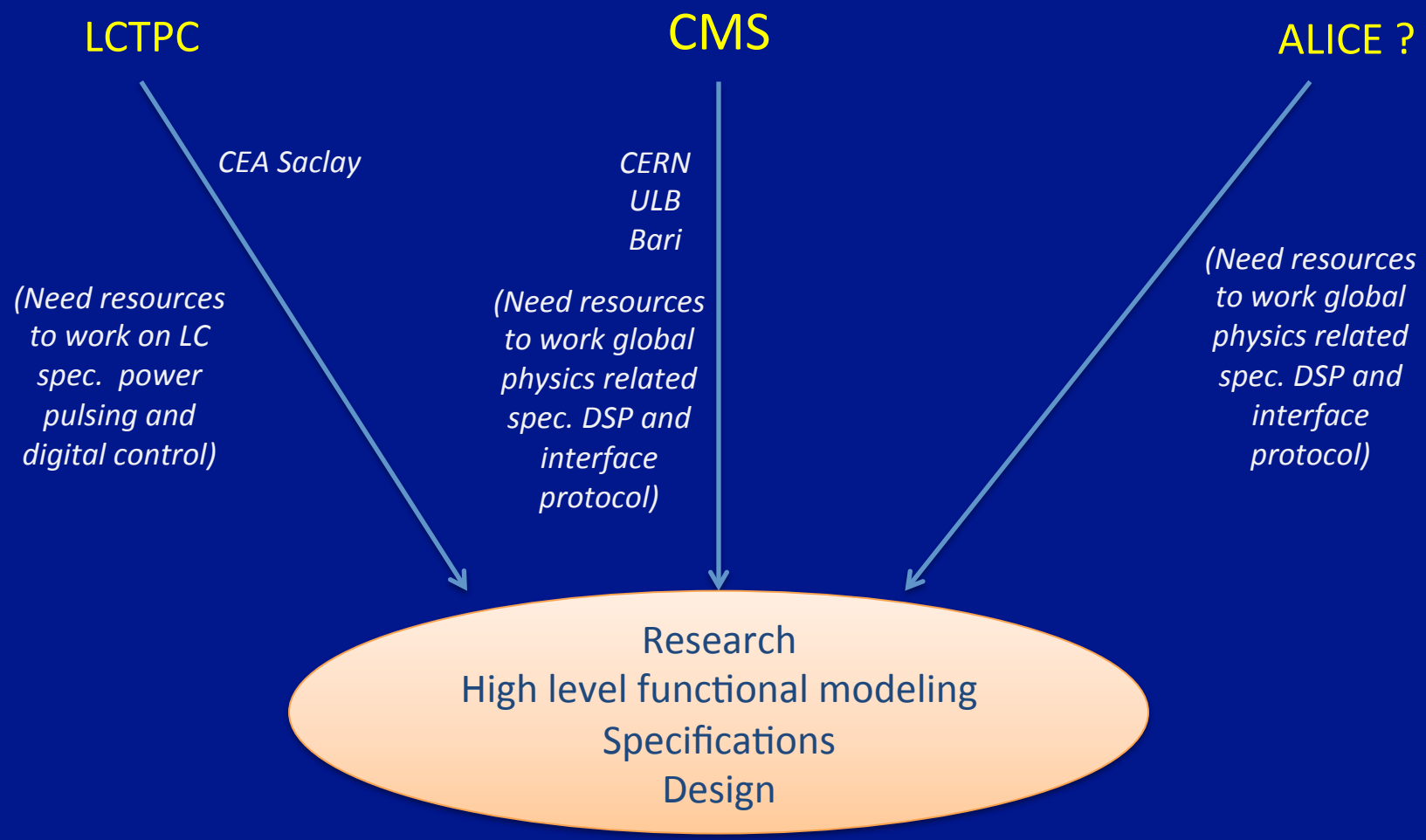
# Digital Building Blocks

| Module | Task | Status (% done) | Notes | Institute |
|---|---|---|---|---|
| DSP | Research<br>Specification<br>High level sim<br>Verilog code & sim.<br>Gate level RTL and verification | 20%<br>-<br>20%<br>- | So far : Starting blocks from SALTRO<br>First investigation in common mode sub.<br>To do : Common mode, BC1 in continuous mode, TOT R&D, specification for centre of gravity | ULB (simulation)<br>Spec.s : + CERN<br>Verilog code : ?<br>Verification : ? |
| Interface Protocol: (Slow Cont. TTC, Data Stream, Sync) | Research<br>Specification<br>High Level sim<br>Verilog code & sim.<br>Gate level RTL and verification | 10% | Largely at the Research before specification stage. | INFN-Bari<br>? |
| SRAM | Specification<br>Veriilog<br>Gate level RTL<br>Verification | - | 64x128 (also 64x256) SRAM prototype being submitted in May 2012. | CERN |
| Control Logic | Specification<br>Verilog<br>Gate level RTL<br>Verification | - | | ? |

There is a need for extra participation in the digital design.
From definition of specification, high level description and simulation to gate level RTL and verification.

# Expanding to other applications

Motivation : Shared cost and additional manpower resources



# Meetings and communication

| | |
|---|---|
| Online meetings | Regular online meetings for 10 minutes review on each sub module.<br>Bi-weekly (Thursday mornings) ? |
| Physical meetings | 2 Days, 3 month intervals ?<br>At CERN. |