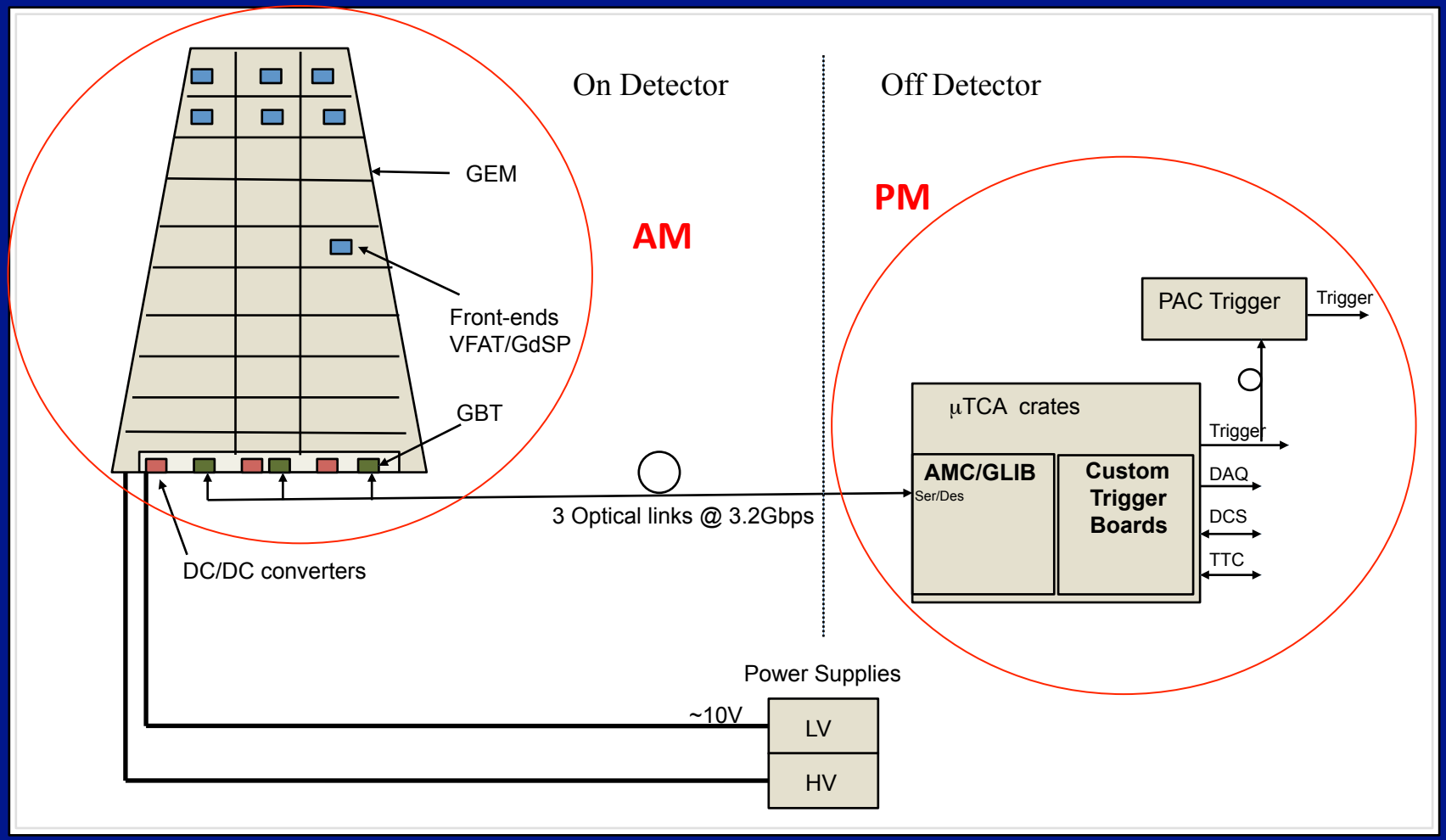
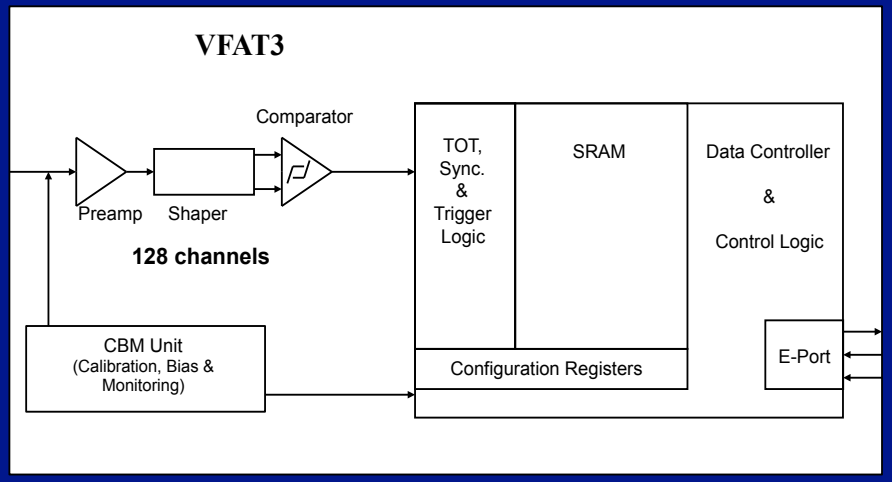
GEMs for CMS Workshop

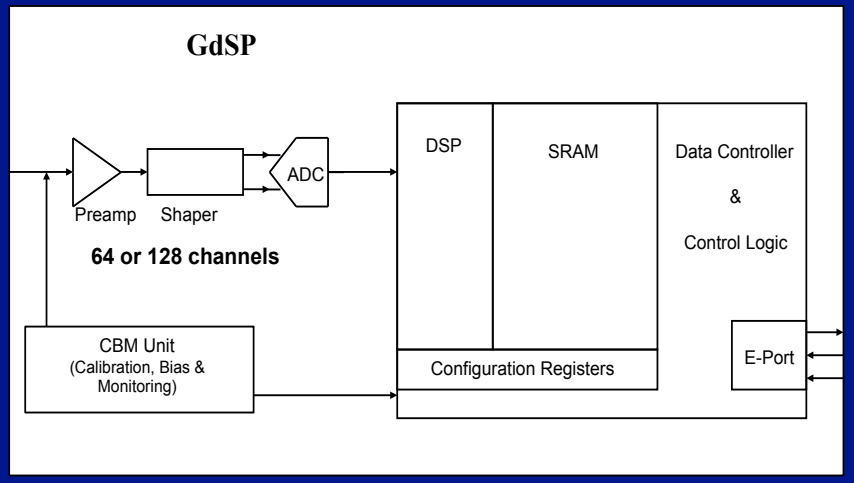


Front-end Microelectronics Design
VFAT3/GdSP ASIC design

2 Trigger & Tracking Front-end architectures considered.



OR



VFAT3 :

Front-end with programmable shaping time.

Internal calibration.

Binary memory

Interface directly to GBT @ 320Mbps.

Designed for high rate (10kHz/cm^2 depending on segmentation)

Approx. 8-10 man years of design work expected .

GdSP :

Similar to VFAT3 except has an ADC / channel instead of a comparator.

Internal DSP allows subtraction of background artifacts enabling a clean signal discrimination.

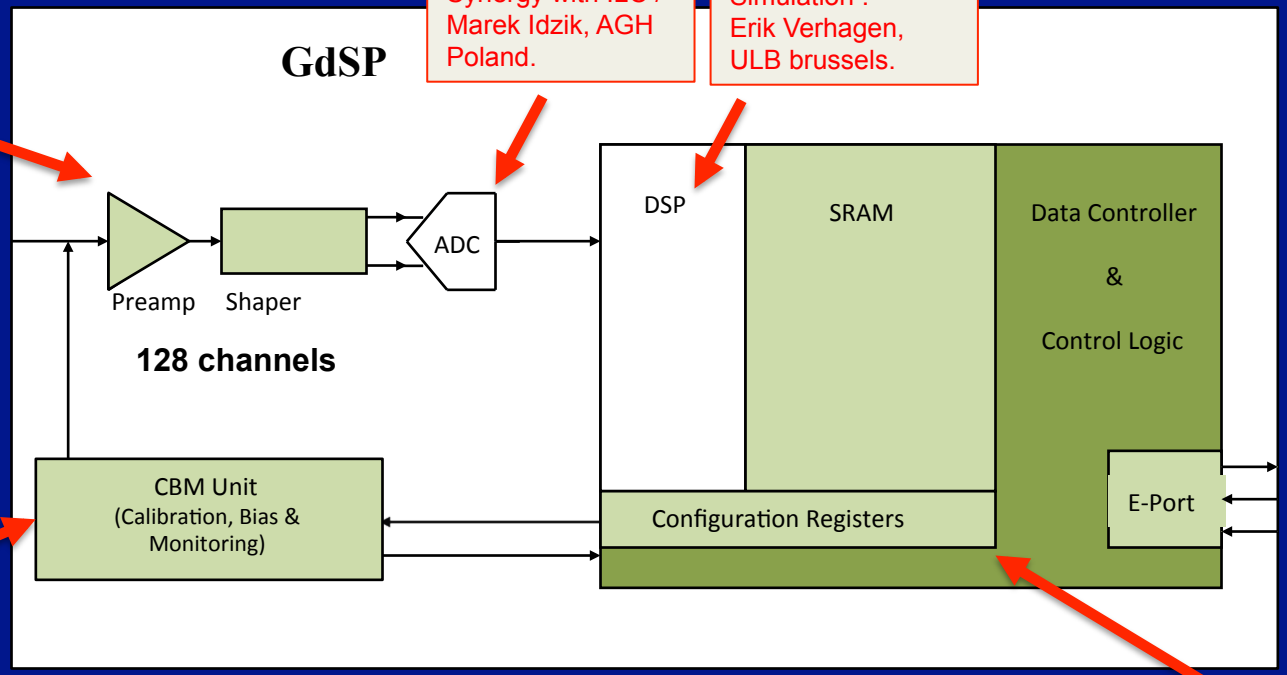
Centre of gravity a possibility to achieve a finer pitch resolution (if needed).

Microelectronics design

Fabrice Guilloux
CEA Saclay

Synergy with ILC / Marek Idzik, AGH Poland.

Simulation : Erik Verhagen, ULB brussels.



Flavio Loddo,
INFN - Bari

Slow Control design,
Giuseppe De Robertis
INFN - Bari

Common elements between VFAT3 and GdSP

Common block but individual modes for VFAT3 and GdSP

2011 : Define global architecture and design team (approx. 8-10 man years needed).
2012 : Initial focus on VFAT3/GdSP elements needed for architecture choice and common architecture building blocks.
Aim to complete design by 2015.
Design team not yet complete .

Coordination :
Paul Aspell, CERN