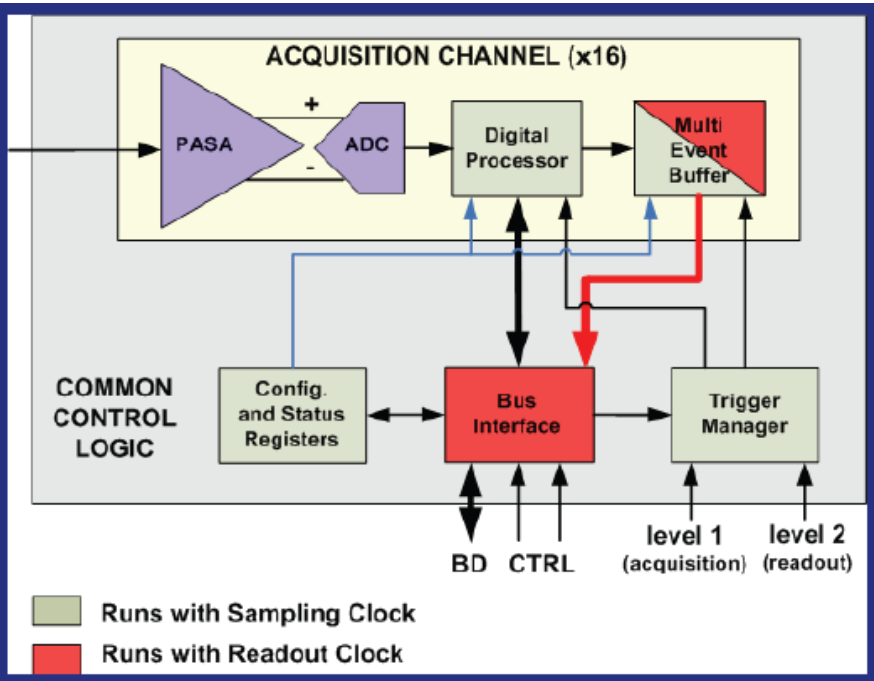
Irfu - CEA Saclay
Institut de recherche sur les lois fondamentales de l'Univers

GdSP ASIC
Front end design

CMS GEM Upgrade Workshop III
CERN, Thursday, April 19, 2012

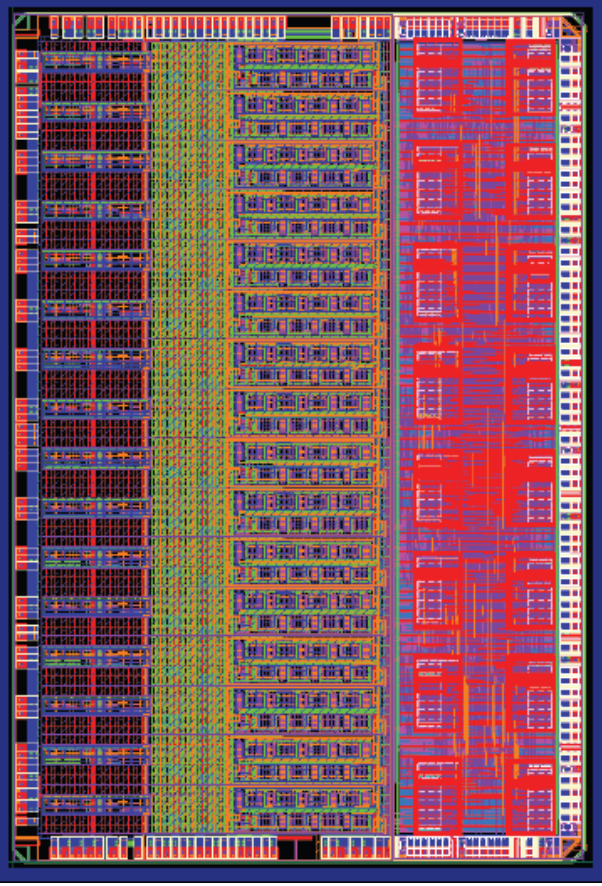
Fabrice Guilloux on behalf CEA/IRFU group

SALTRO16



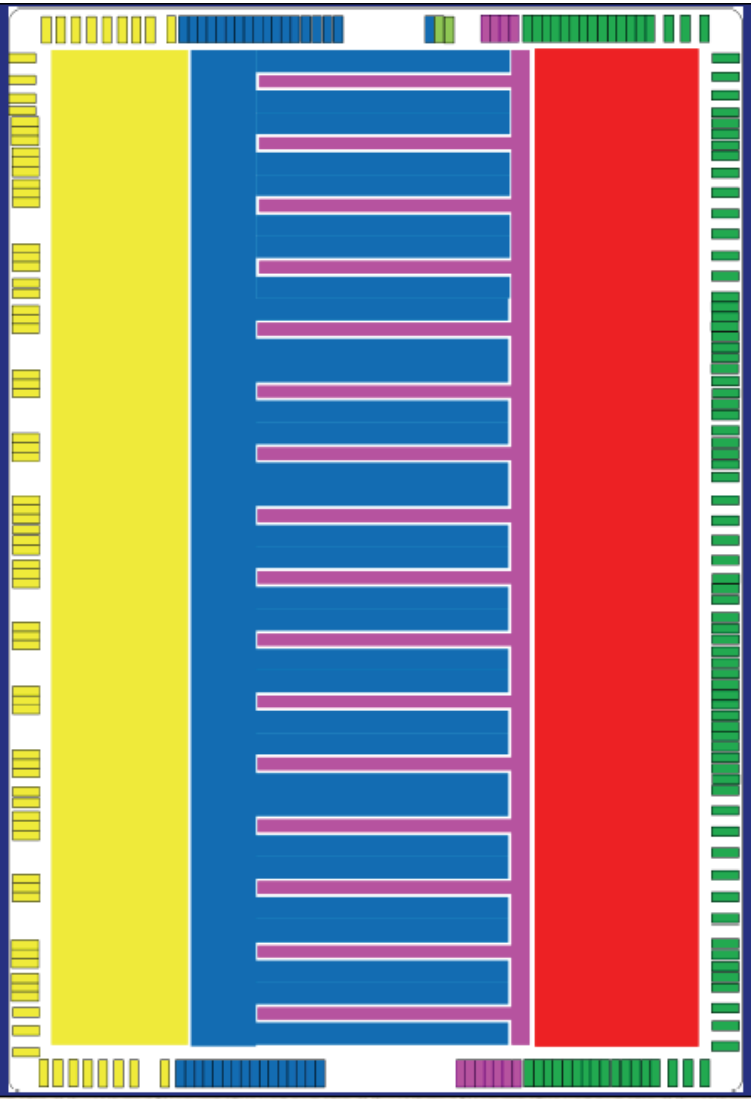
Designed in 2009-2010
Beautiful success.
First chip integrating low noise FE, ADC & DSP

Technology :
IBM 130nm
CMOS



Luciano Musa ..... S-Altro Specs. & Architecture
Paul Aspell ..... Coordinator of design
Designers :
Massimiliano De Gaspari ..... Front-end + ADC
Hugo França-Santos ..... ADC core
Eduardo Garcia ..... Data Processing & Control

SALTRO16: Power consumption



Power domains:

PASA analog

ADC analog

ADC digital

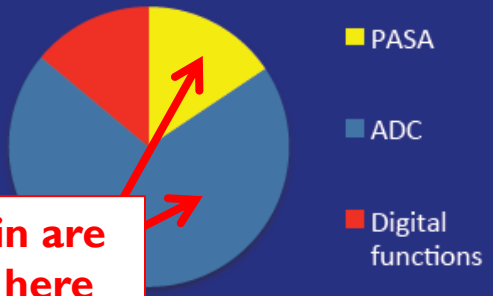
Digital core

Digital Pads

PASA ~8mW/ch,
ADC 36mW/ch @40MHz
Digital functions ~114mW
Total power ~ 750mW

Succesful power pulsing operation

Power Distribution for 16 channels



Large gain are possible here

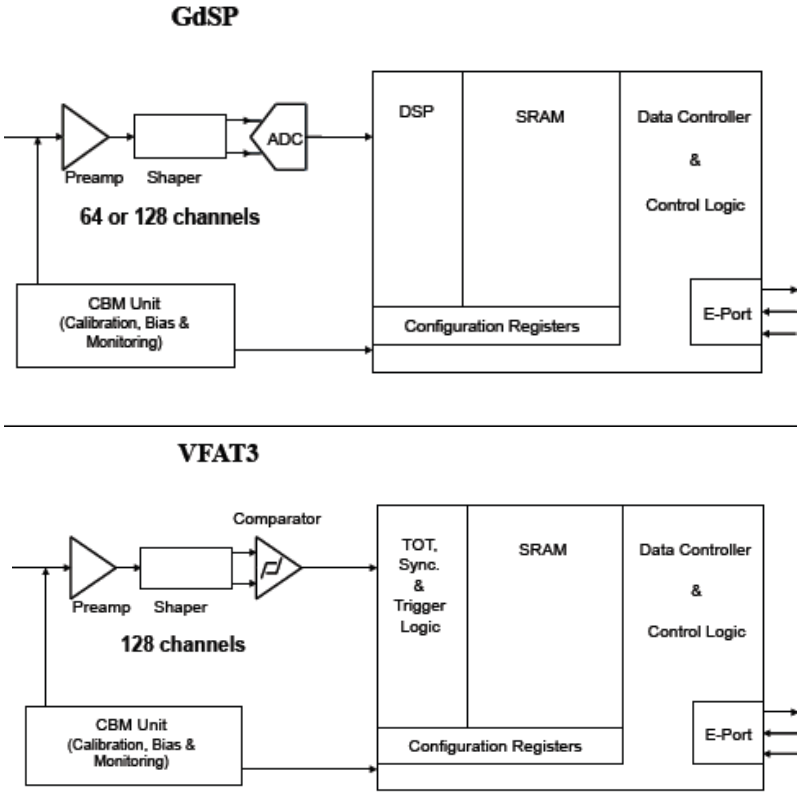
It is clear that the ADC power consumption limits the design to small channels counts.

But times are changing.

GdSP ASIC

- Join effort to have one ASIC for 2 projects. Or at least large common parts.
  - LCTPC (AIDA)
    - specifications derived from SALTRO16 *(slower, low cap)*
  - Muon CMS upgrade :
    - First option : VFAT3 ASIC = PSD chip
    - Second option : GdSP ASIC
    - Specifications derived from previous VFAT2 *(faster, high cap)*

Common front end

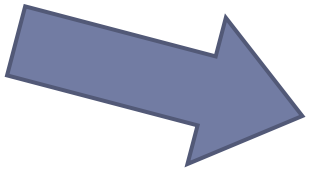


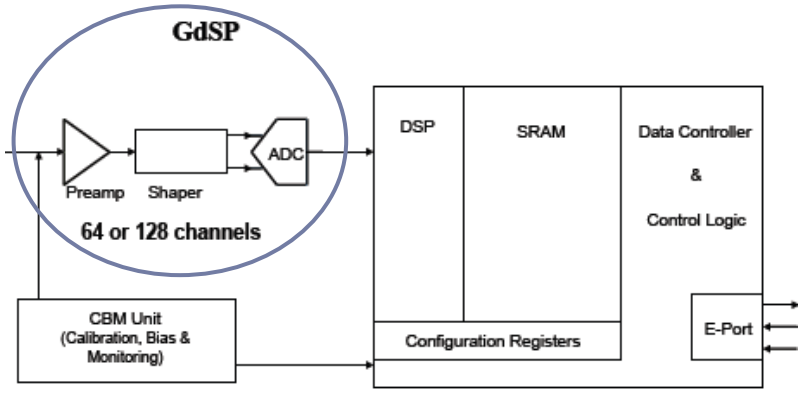
- The technology issue:
  - Long term project (> 2014-2015)
  - Uncertainties on the future of IBM 130nm ?
  - Cern is moving to TSMC technology for 65nm technology.

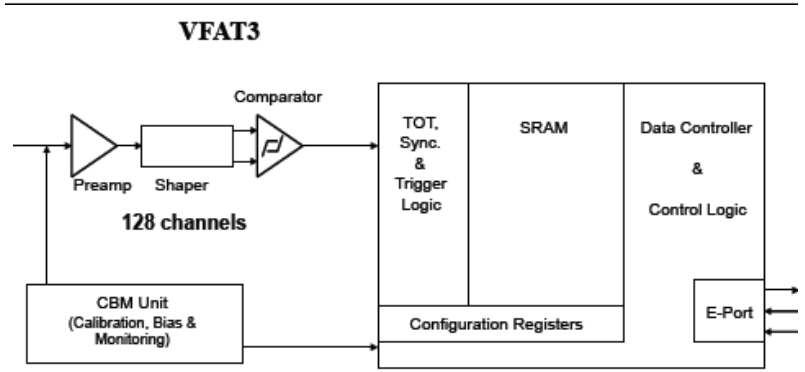
- Development ~ frozen during few months (simulations only):
- Decision now taken to go on with IBM 130nm.

GdSP ASIC

- Focus on front end







GdSP Front End specifications

- Technology :
  - CMOS 130nm ; Power supply 1.2V

From Paul Aspell

Parameter	VFAT2	SALTRO	VFAT3 / GdSP
Polarity	dual	dual	dual
Shaper peaking times (ns)	22	Programmable : 30, 60, 90, 120	Programmable : 25, 50, 100, 200, 400 ?, 600 ?
Gain (mV/fC)	60	Programmable : 12, 15, 19 & 27	Programmable: Values TBD

- Shaping times :
  - 25 ns ➔ Silicon Strip Detector (demanding for power)
  - 100 ns ➔ Gazeous Detector (optimum from our knowledge)
  - 500 ns ➔ Micromegas Detector with resistive layer (may be not necessary now)
    - Idea to reduce the set of shaping times by applying latter a digital filter to obtain longer shaping

- (Shaper + Gain) programmable through slow control

GdSP Front End specifications

From Paul Aspell

Parameter	VFAT2 (IBM 0.25)	SALTRO (IBM 0.13)	VFAT3 / GdSP (IBM 0.13)
Linear range	+- 12fC	150fC	100fC, TBD
Input capacitance (pF)	20	0-20	15 – 20 – 30 – 60
Noise	~500e + 40-60e/pF @ 25ns	See previous talk	< SAltro /VFAT

Starting from data measured on ABCN (130nm design by Jan Kaplon for ATLAS SCT):

** 800 e- @ 5pF, tp=22ns, 100µW*

** assuming serie noise only + strong inversion for the input transistor*

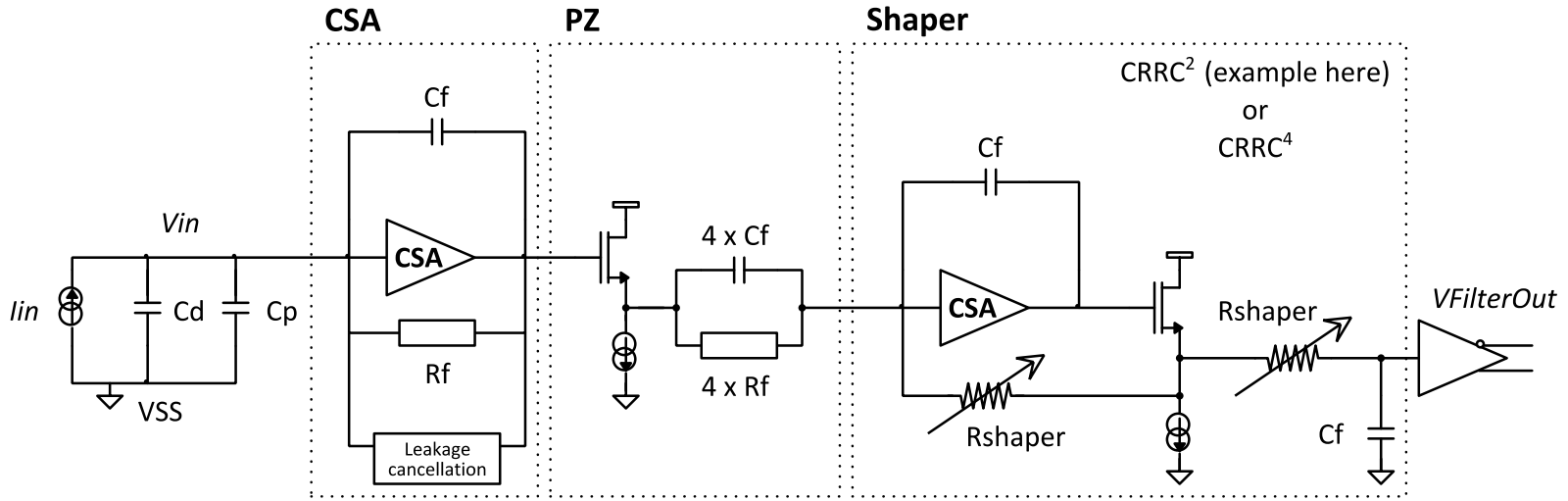
➔ ***we can hope 530 e- @10pF, tp= 100ns, 200µW***

➔ ***Ultra Low power low noise design seems feasible***

Parameter	VFAT2	SALTRO	VFAT3 / GdSP	This FE study
Power (mW/channel)	1.5 (IBM 250nm) (incl. comparator)	8	<< 1	< 0.24 (CSA only)

GdSP Front End : pre-amp study

- Simulations : pre-amp + biasing + shaper (still to be optimized)
- Pre-amp in CSA configuration (transimpedance should be optimized for a single Cin)
- Global Architecture not frozen yet
  - Two types of low frequency feedback + PZ cancellation schemes tested:
    - Current conveyor
    - MOS transistors

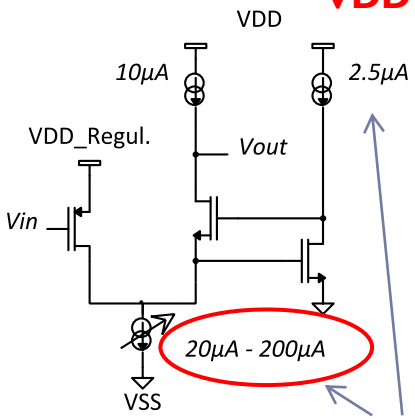


GdSP Front End : pre-amp study

- CSA Structure
  - Low gain from intrinsic transistor parameters
    - (1) Simple common source : G ~ 30dB
    - (2) Common source + cascode for the input : G ~ 39dB
    - (3) Common source + cascode for the input + cascode for the load : G ~ 47dB
    - (4) Common source + regulated cascode for the input + cascode for the load : G ~ 73dB
    - (5) Common source + regulated cascode for the input + regulated cascode for the load : G ~ 86dB
      (5) ➔ As in Jan Kaplon design

  - Chosen architecture : regulated folded cascode
    - Flexible architecture
    - Input transistor : weak inversion
    - Gain – bandwidth – noise – power consumption tradeoff.

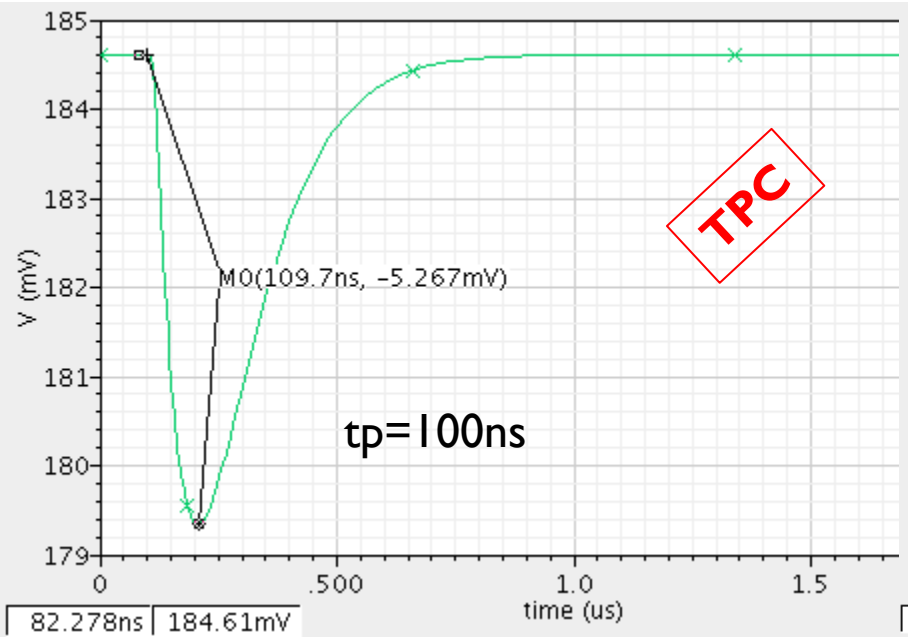
VDD =1.2V

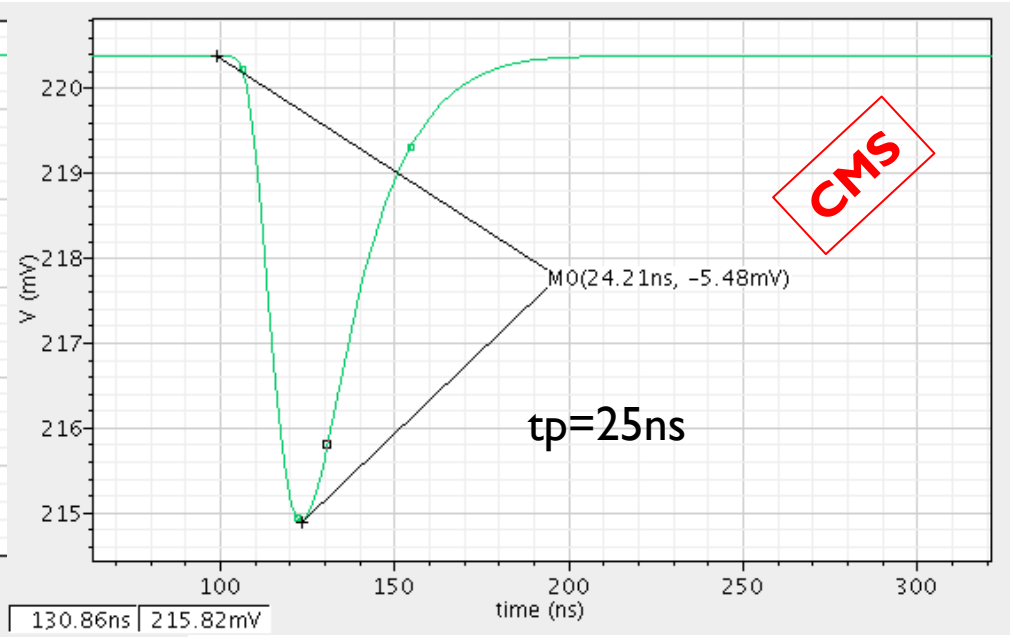


To multiply by 1.2 to obtain the CSA power consumption

GdSP Front End : pre-amp study

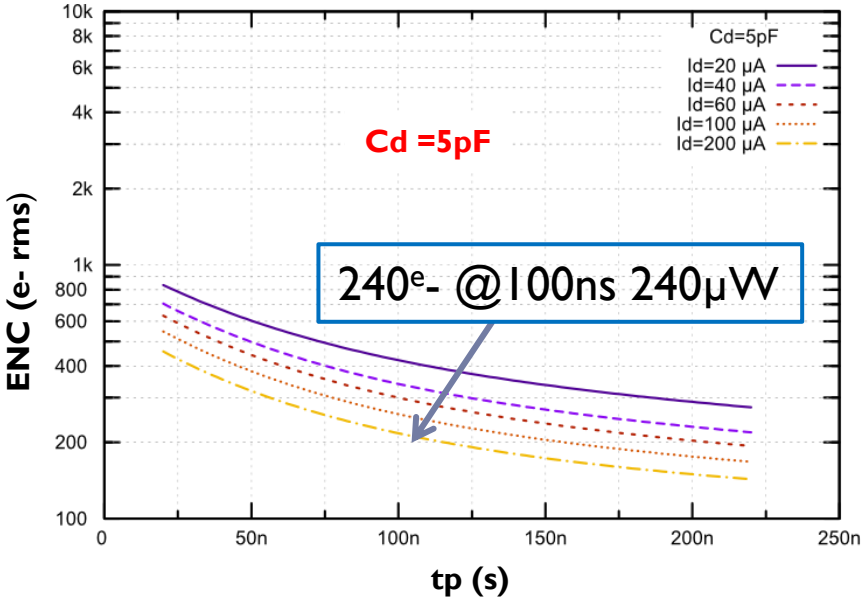
- Simulations : preamp+ biasing + shaper
  - Cd = 30pF
  - Cf = 200fF ; Rf ~50MΩ
  - Tp = 100ns
  - **Iin = 70µA => 90 µW**
  - Cd = 30pF
  - Cf = 200fF ; Rf ~50MΩ
  - Tp = 25ns
  - **Iin = 200µA => 240µW**

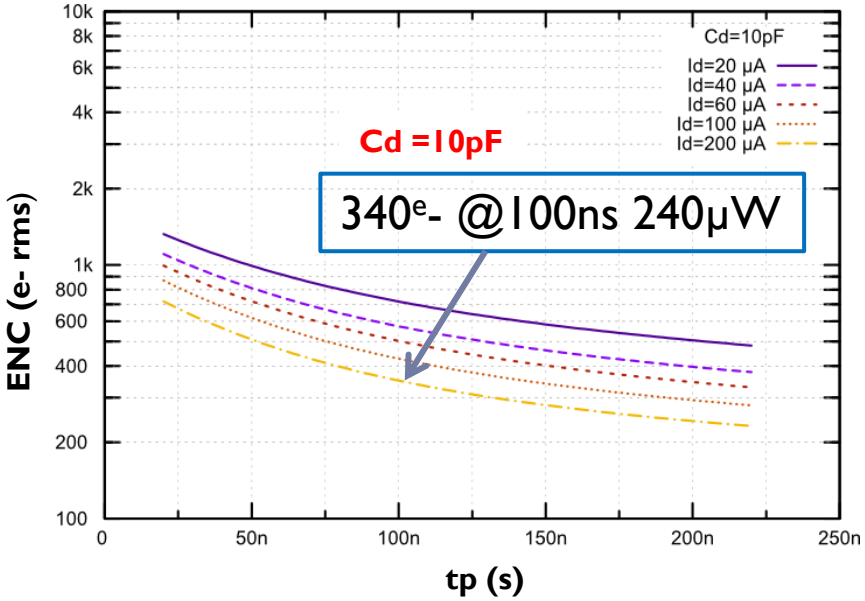


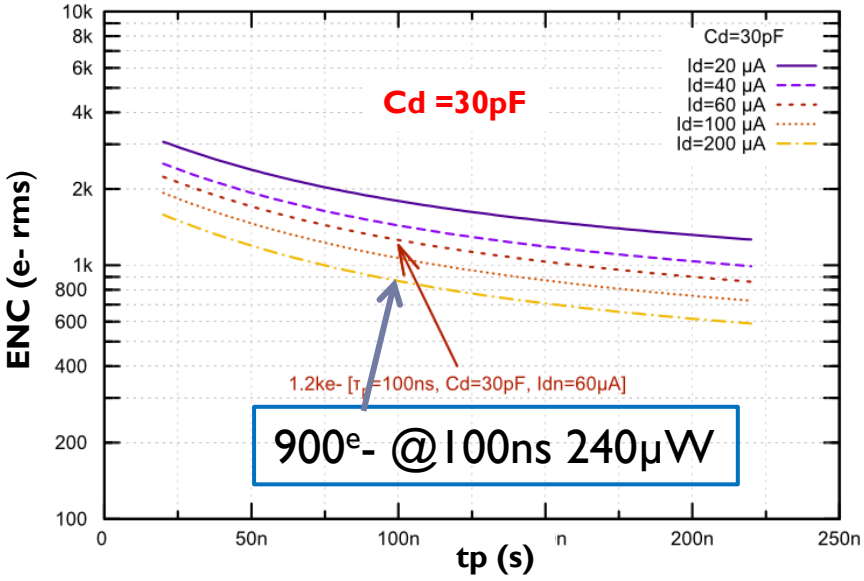


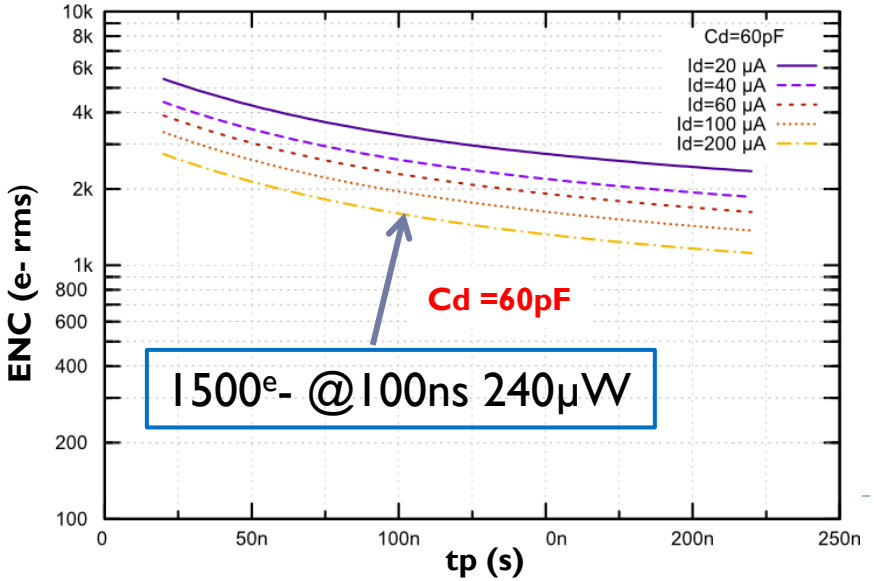
- ENC ~ 1330 e-
- ENC ~ 2100 e-

GdSP pre-amp study (pre-amp + ideal shaper)



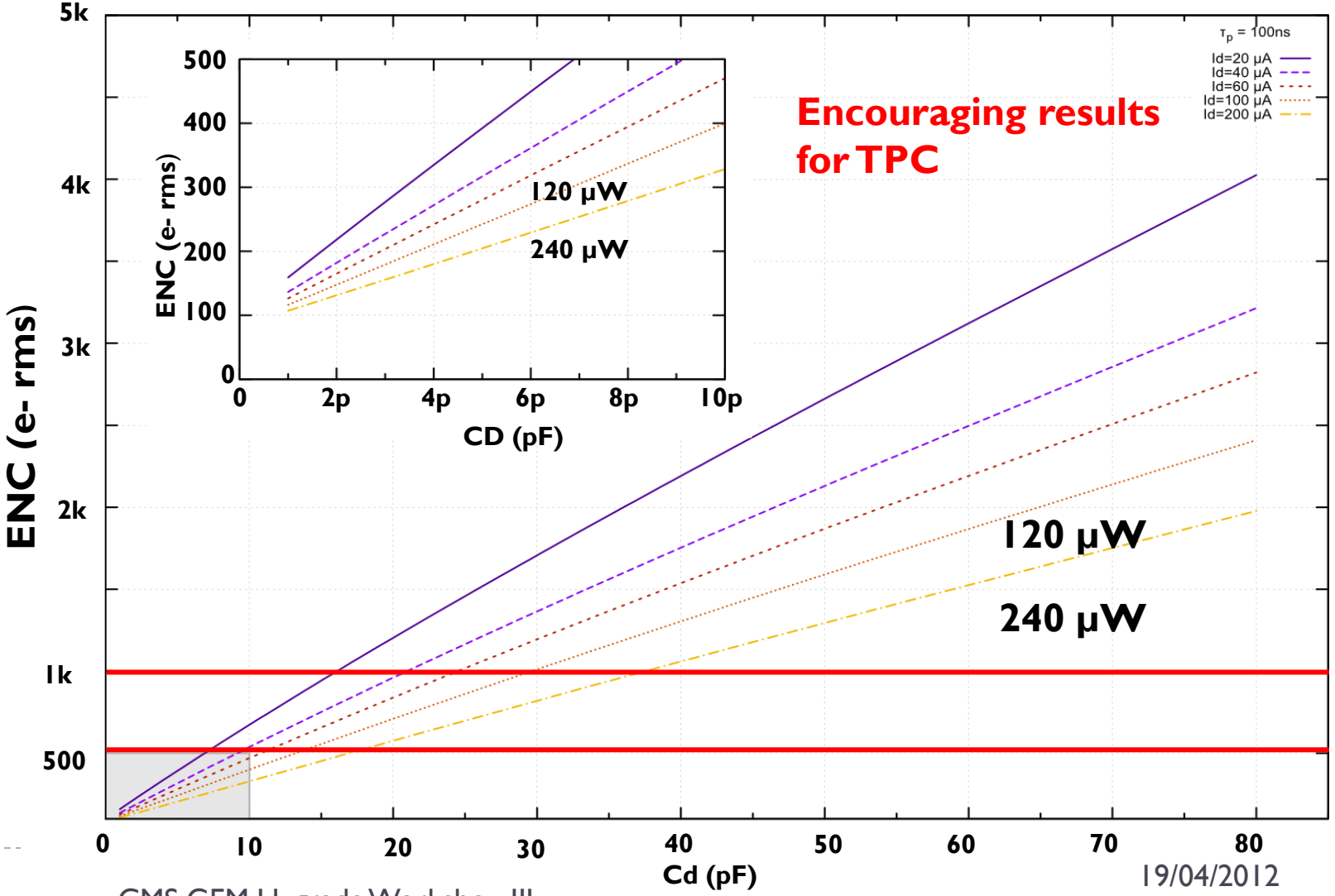






GdSP pre-amp study (pre-amp + ideal shaper)

- Simulation of pre-amp, ideal shaper (**tp=100ns**).

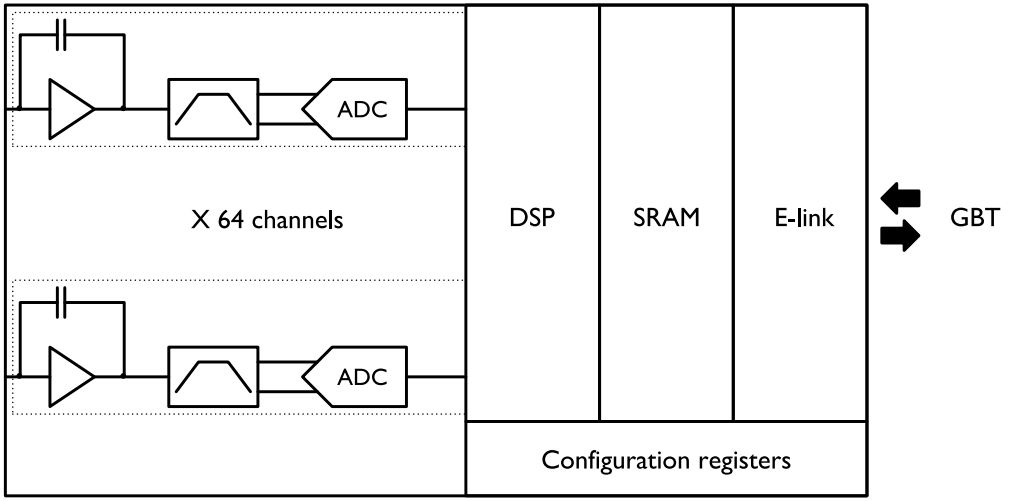


Conclusions

- A GDSP design common for CMS and LCTPC is seriously considered.
- A low noise front-end part seems to be feasible with a power significantly lower than in PASA/SALTRO
  - Pre-amp : Folded cascode most flexible solution
  - PZ + shaper still studied
    - MOS resistor feedback promising
    - Linearity still to be studied
    - Impact from leakage current
- After the long simulation phase, the next step is to go to a prototype (front end only)

Backup : GdSP ASIC

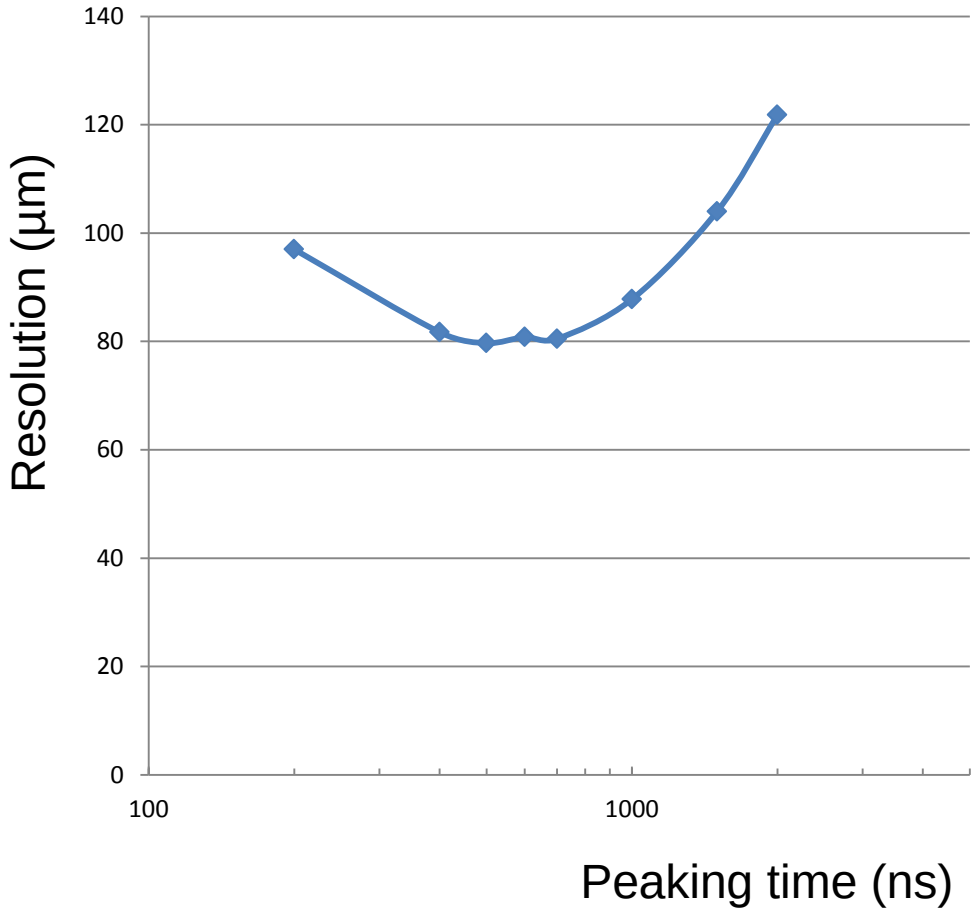
- Readout circuit for TPC
- Architecture based on Saltro16 ASIC
  - Pre-amp / Shaper front end
  - Analogue to Digital Converter
  - Digital Signal Processing
  - Static Random Access Memory
  - *New interface :* GBT E-link developed by CERN



- Design optimization
  - Keep main specifications of SALTRO16 + extend capability on fast signal (from VFAT2)
  - Low power consumption driven design !

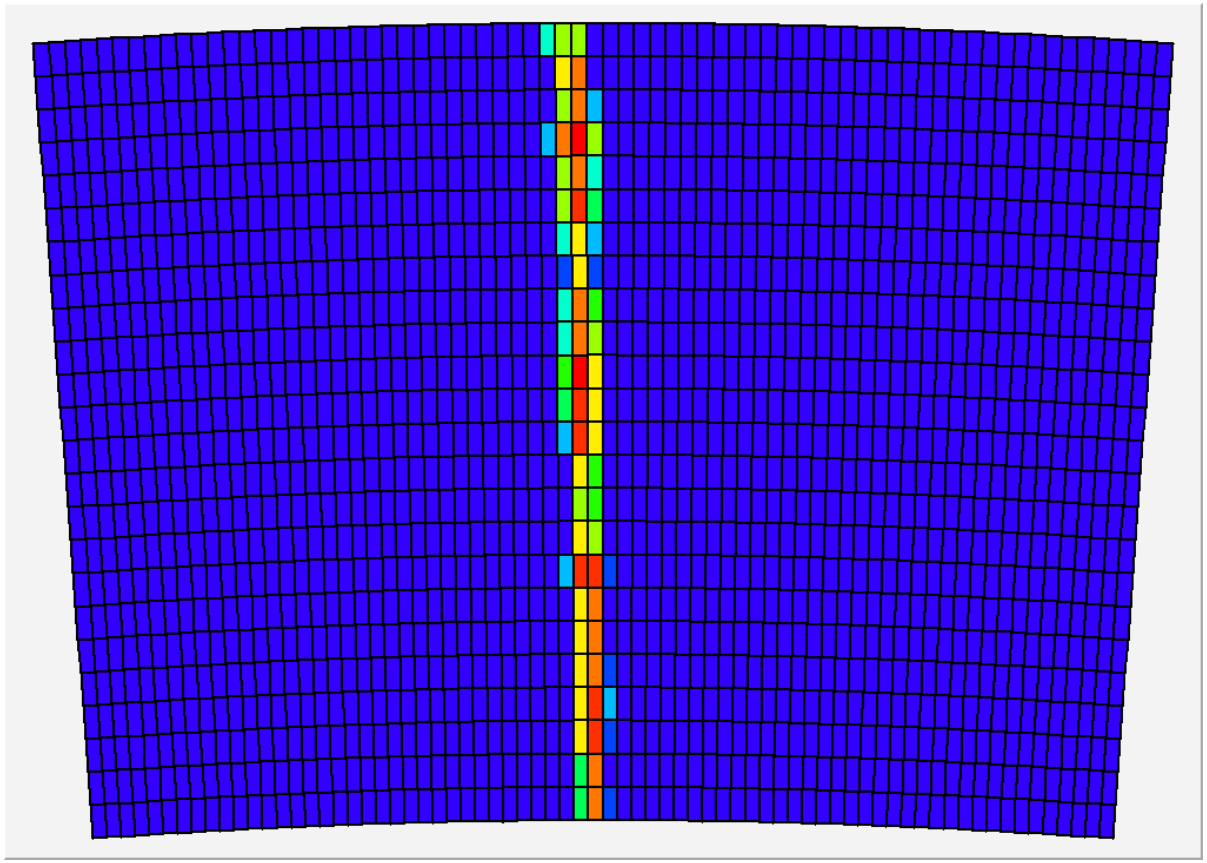
Backup : From SALTRO16 to GdSP

- Larger number of channels (16 => 64) ➔ more compact
- Lower power consumption:
  - ADC
  - Front-end
- Larger versatility, programmability (gain, shaping, range of Cin)
- Optimization of DSP + new readout
- But large design effort required (~10 man.y) and (S)ALTRO team is no more available:
  - Common design for CMS muon upgrade and for LCTPC.
  - International design team led by P.Aspell (CERN).



Backup :
Space resolution of Micromegas with resistive layer in function of the peaking time

The optimum is found for a peaking time around 600 ns.



Backup : Track in a TPC

The spatial resolution is manly given by the adjacent PADs.

For a Micromegas operating at low gain (~1000):

- The main PAD collects about 3.2 fC
- Setting a limit at 1/10 of the main PAD, the minimum charge required to be detected is 0.32 fC ➔ 2000 e-
- Noise limit ?