VFAT3 Slow Control Architecture

A proposal for the VFAT3 slow control section

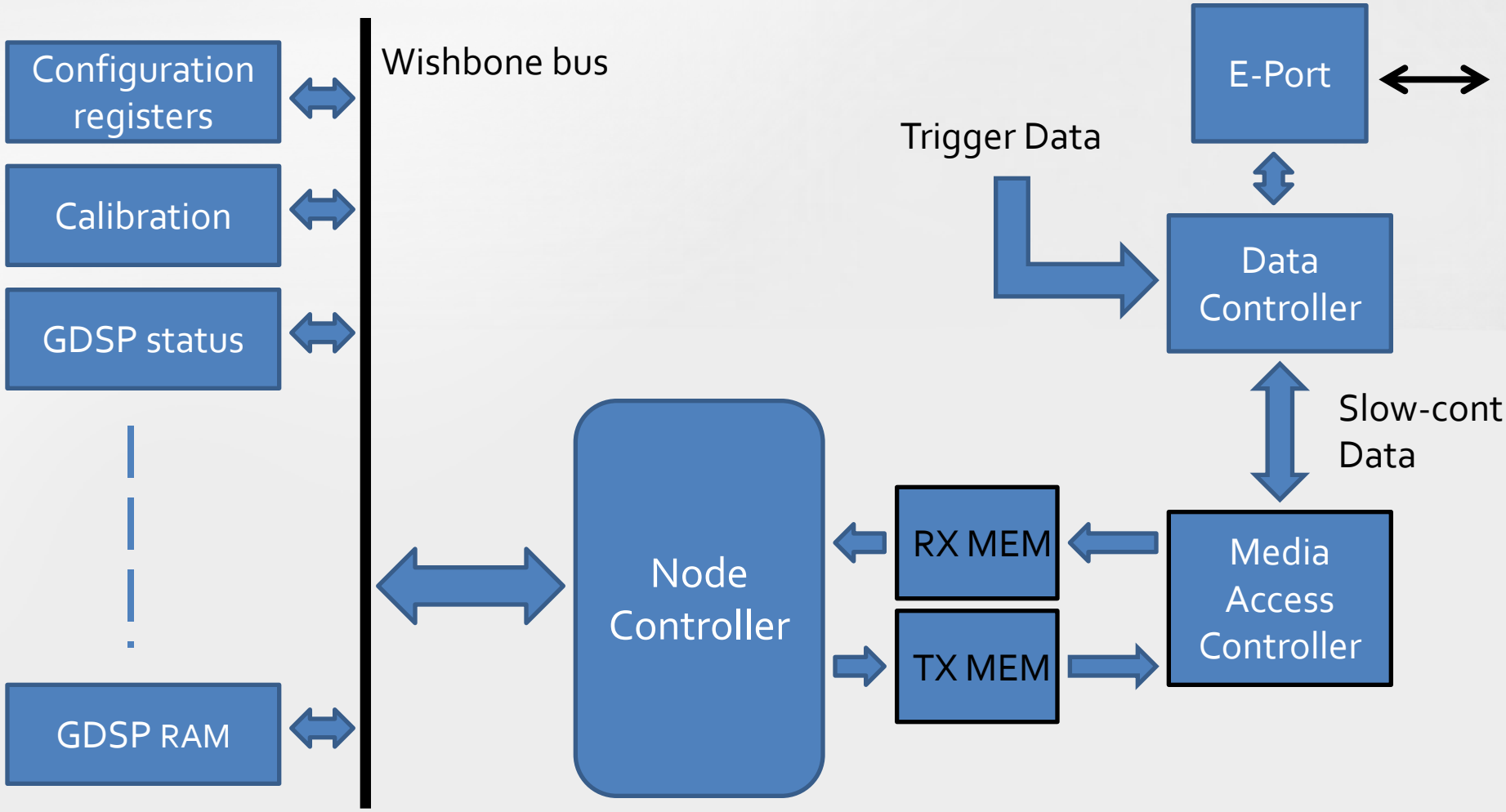
General requirements

- All configuration and status registers should be organized in 8 bits registers with 16 bits address
- Registers should be read/write using the Wishbone bus protocol

Wishbone Bus Features

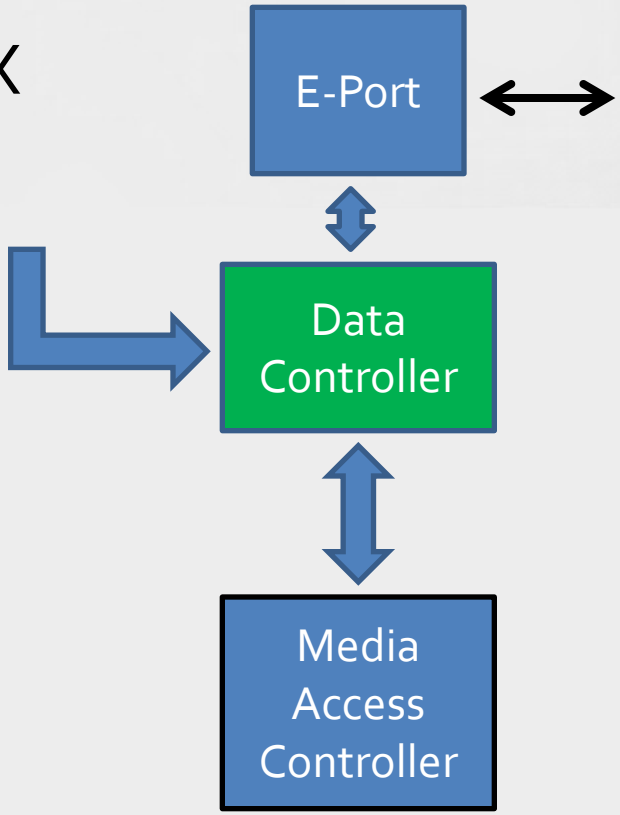
- Free standard designed for System-on-Chip IP Interconnection
- Simple, compact, logical IP core hardware interfaces that require very few logic gates
- Synchronous design
- Handshaking protocol allows each IP core to throttle its data transfer speed
- Supports normal cycle termination, retry termination and termination due to error

VAFT3 Slow Control Block Diagram



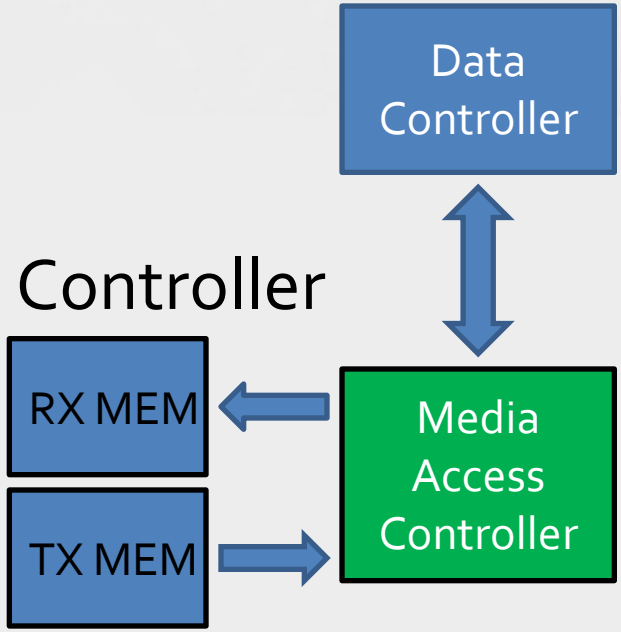
Data Controller

- Manage the readout & trigger data flow
- Data formatting
- Extract slow control bitstream in RX
- Insert slow control bitstream in TX



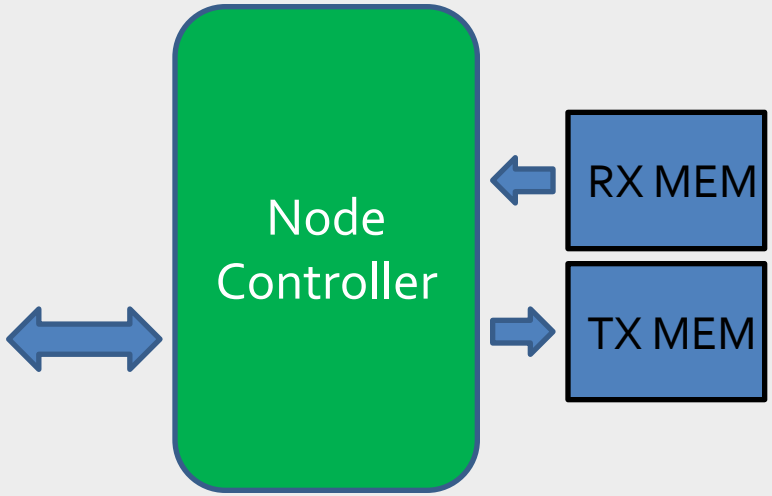
Media Access Controller

- Detect and verify command frame and align it into the RX Memory
  - Verify Frame format
  - Check the destination address
  - Remove Header
  - Verify CRC
- Forward transmit data to the Data Controller
  - Insert Header
  - Insert CRC

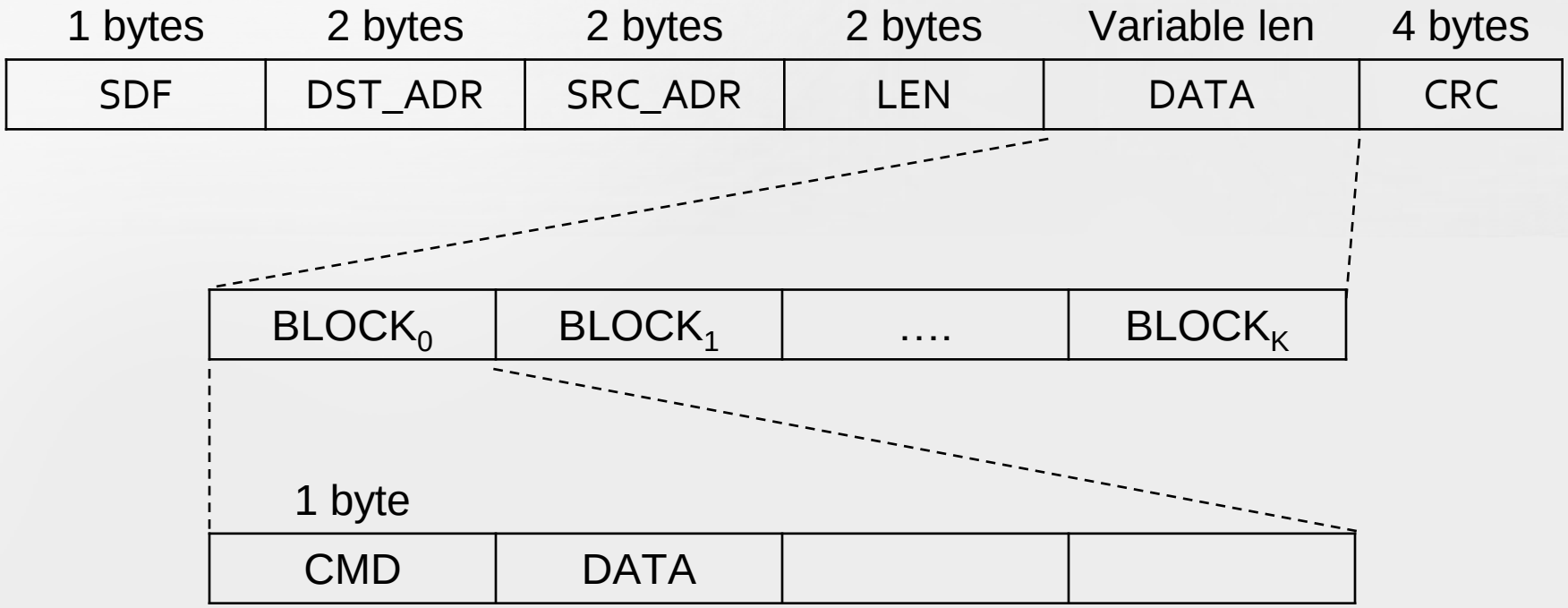


Node Controller

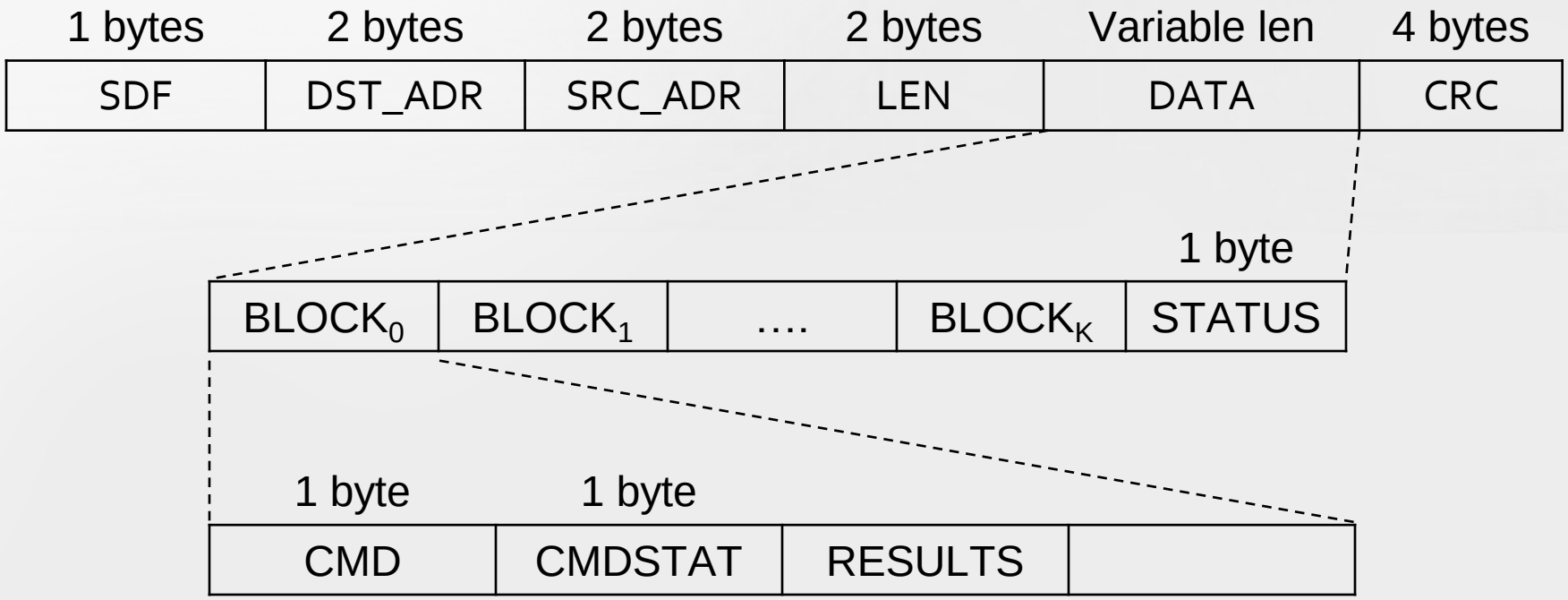
- Translate commands from the RX packet
  - Generate Wishbone bus transactions
  - Write data to registers
  - Read data from registers
- Fill the replay packet with transaction results
  - Copy command
  - Write transaction status
  - Write read data



Forward Frame Format



Replay Frame Format



Command list

- Simple Write
  - Write only one register
- Multiple Write
  - Write N bytes in N successive registers
- Multiple Write FIFO
  - Write N bytes at the same address
- Simple Read
  - Read only one register
- Multiple Read
  - Read N bytes from N successive registers
- Multiple Read FIFO
  - Read N bytes at the same address
- Reset
  - Reset the whole chip or just one block

Command status

- Everything ok
- Invalid OPCODE
- Error answer on Wihsbond bus
- Time-Out after “RTY”
- OverFlow on TX memory
- Wrong Magic Numbers

Upstream data format – Option I

Karol Buńkowski protocol proposal:

Cluster position option

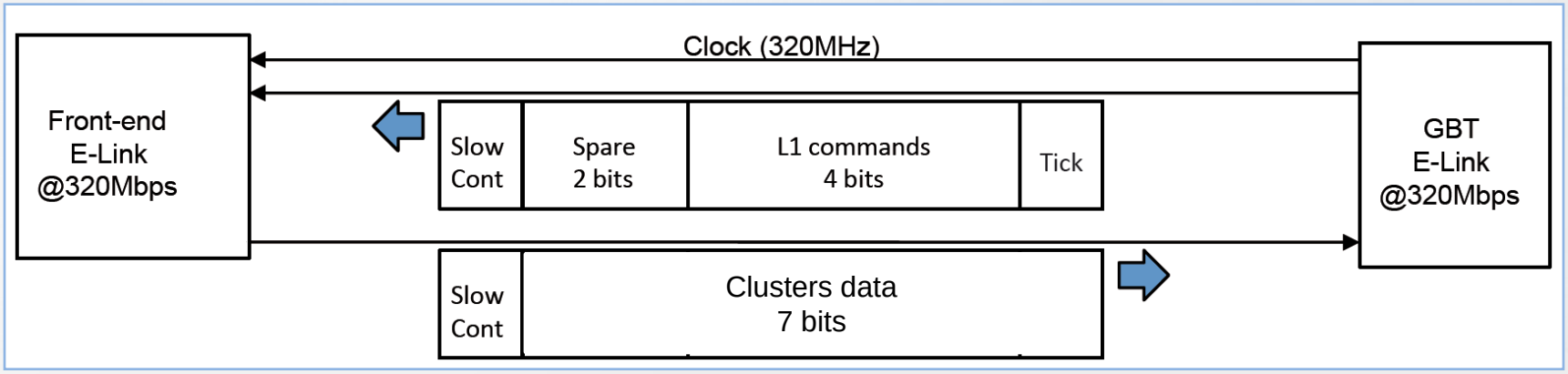
- 7 bits cluster position,
- 3 bits cluster size (**1 to 8 strips**),
- 3 bits of partition delay (**up to 8 BX latency**) ,
- 1 bit – NDL (next-data-lost) – set when there was to much frames and some were lost,

⇒ **14 bits in total (7 bits/clock)**

- **Two BXes are needed to transmit one frame**

Rate [Hz/cm^2]	Rate Hits/chip/BX	Lost frame fraction
2 339	0.01	$<10^{-8}$
4 679	0.02	$<10^{-8}$
11 697	0.05	$<10^{-7}$
23 393	0.1	1.4×10^{-5}
46 787	0.2	7×10^{-4}

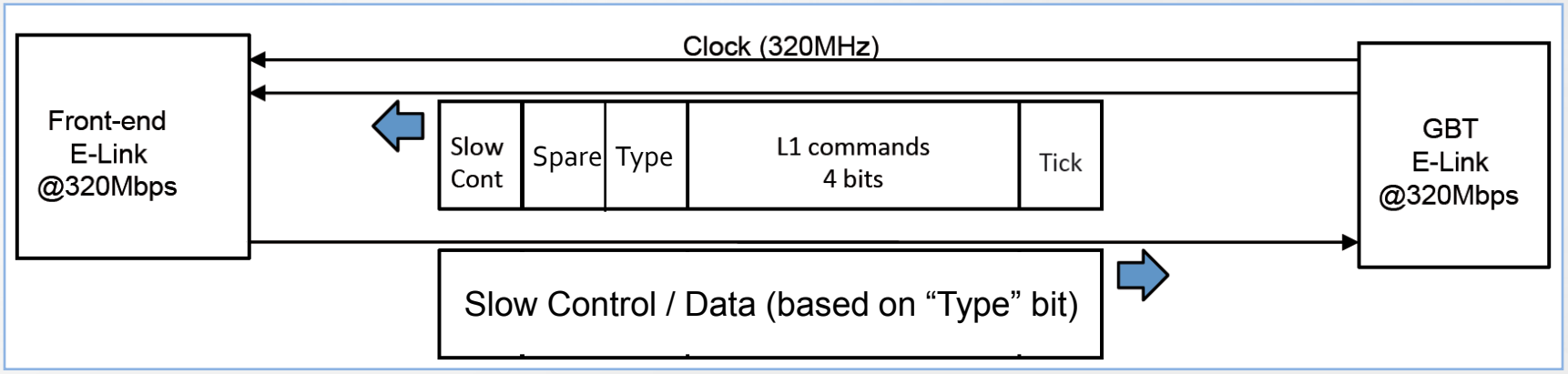
Data stream – Option I



Synchronization is required for the upstream flow.

BC0	1	1	1	0	0	0	Slow cont	⬅ IDLE
ClusterPos[3:0]				Cluster size			Slow cont	⬅ Cluster data (first half)
NDL	Delay			ClusterPos [6:4]			Slow cont	⬅ Cluster data (second half)

Upstream data format – Option II



Synchronization is required for the upstream flow.

BC0	1	1	1	0	0	0	Slow cont

Slow control packet

Trigger / Tracking data

Data packet

Upstream data format – Option II

- While running (in data mode) the chip should send idle packets with a fixed bit pattern to allow the receiver to check the link synchronization

- Many other option on data protocol
  - Center of gravity of the charge
  - Analog information
  - …..