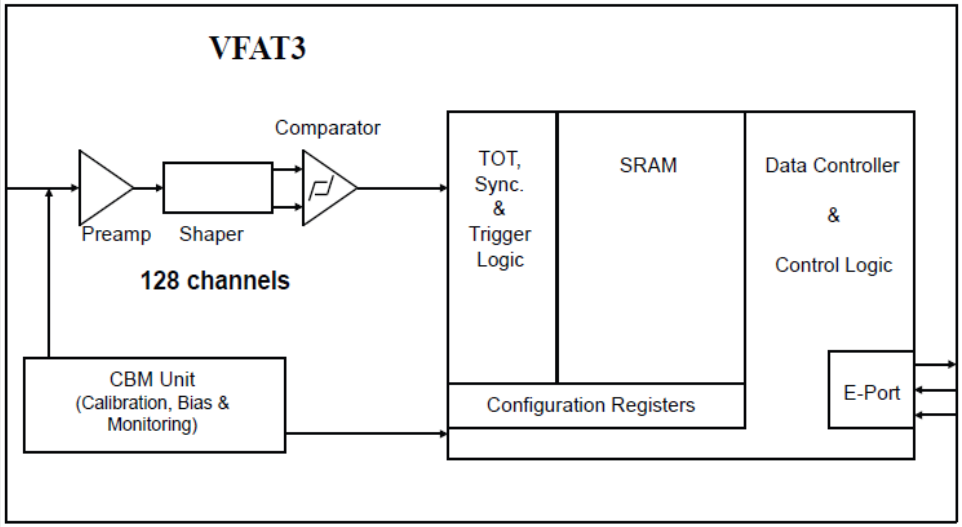
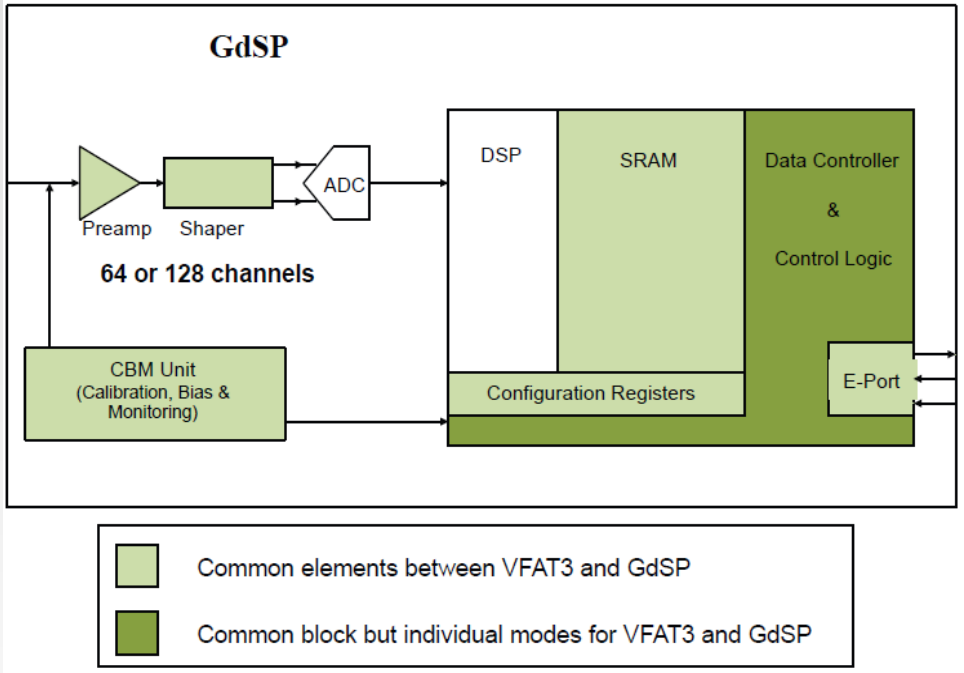
ToT and DSP

IIHE Brussels

Context

- Digital part of the ASIC, between analog front-end and memory





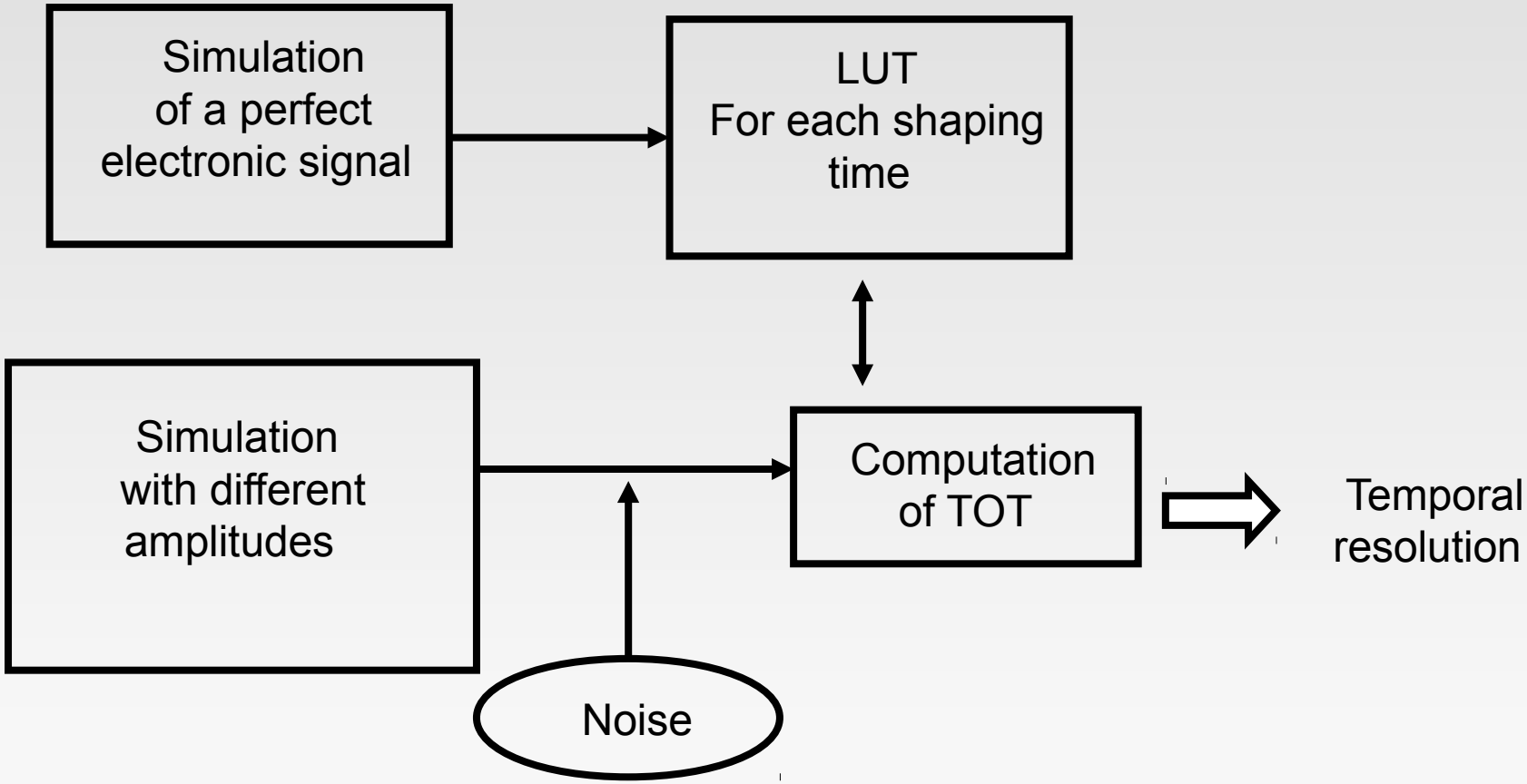
- Still considering vFAT (ToT) and GdSP approach

Conclusions of last meeting

- We need more info about:
  - Signal shape out of a GEM
  - Resolutions (time here)
  - Parasitic signals (noise, common mode...)
  - The shaper (needs + implementation)

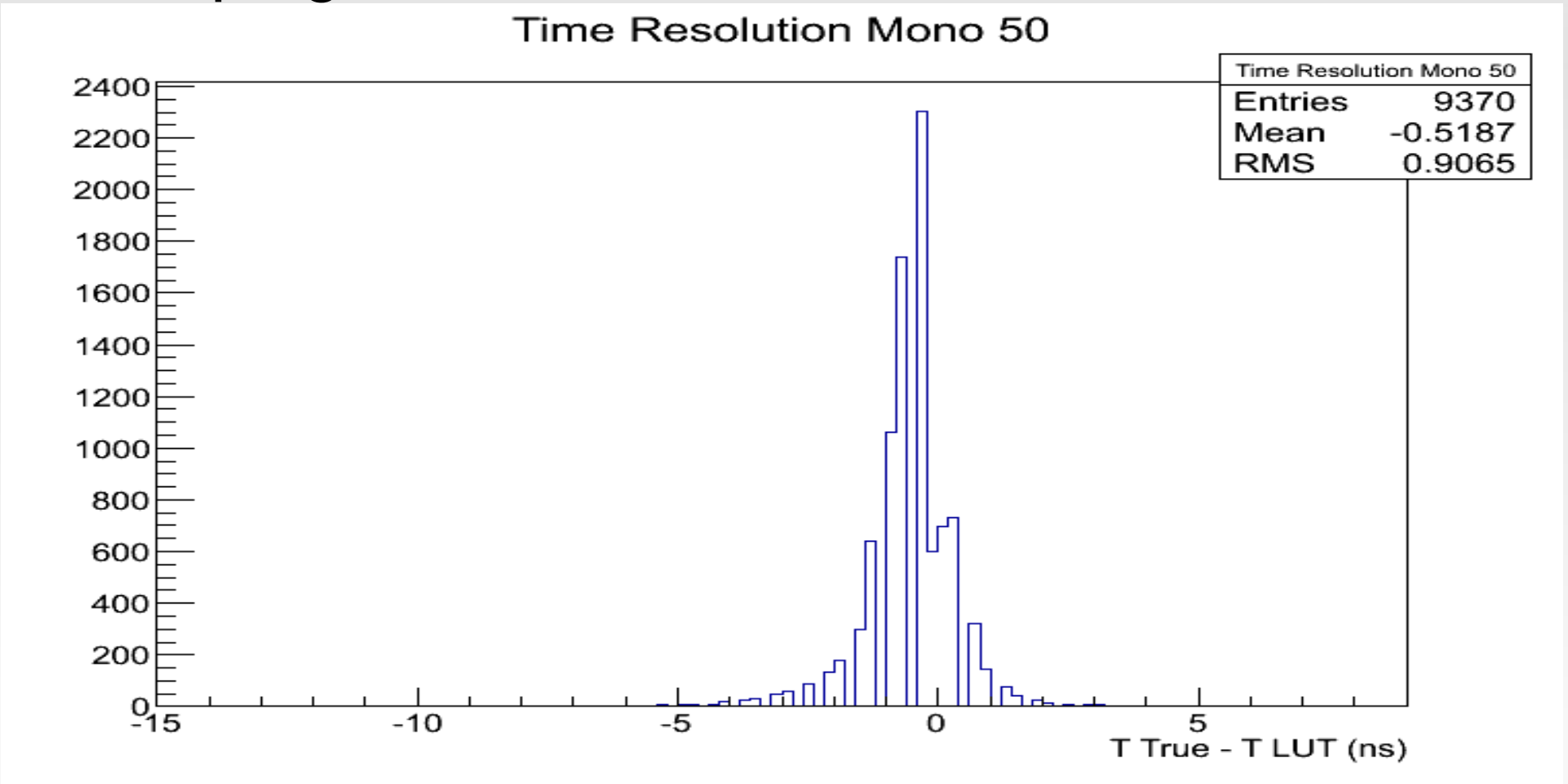
Resolution (ToT)

- Thierry Maerschalk (IIHE)



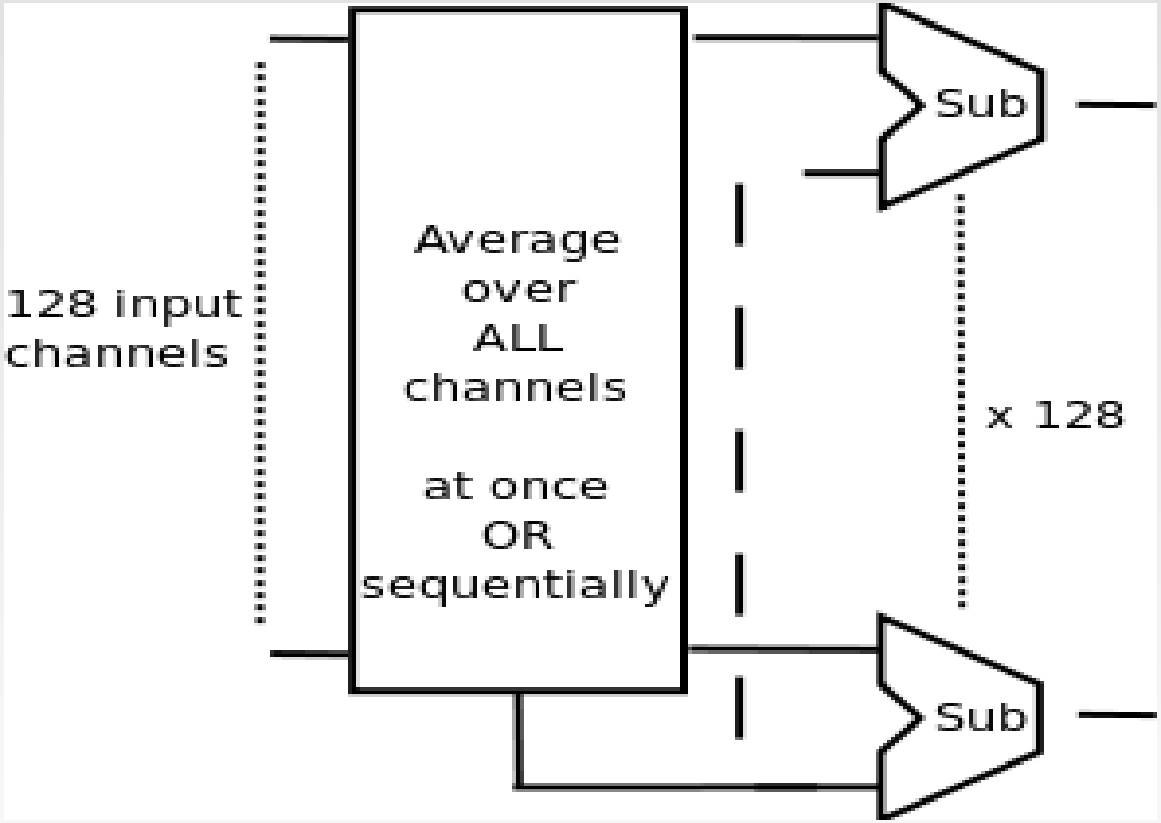
Resolution (ToT)

- Shaping time: 50 ns, Fclk: 320 MHz



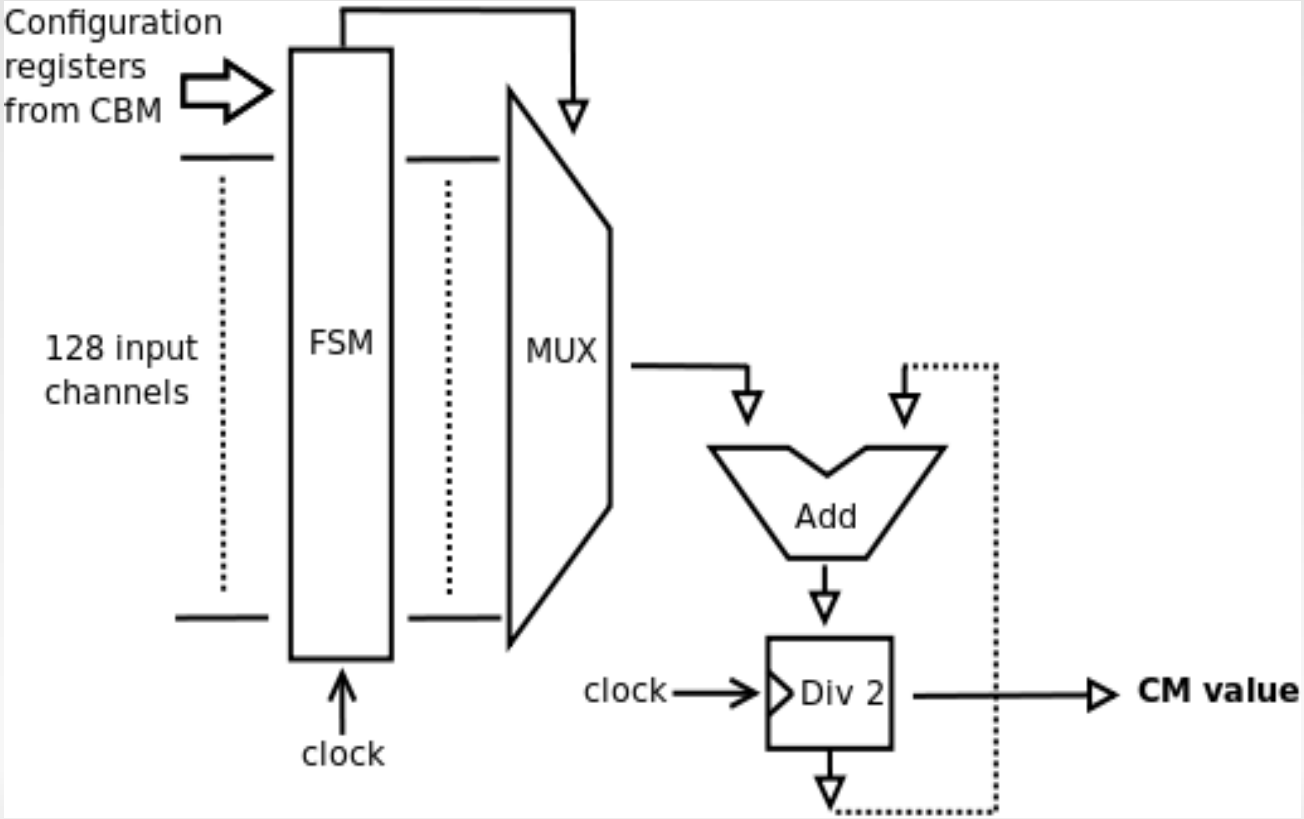
Common mode

- Detection + subtraction

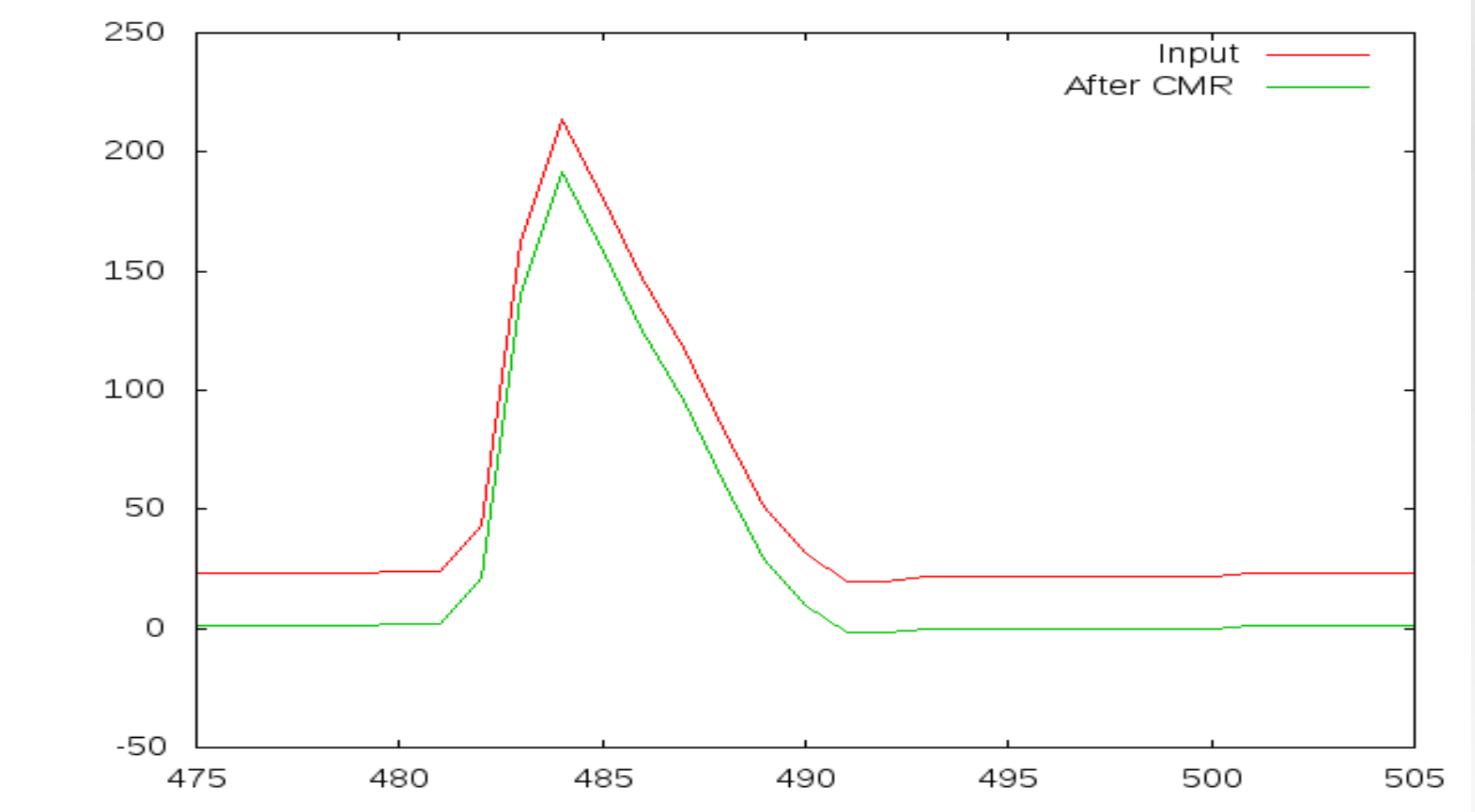


Common mode

- Full parallel = more than 30k transistors and propagation delay of ~3000 gate delays
- Sequential:

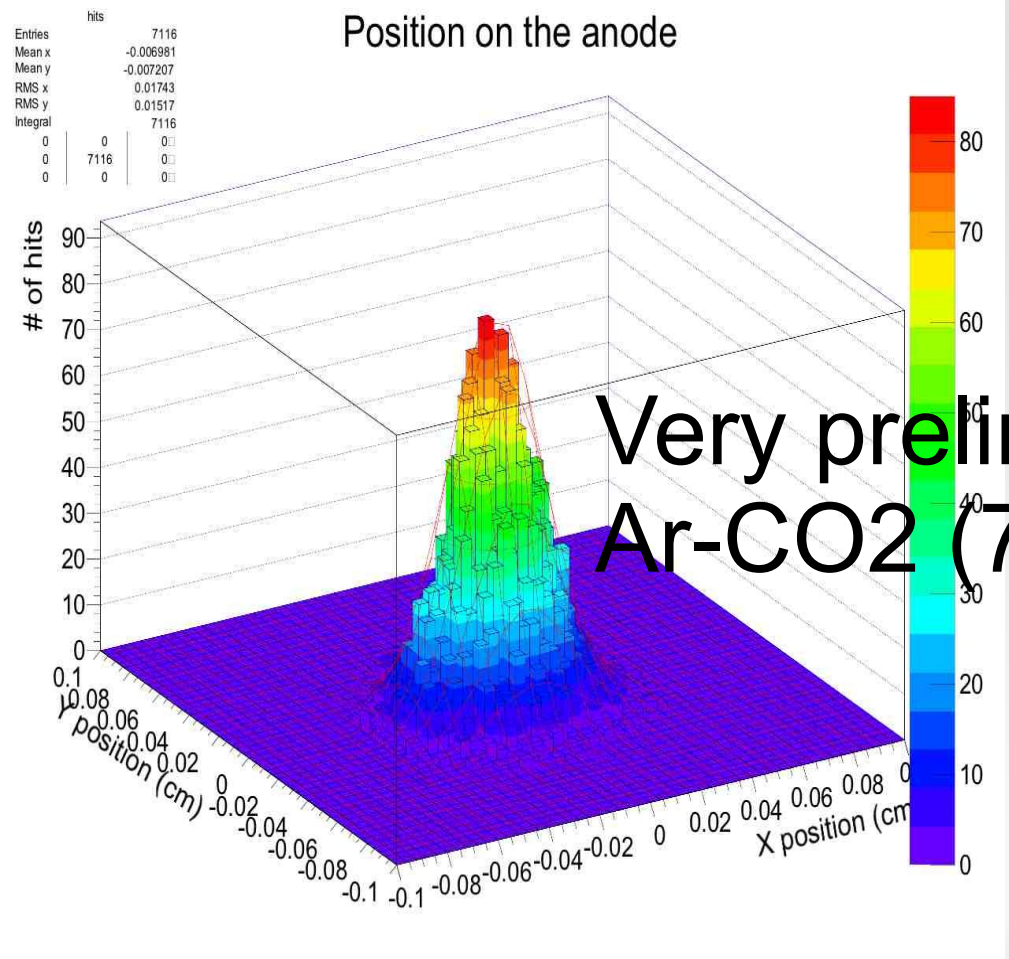


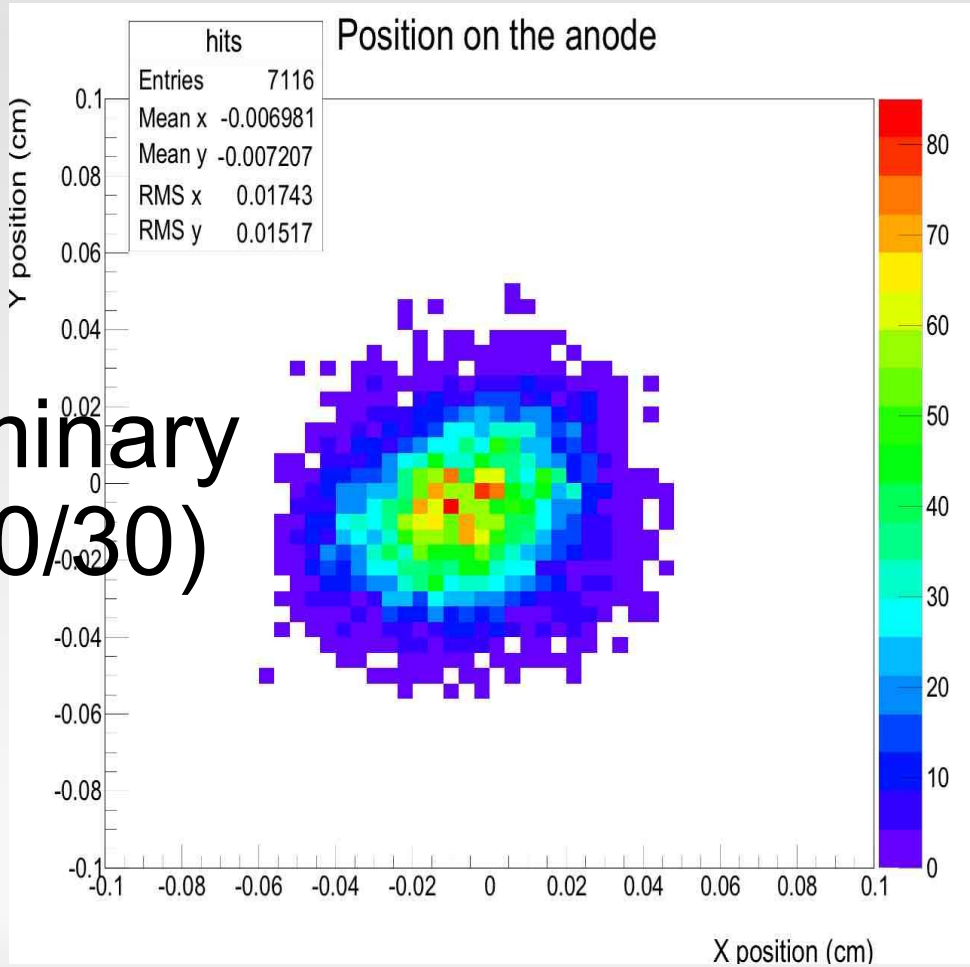
Common mode – ONE channel hit



Signal shape – GEM output

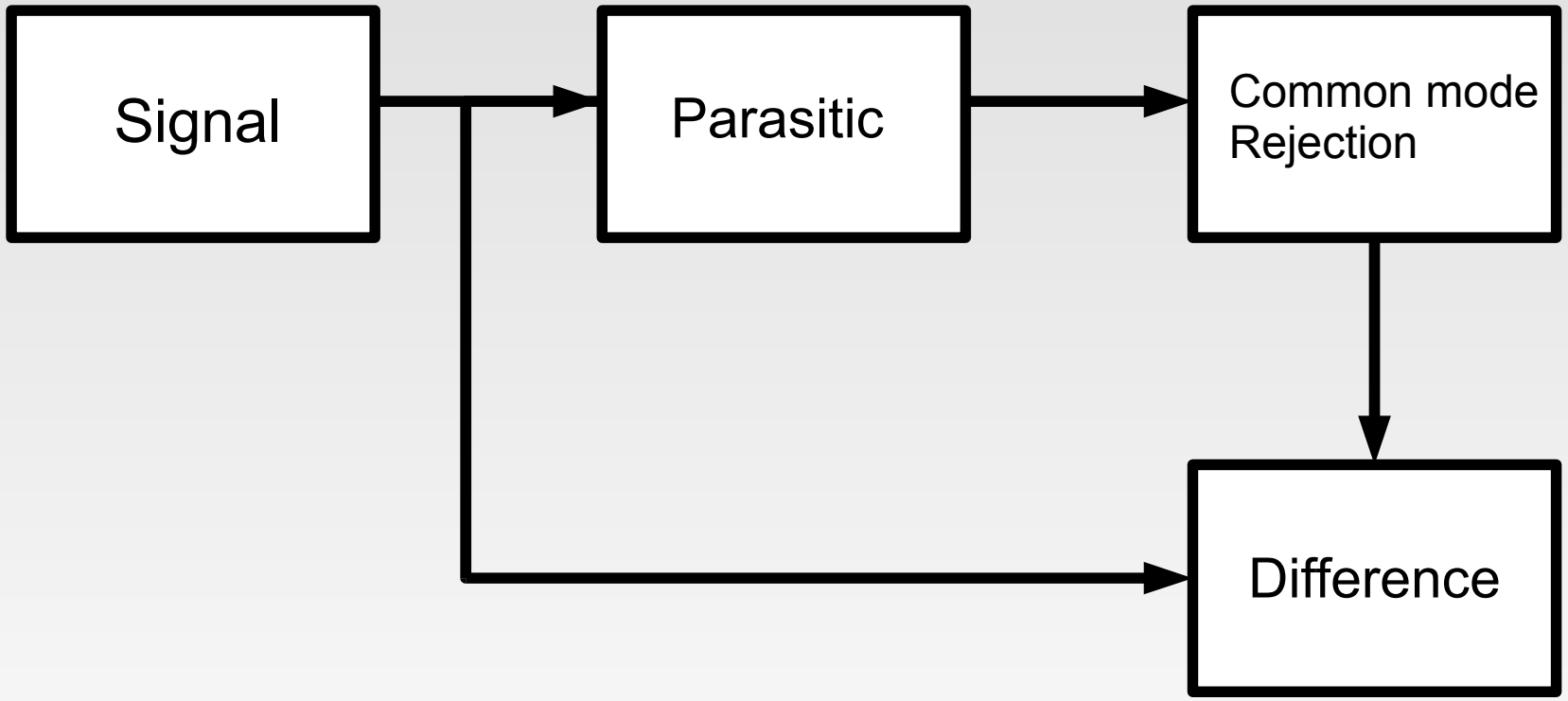
- GARFIELD Simulation, Geoffrey Mullier (IIHE)



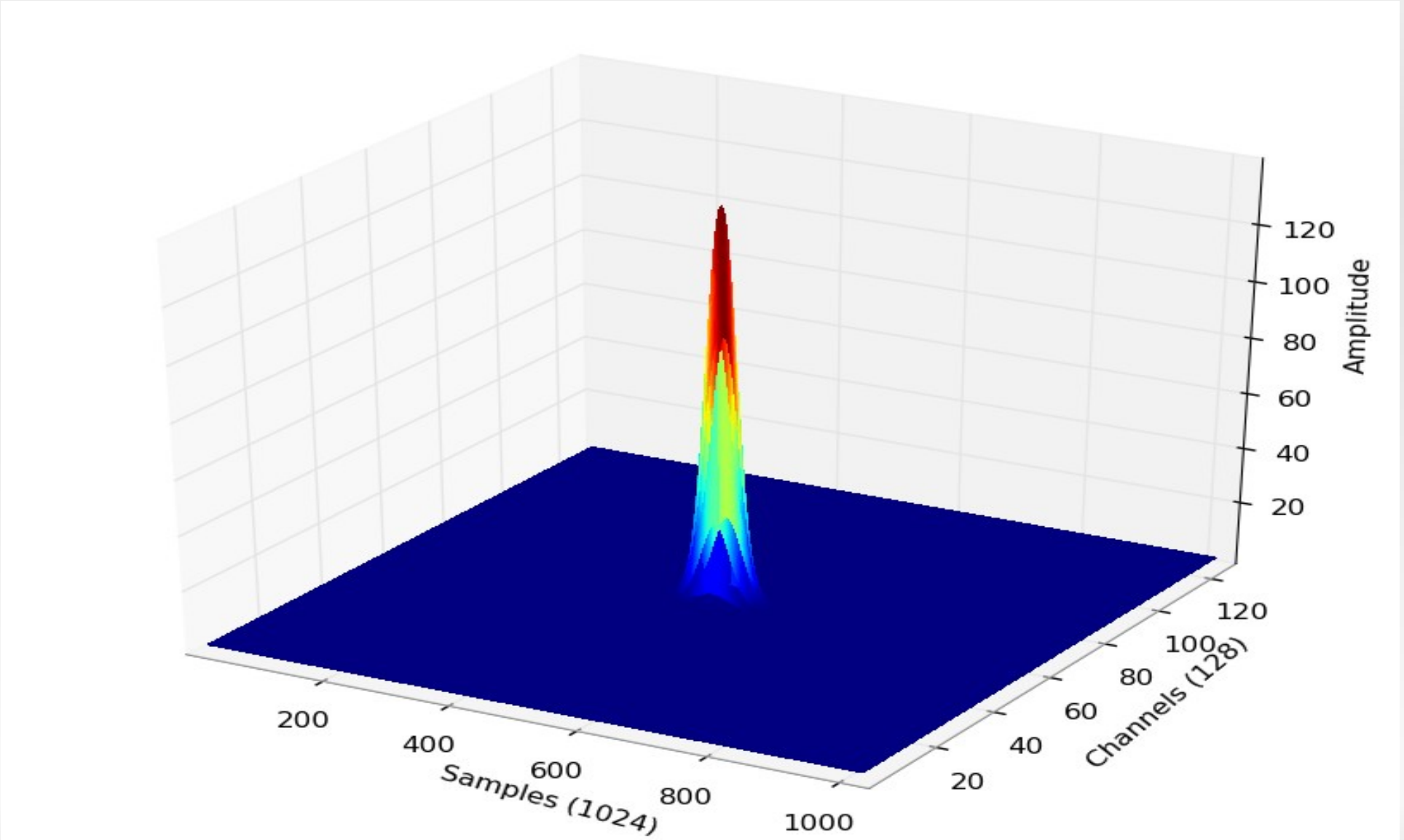


Very preliminary
Ar-CO2 (70/30)

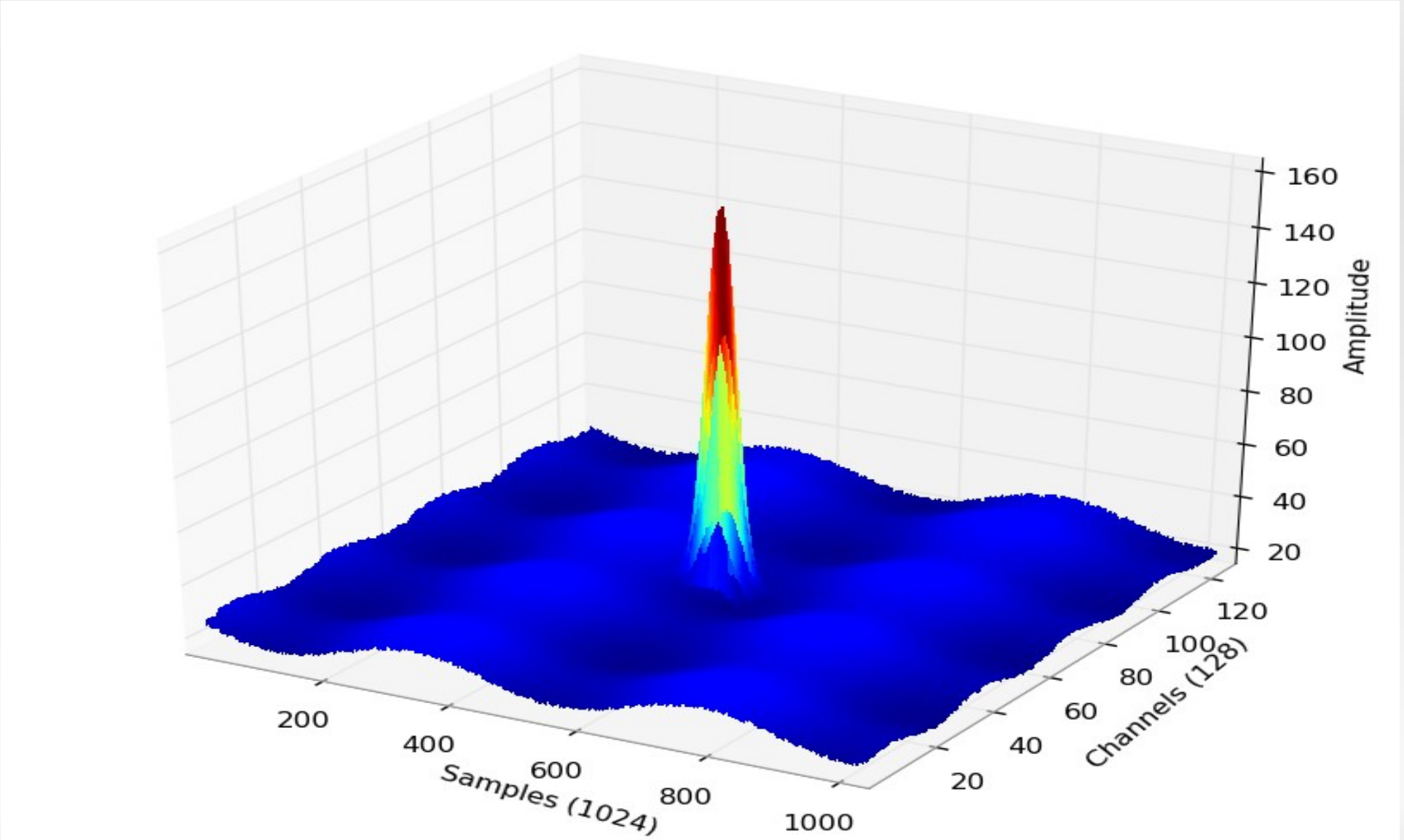
Common mode – ALL channels



Common mode - Signal



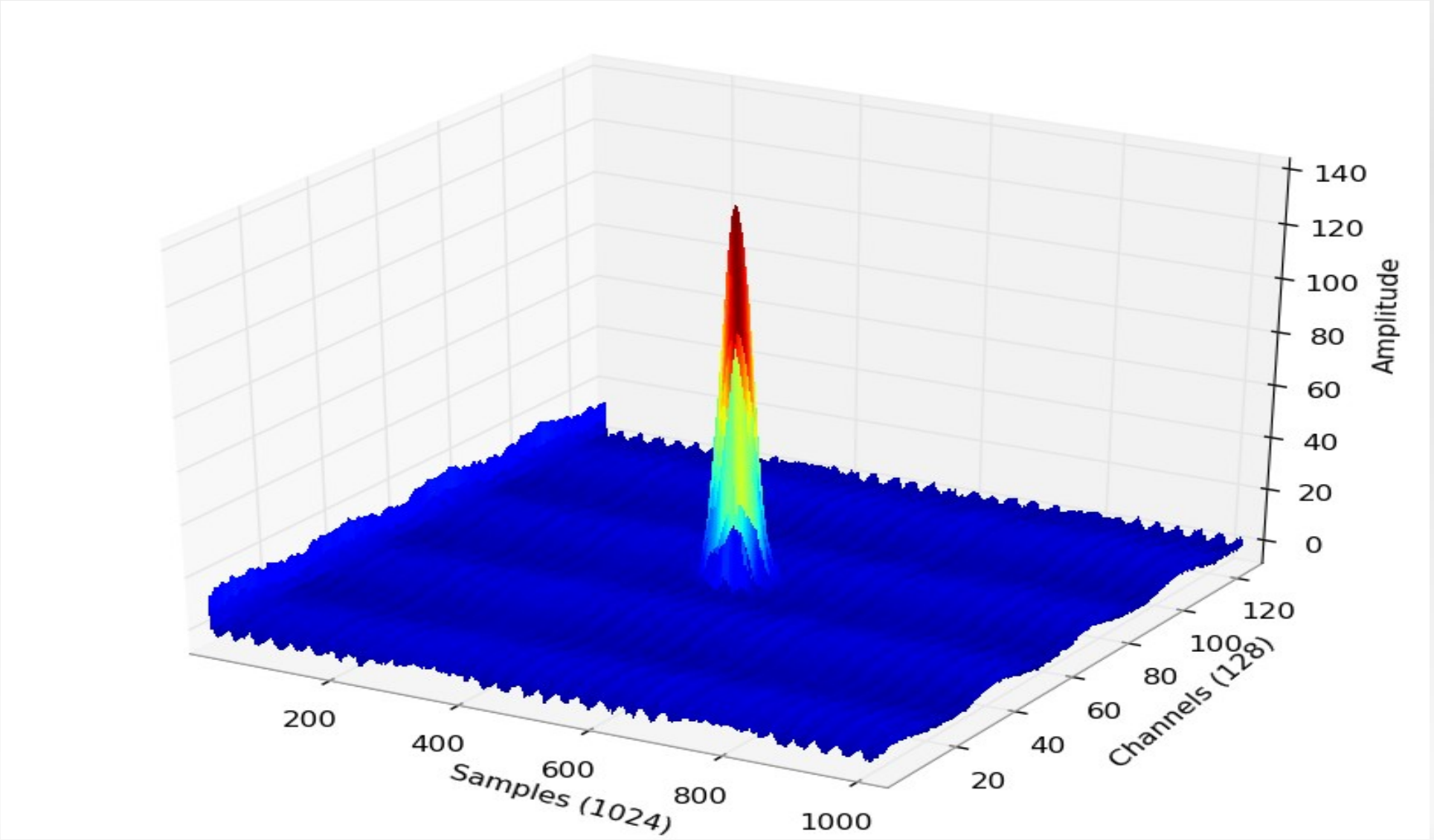
Common mode - Parasitics



Common mode - results

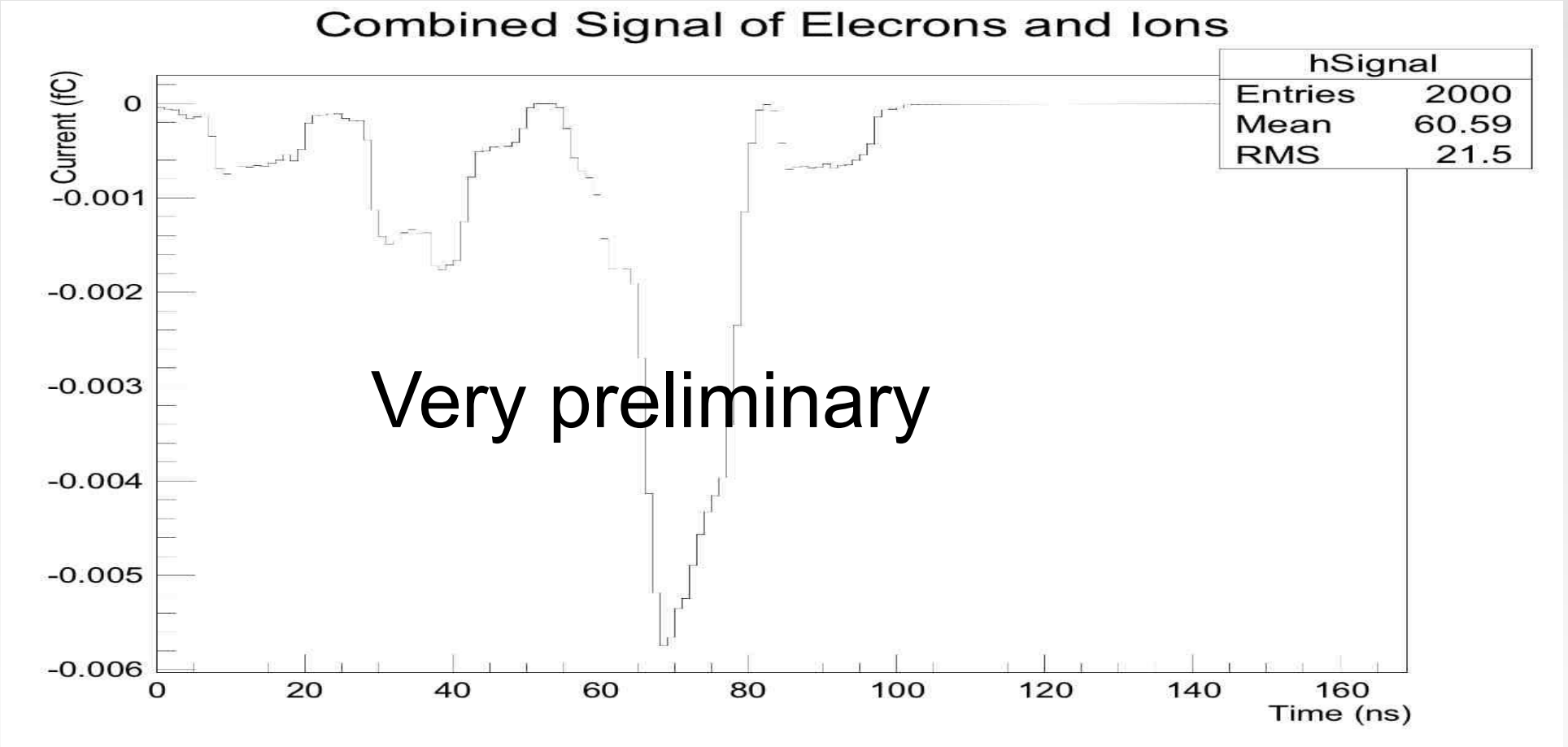
- Learning phase, but quick converge
- Need good channel exclusion mechanism
- Different cases:
  - Static common mode: VERY GOOD
  - Static + variation: VERY GOOD
  - Static + noise: GOOD (static is gone)
  - Static + space variation: less good (static gone)

Common mode - results



Shaper – Work in progress

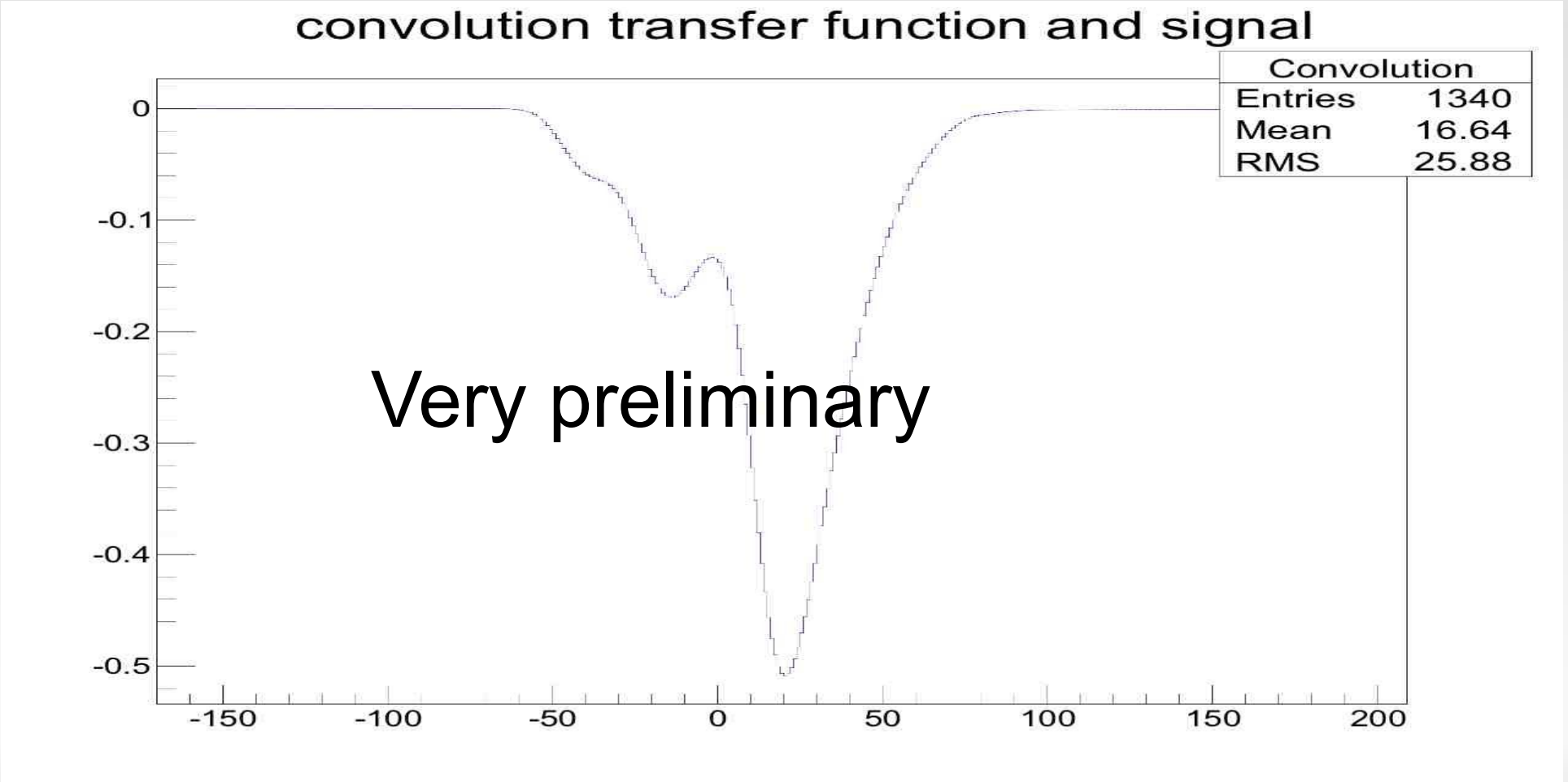
- Simulated signal (GARFIELD)



Shaper – Work in progress

- Useful for shaper time estimation

Using transfer function from Fabrice (CRRC²,20ns)



Outlook

- We have all the building blocks to perform thorough simulations
  - Signals
  - Shaper
- Make a RTL prototype
  - Timing analysis (critical paths, latency...)
  - Idea of the area (transistor count)