

GBT Project Status

Paulo Moreira

CERN

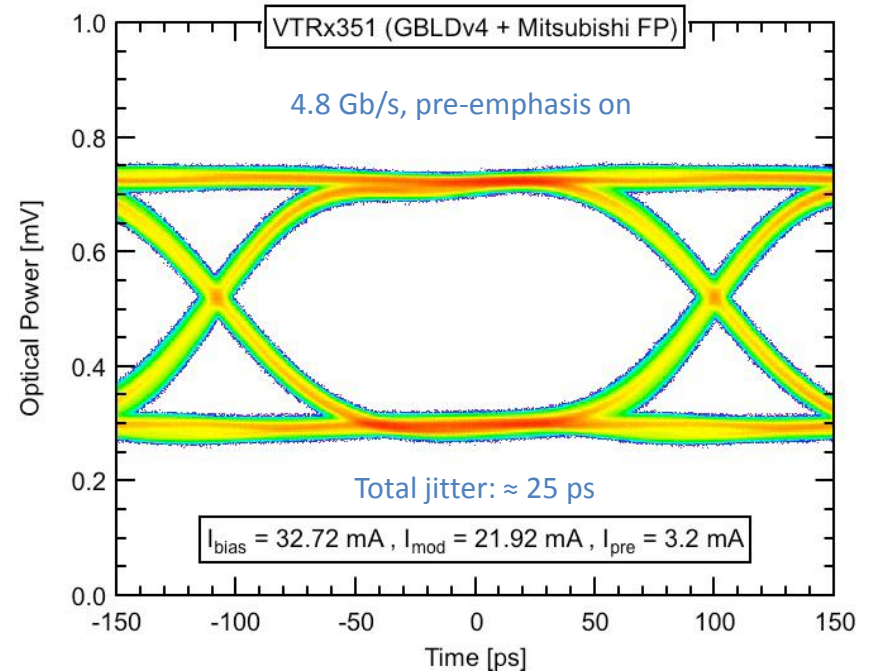
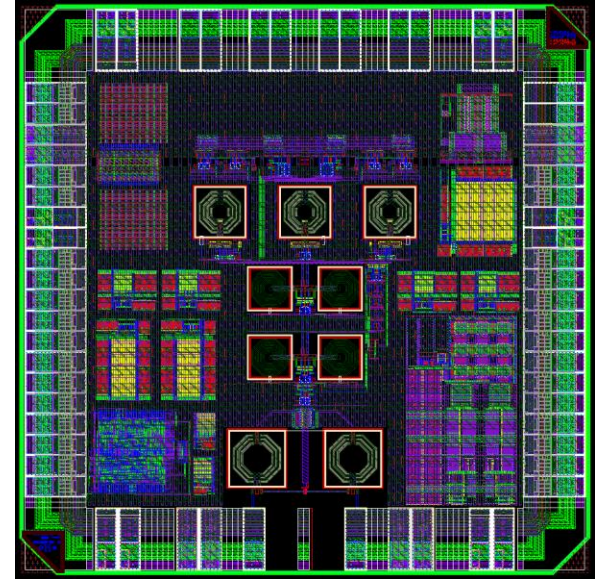
19 April 2012

Outline

- GBLD
- GBTIA
- GBTX
- GBT-SCA
- GBT Project Future

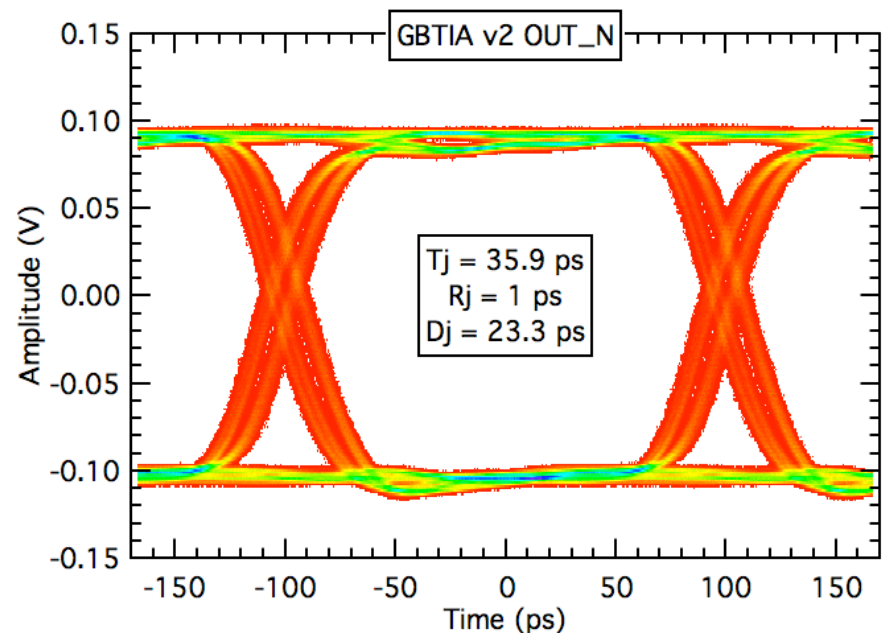
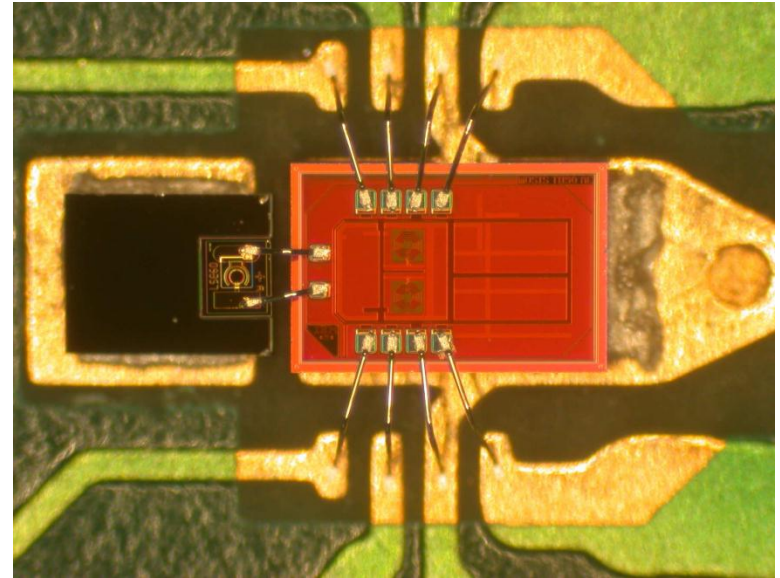
GBLD - Status

- GBLD V4 performs according to specs (+):
 - Modulator
 - Laser bias
 - Radiation hardness still to be tested.
 - Planned for the week of the 8th of May
- If there are no surprises with the radiation tests, the ASIC is production ready!
- Chips currently available in small quantities: ≈ 120 chips
- Small “production” run
 - May: ≈ 400 chips
- Next step:
 - Integration in the Versatile Link



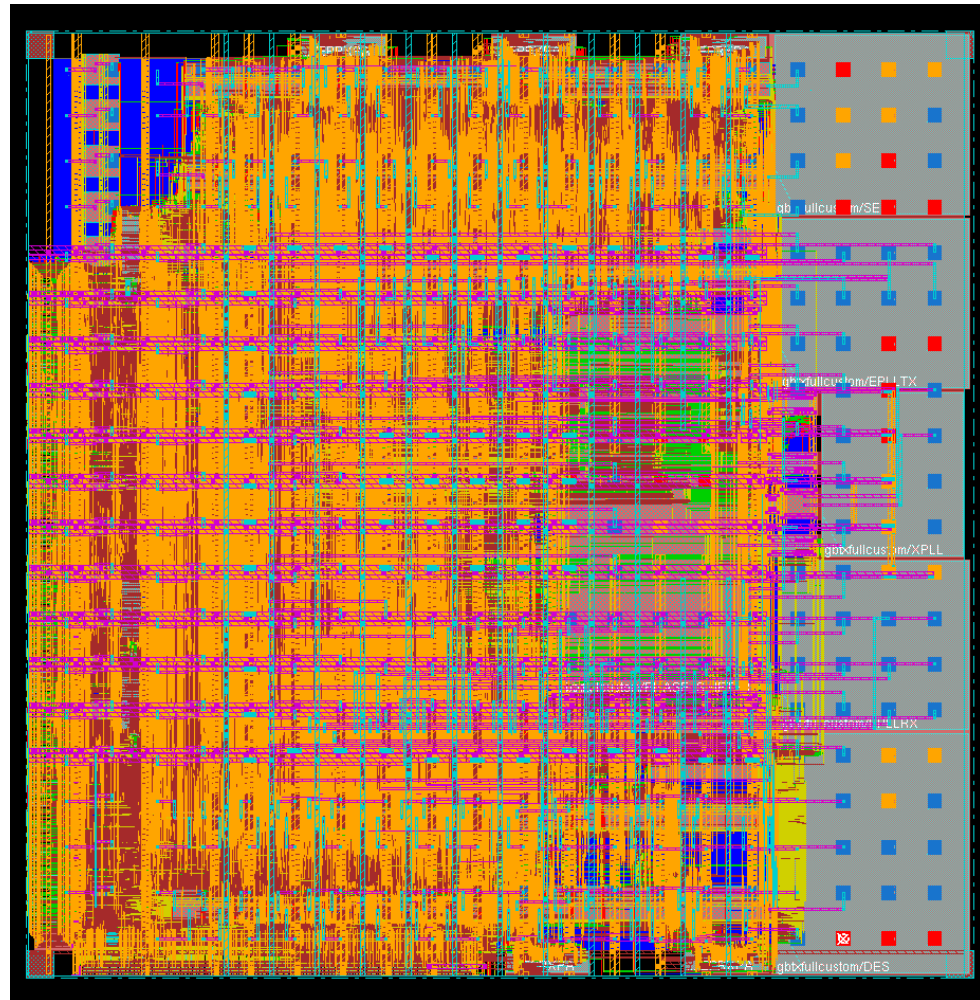
GBTIA - Status

- First version fabricated in 2008:
 - Fully functional
 - Performance according to specifications (+)
- New version fabricated in 2012:
 - New pad layout
 - Received Signal Strength Indication (RSSI)
 - To facilitate optical fiber/PIN-diode alignment.
 - Higher reversed bias voltage for the PIN-diode
 - Voltage regulator 2.5 V to 2.0 V
 - Tests results reveal performance similar to the first version
- Chips currently available in small quantities: ≈ 240 chips
- Small production run:
 - August 2012, $\approx 200/400$ chips
- Next step:
 - Packaging and integration in the Versatile Link



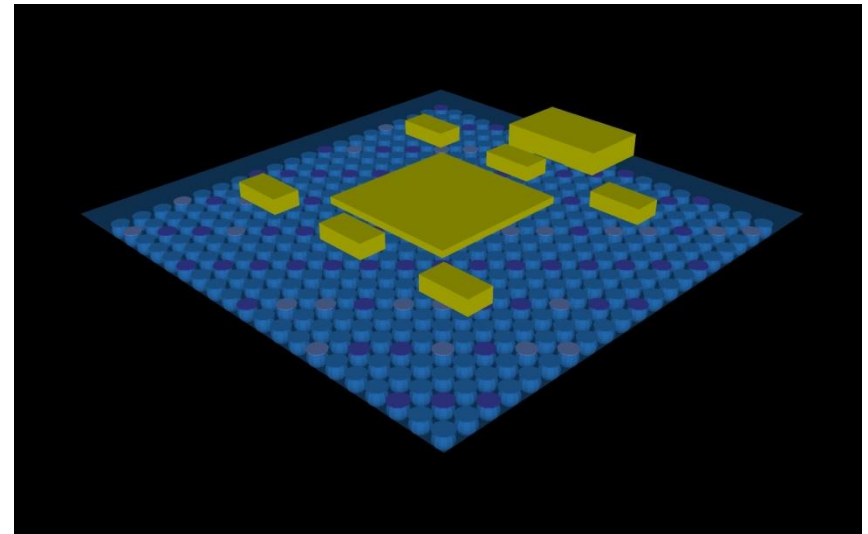
GBTX - Status

- GBTX team currently hard working towards the:
 - 6th of August MOSIS submission
 - Layout work very close to completion
 - Still quite a bit of verification work to be done
- Preparation of the test-setup currently running in parallel with the ASIC design
- Forecast:
 - Submission: 6th of August 2012
 - Chips back from foundry:
 - November 2012
 - Chips packaged
 - Feb 2012
 - Prototypes available for distribution:
 - May 2013



GBTX - Package

- Package:
 - 20 × 20 ball array
 - 0.8 mm pitch
 - Size: 17 mm × 17 mm
- Package:
 - Manufactured by ASE:
 - Integrate the decoupling capacitors
 - Integrate the XTAL
- Package development by ASE has already started



GBT – SCA Status

- Dedicated to slow control functions

- Interfaces with the GBTX using a dedicated E-link port
 - Standard e-Ports in the 80 Mb/s can be used as well
- Communicates with the control room using a protocol carried (transparently) by the GBT

- Implements multiple protocol busses and functions:

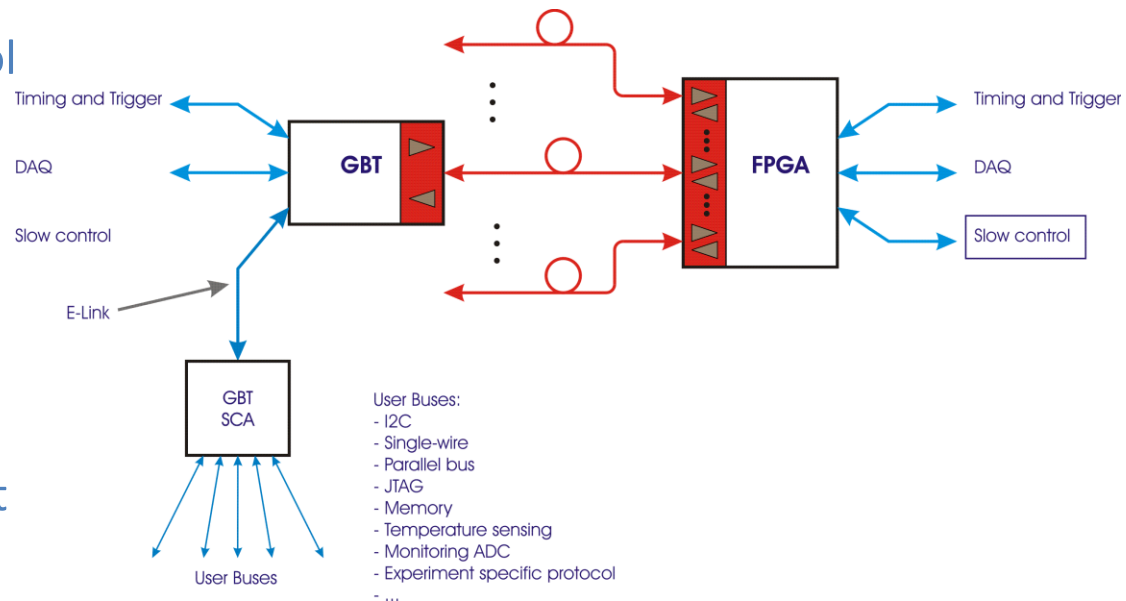
- I2C, JTAG, PIA, etc...

- Implements environment monitoring functions:

- Temperature sensing
- Multi-channel ADC
- DAC

- RTL code under development

- Submission date
 - 5th of November 2012
- Chips packaged:
 - February 2013
- Prototypes available:
 - May 2013



GBT Project Future

- LpGBT: Low power GBT chip set
 - Reduce the GBT chipset power consumption to $\sim \frac{1}{4}$ (~ 500 mW)
 - Two “SERDES” ASICs:
 - Simple SERDES with reduced functionality
 - Low pin count and footprint (targeting tracker developments)
 - Simple parallel port
 - Full GBTX functionality
 - General purpose
 - E-Links
 - High bandwidth capability:
 - Downlink 4.8 Gb/s (as in the GBTX)
 - Uplink two modes: 4.8 and 9.6 Gb/s
 - E-Links double the bandwidth in the 10 Gb/s mode
 - Technology: 65 nm CMOS
 - LpGBT – SerDes
 - LpGBTX
 - LpGBTIA and LpGBLD will be very likely kept in 130 nm CMOS
- Serious development effort to start summer 2012
 - Target:
 - LpGBT – SerDes prototypes in 2014
 - LpGBTX prototypes in 2015