
VFAT2 hybrid and SRS design & production

Sorin Martoiu, RD51-CERN

Outline

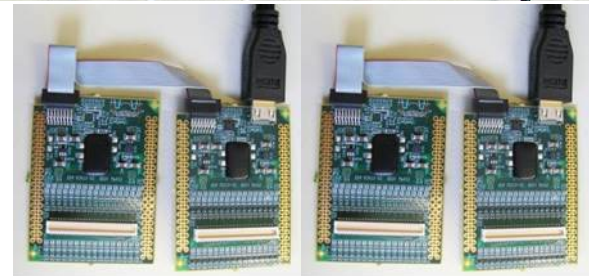
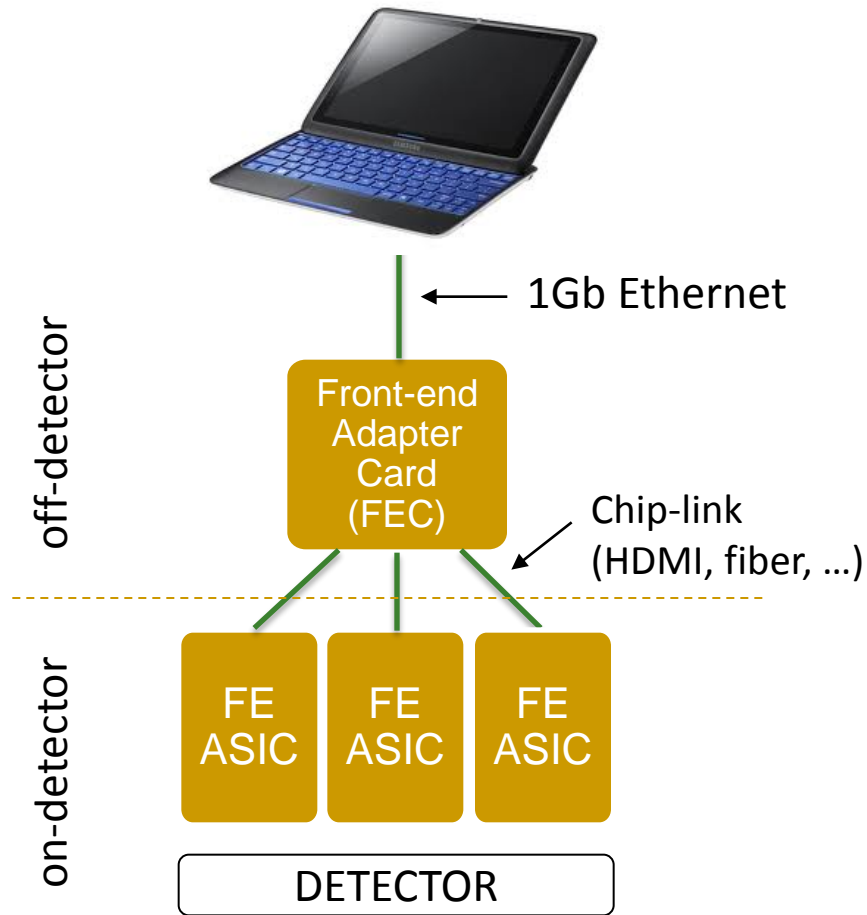
- Scalable Readout System (SRS) overview
- VFAT2 integration
 - VFAT2 Hybrids
 - Digital adapter card
- Summary

Scalable Readout System

- Product of the RD51 Collaboration for the Development of Micro-Pattern Gas Detectors Technologies
- General purpose multi-channel readout solution for a wide range of detector types, detector complexities, and different experimental environments.
- Scalable - size
 - Only point-to-point links. No busses
 - Star topology
- Scalable - application
 - Allows the use of different front-ends
 - Can integrate different sub-detectors DAQ in the same system
- Cost effective
 - Use of cost effective components from high-volume markets (eg. HDMI cables, PCIe connectors, Cat5/6 UTP cables, ...)

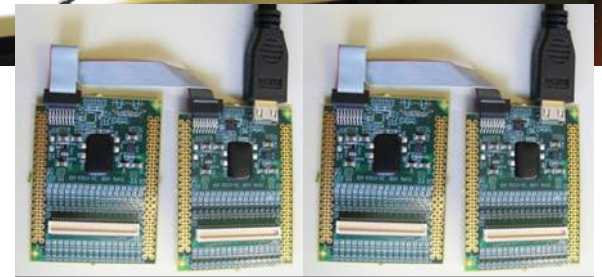
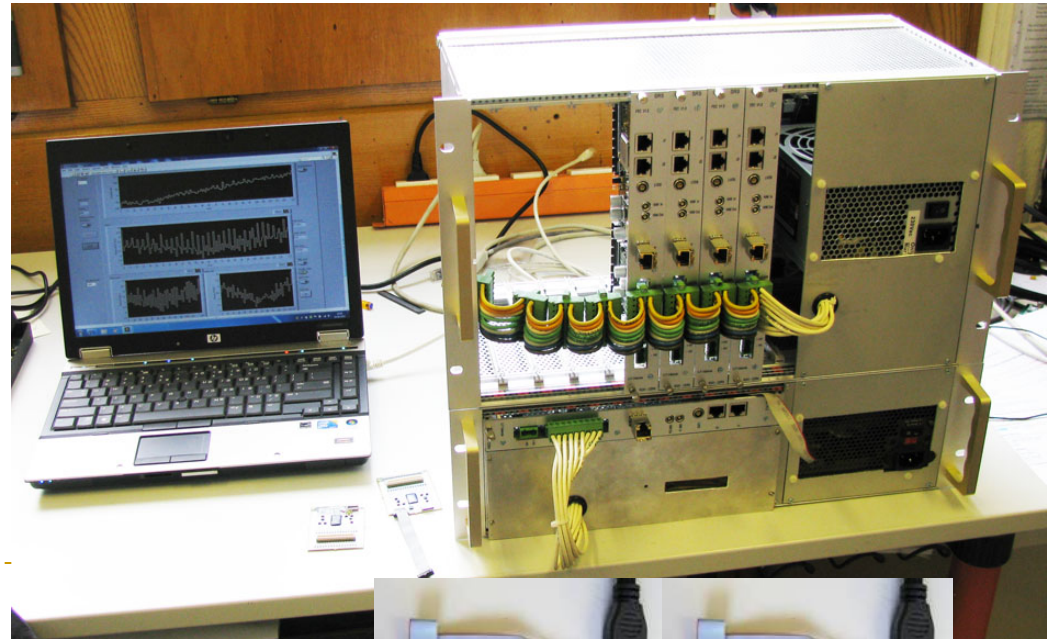
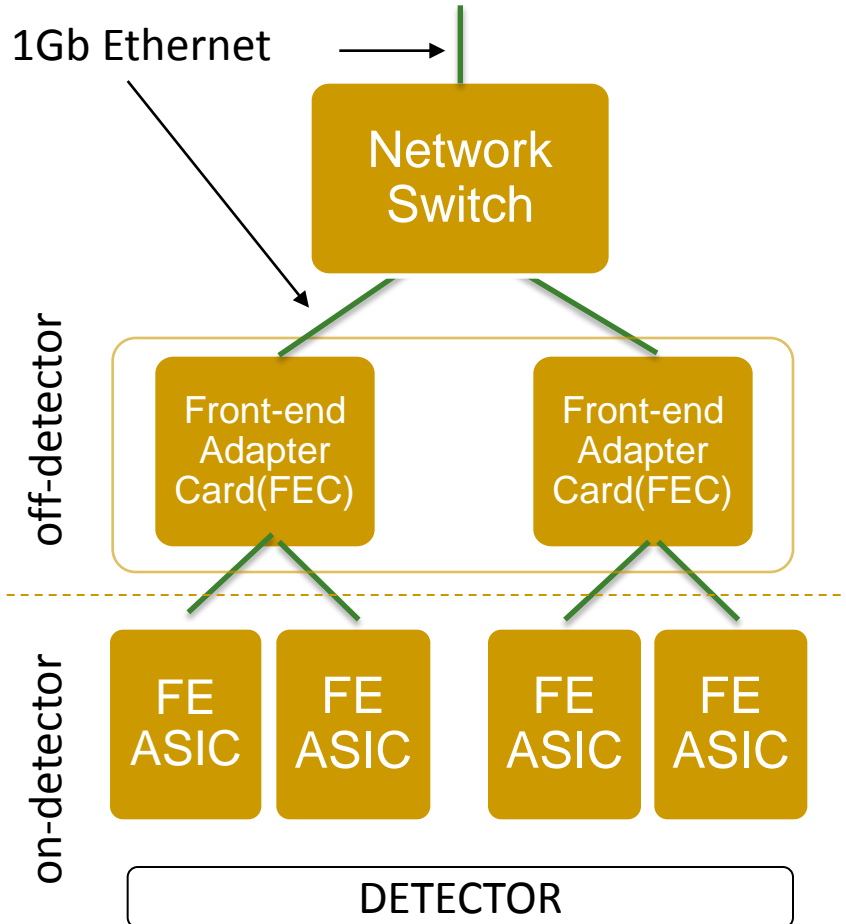
Scalability Concept

System Size (small)



Scalability Concept

System Size (medium)



Scalability Concept

System Size (large)

1/10/40.. Gb Ethernet
(opt. DDL/S-Link/...)

Scalable
Readout
Unit (SRU)

DTC Link
(Data, Trigger & Control)

Eurocrate

Front-end
Adapter
Card(FEC)

Front-end
Adapter
Card(FEC)

Front-end
Adapter
Card(FEC)

FE
ASIC

FE
ASIC

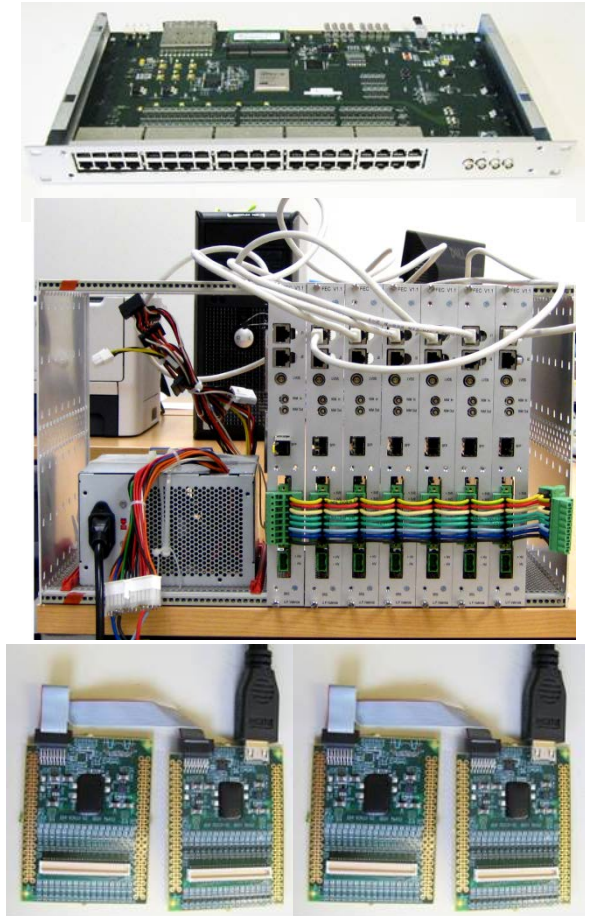
FE
ASIC

FE
ASIC

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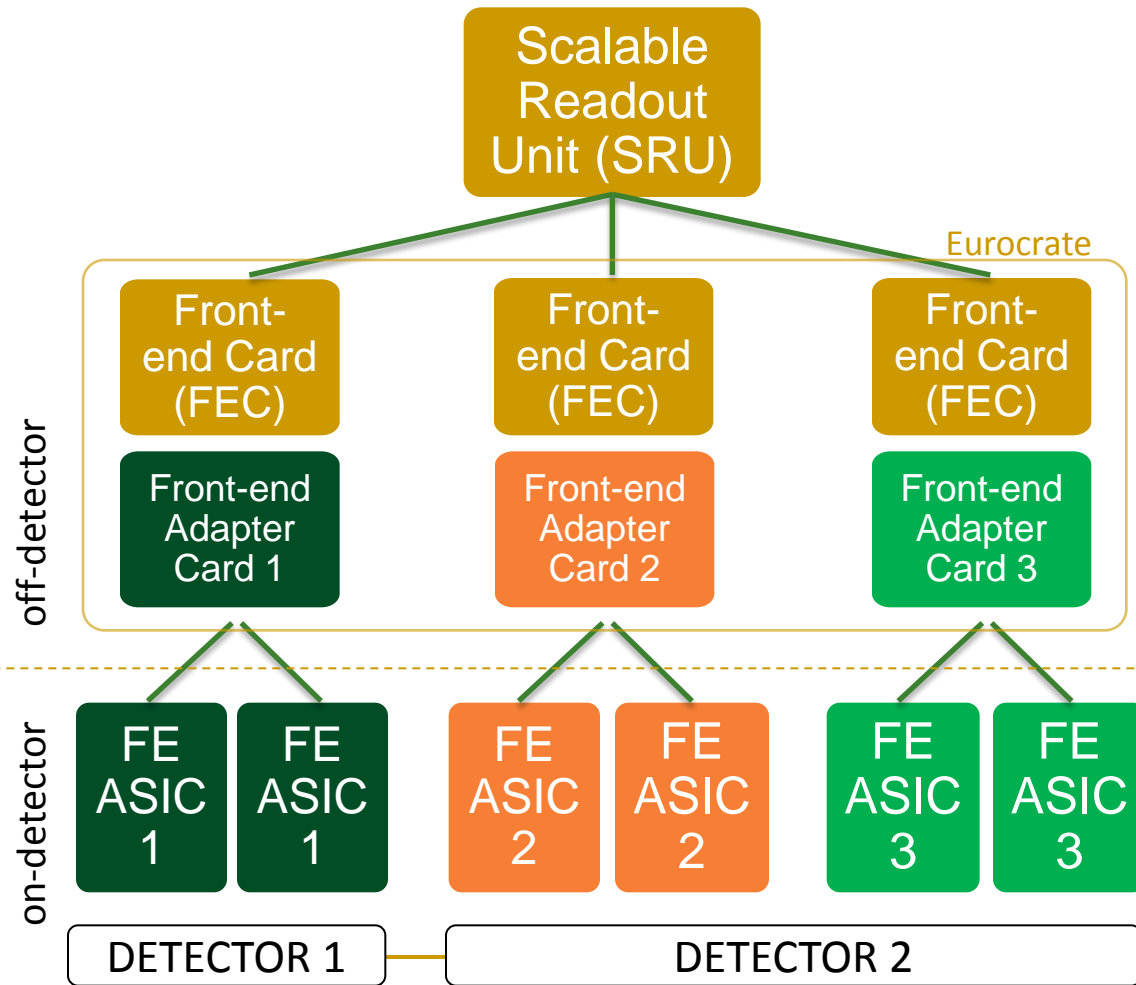
FE
ASIC

DETECTOR



Scalability Concept

Application

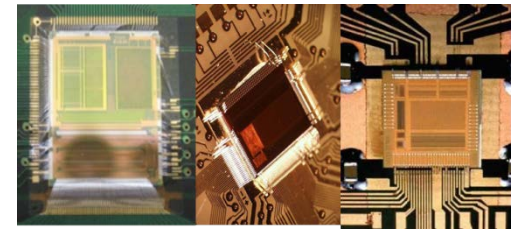
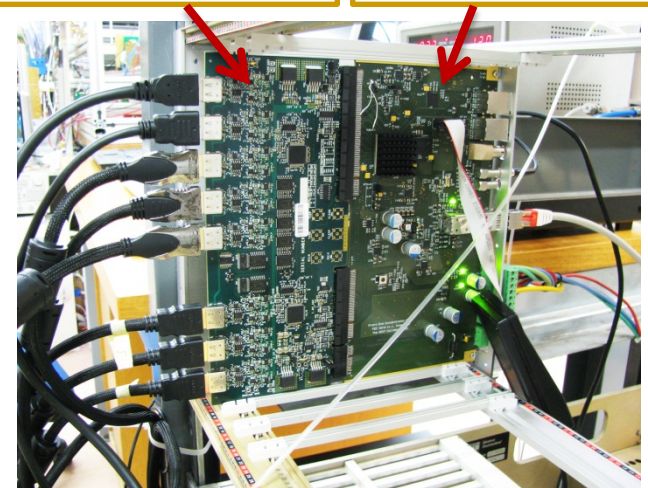


Front-end adapter

- ADC card
- digital FE card (VFAT)
- GBT receiver
- ...

Front-end FPGA card (SRS standard)

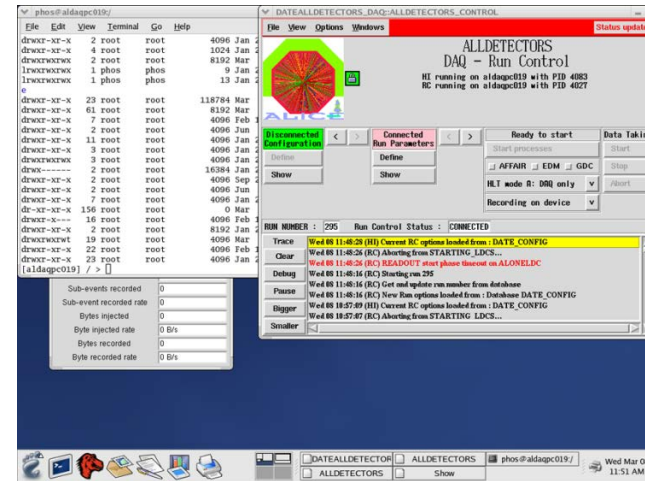
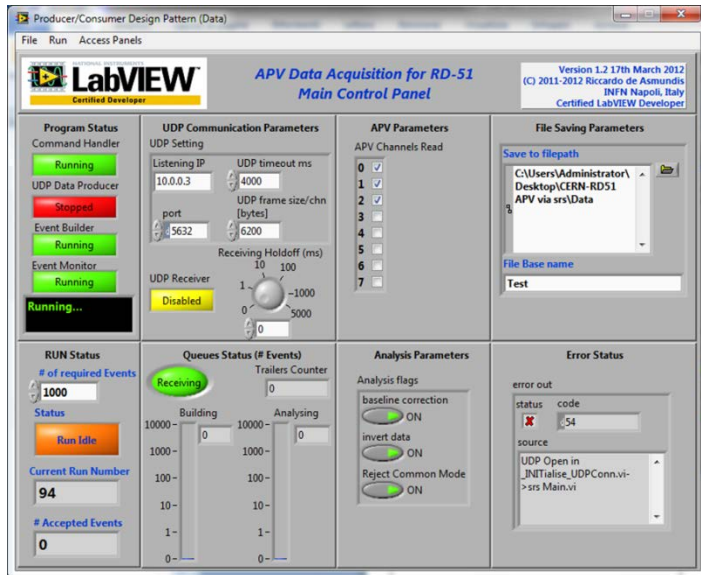
- SRS DAQ & control
- application specific firmware



Online software for SRS

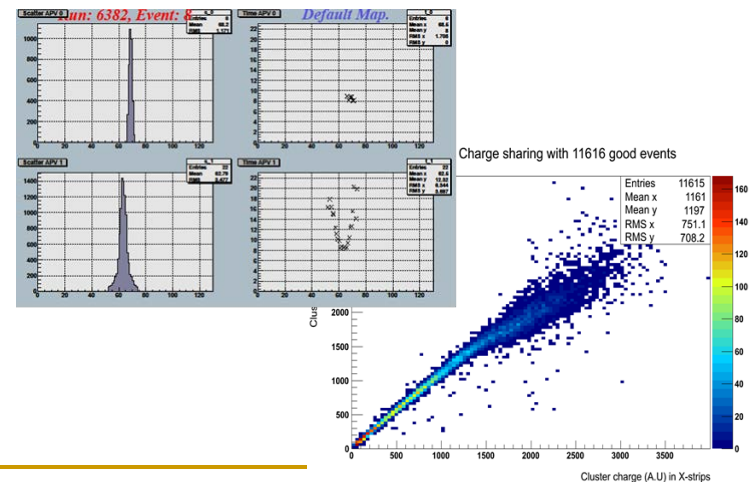
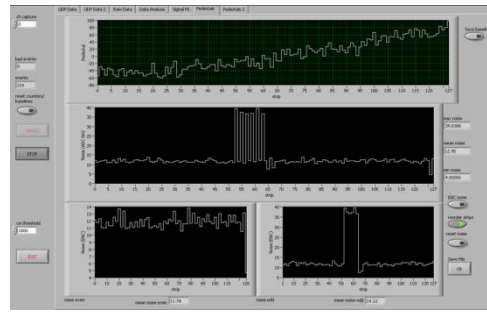
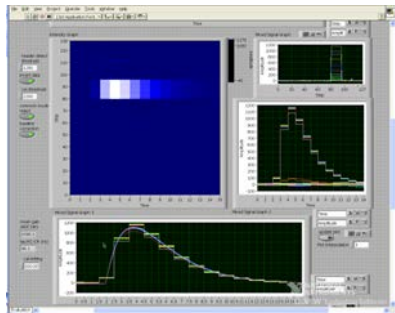
SRS-Labview

DATE , MMDAQ , RCDAQ (Linux based)



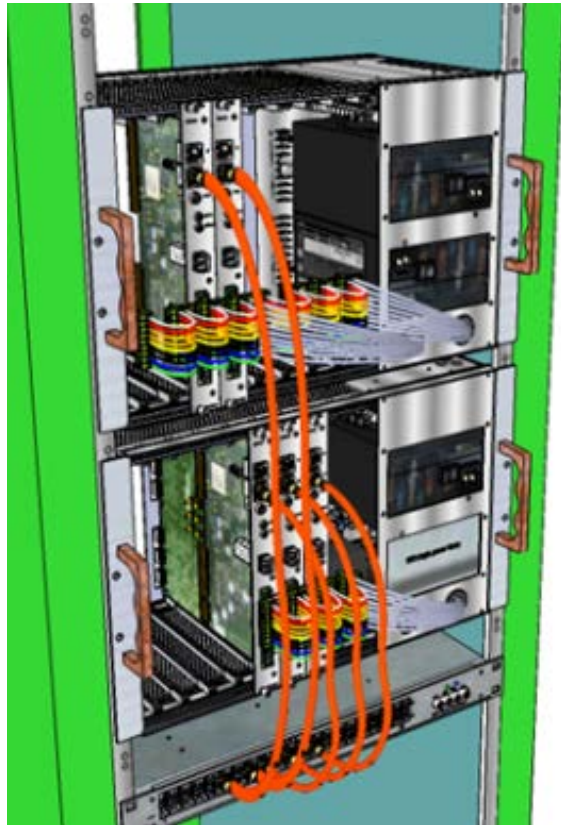
Root Analysis: Event statistics, distributions, cuts and fits

Online Monitoring: pulse-shape, x-y plots, pedestals, noise



Present and Future

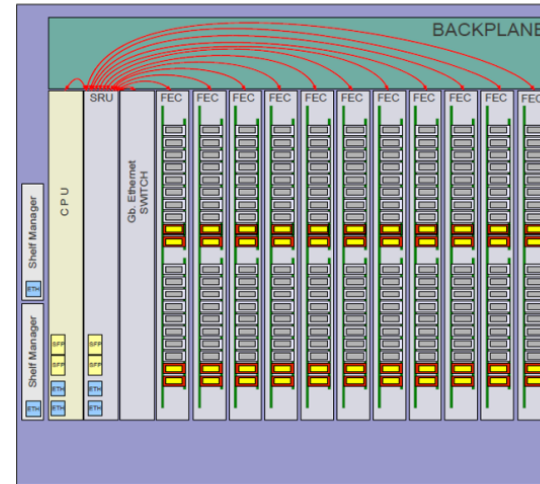
Current SRS implementation



Eurocrate build

- CERN store
- Rack systems**
- up to **5 Crates = 82 k channels**
- parallel FEC readout
- via 1 Gb DTC links (Data-Trigger-Control)
- 1 SRU / Rack (cluster concentrator)**
- 40 DTC links input
- 10 Gb to DAQ
- 1 Gb Slow Controls
- 1 Gb Monitoring
- 1 TTC for trigger

ATCA 14 slots Crate – SRS



- 11 FEC-ATCA blades
 - 64 ADC ch. per FEC board
 - 704 ADC channels in shelf
 - 67 k ! channels per shelf
 - 1 SRU blade in the shelf
 - remote programming
 - optional CPU in the shelf
- + 2 FEC-ATCA in no CPU&Switch

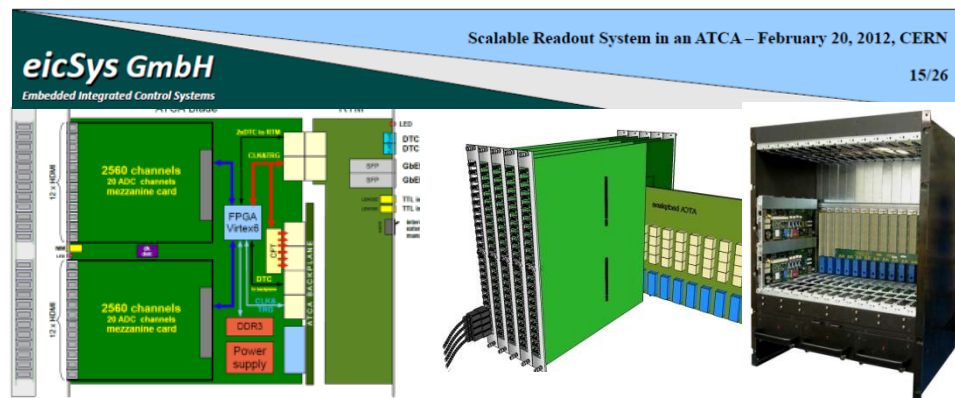


Figure 10. FEC-ATCA

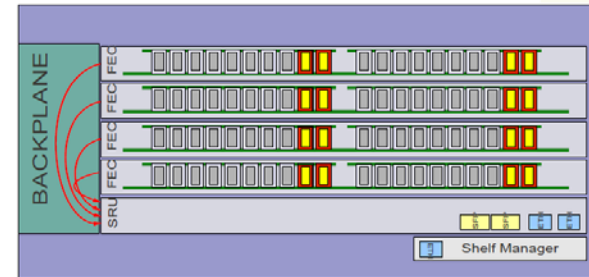
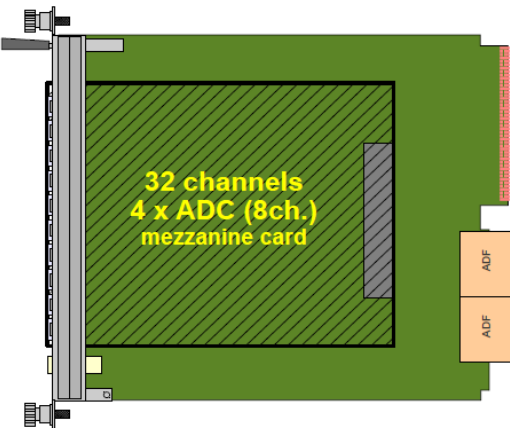
xTCA SRS (Small Systems)

mTCA.4 – FEC board

ATCA 5 slot – solution for a small system

Suitable for small systems
4-10 slots crate

- 4 FEC-ATCA blades
- 256 ADC channels in shelf
- 32768 channels per shelf
- 1 SRU blade in the shelf

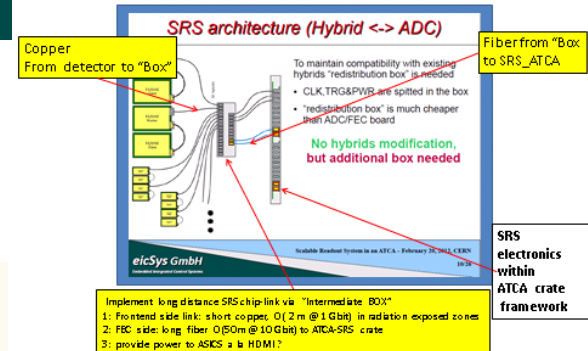


ATCA 2 slot – solution for a small system

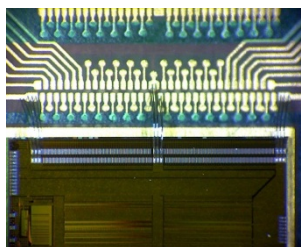
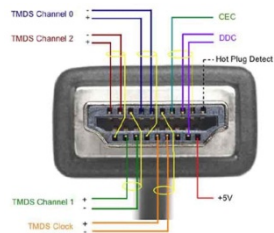
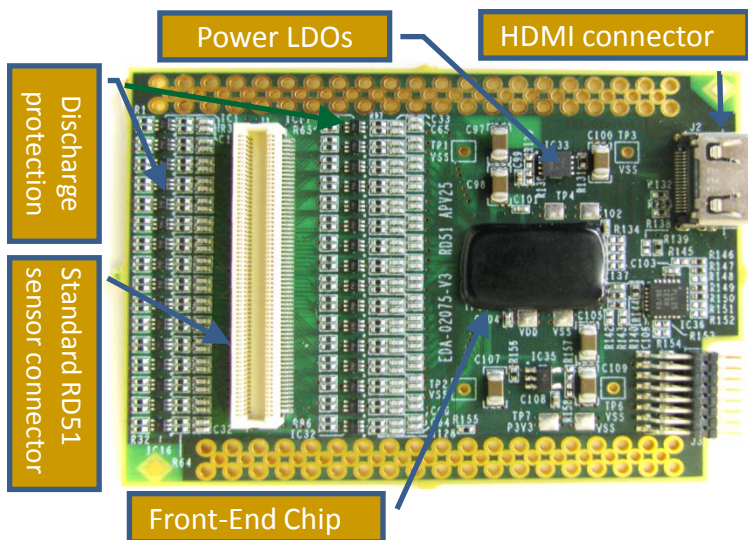
- 2 FEC-ATCA blades
- 128 ADC channels in shelf
- 16384 channels per shelf



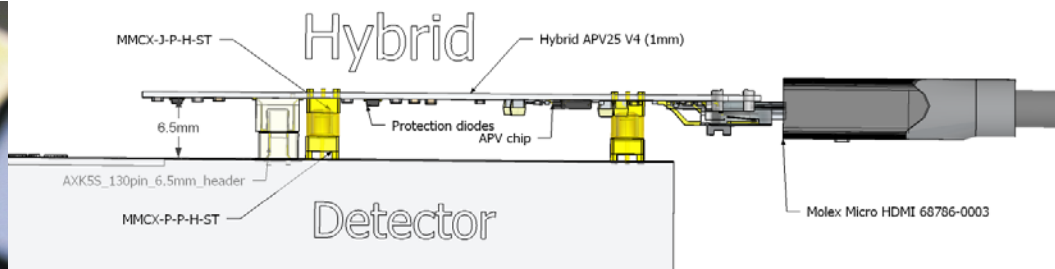
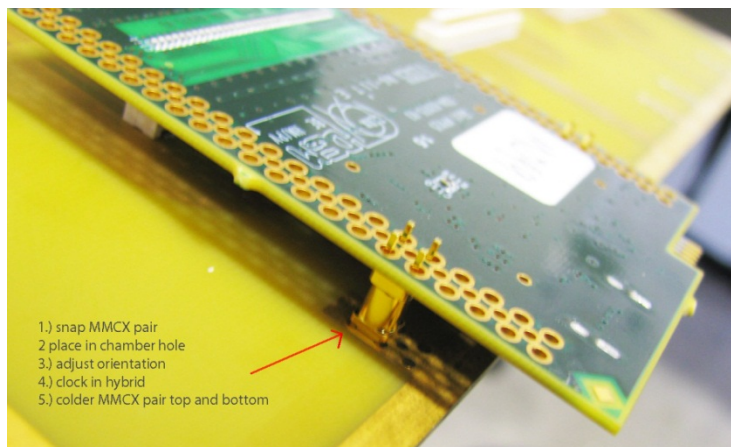
Upgrade plans for frontend



SRS Hybrids



- standard RD51 connector
- discharge protection
- micro-HDMI
 - clk & trg
 - data links
 - dcs (I2C)
- industry-ready design
- purchase through CERN store



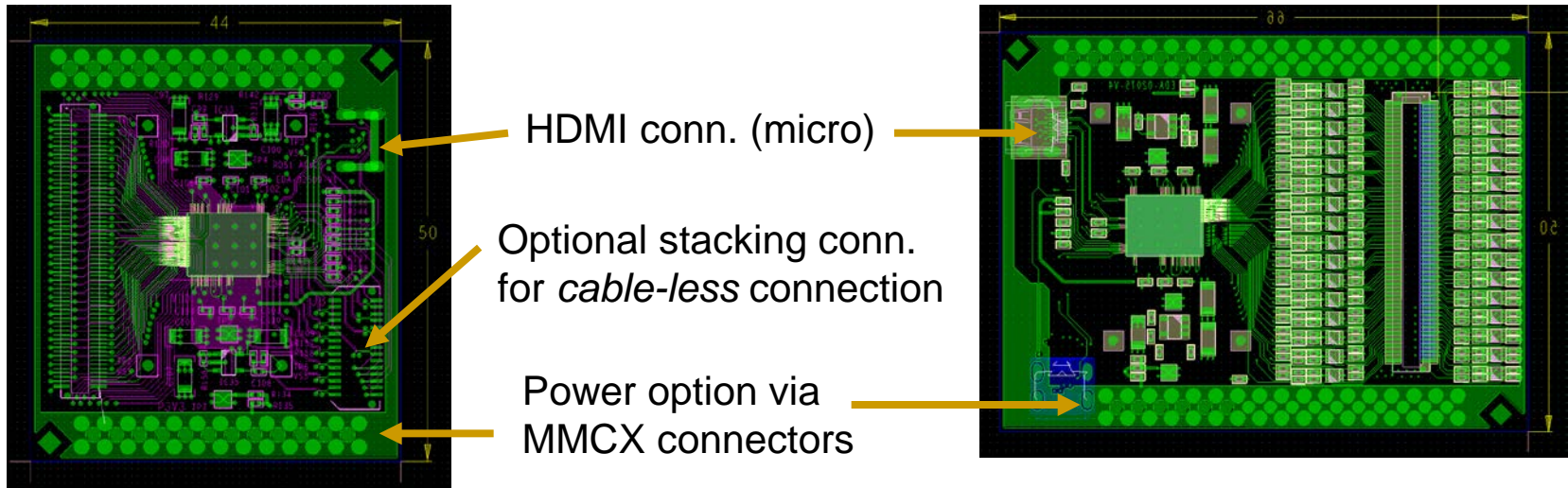
Samtec MMCX coax connector

GND connection (< 2mohm)
middle pin can be used for power
mechanical connection

VFAT2 Hybrid

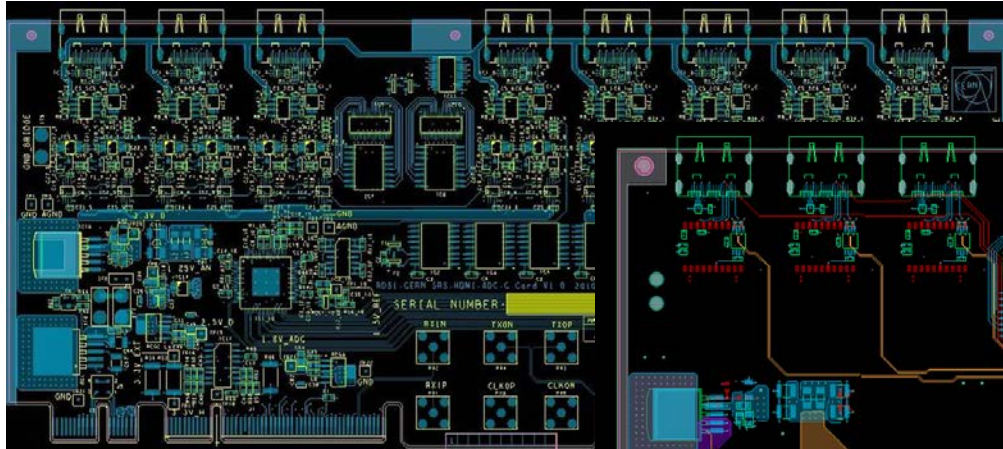
Short version – no input protection

Long version – full RD51 compatibility

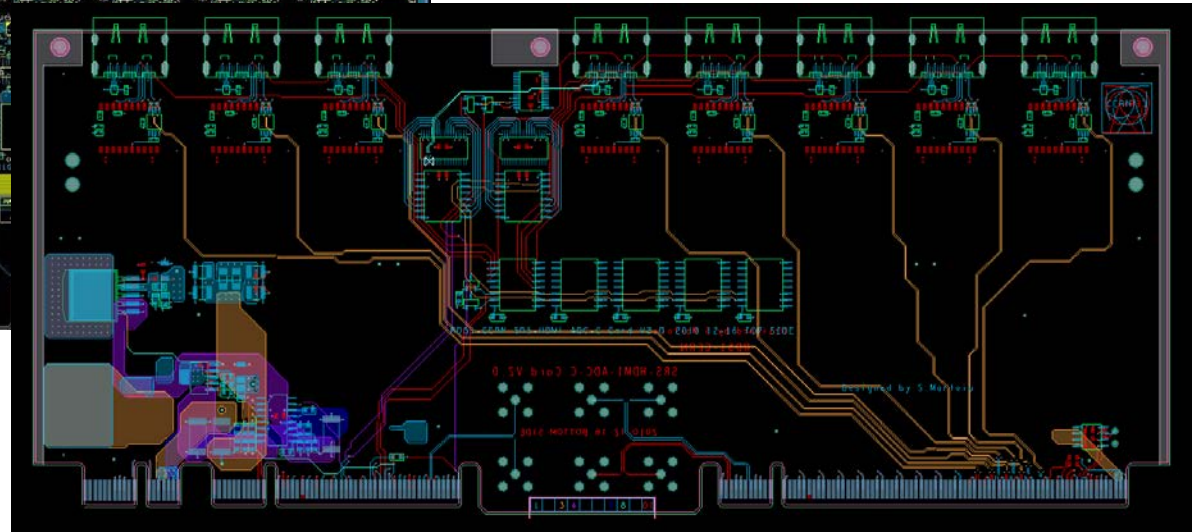


- schematic done
- layout under design (1 week)
- production and assembly (2-3 months (??))

Digital Adapter Card



Stripped down version of the ADC adapter



- schematic under design (1-2 weeks)
- layout (2 weeks)
- production (2 weeks – prototyping service (pool))
- assembly (1 – 1.5 months (??))

FW and SW

■ Firmware

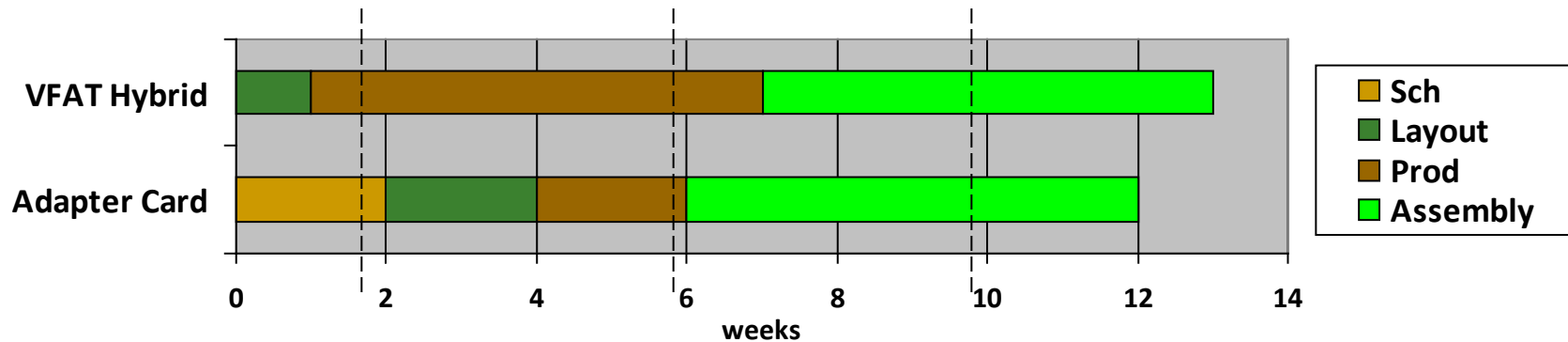
- ❑ Reuse of the SRS standard modules (GbEthernet, buffering, slow-control)
- ❑ Application specific fw – VFAT2 Frame decoder and Event Builder - considerably simpler than APV fw

■ Software

- ❑ Fast track: connecting existing LabView SRSDAQ to Turbo LV sw
- ❑ Other: DATE, CMS DAQ, ?

Summary

Tentative timeline:



Workload:

- Hardware
 - RD51: S. Martoiu (until end June 2012)
 - CERN DEM: William Billereau
 - External: Intrasys (layout), ELTOS/PCB-Pool (prod), Hybrid SA/other (assembly)
- SW & FW
 - ??

Summary

- Production of SRS base components externalized. Purchase via CERN store
- First pilot run due in mid 2012
- Design of VFAT2 SRS components well advanced. Production synchronized with VFAT2 and SRS availability
- Full VFAT2 SRS system (HW & SW) may be ready for Aug-Sep. 2012
- Possible upgrade path with xTCA, optical, GBT, ...
- A lot of interest from RD51 for VFAT2/VFAT3/GdSP

Spare

SRS Front-End Overview

Front-End Hybrids

(on-detector)

- APV25
- VFAT
- BEETLE

• ...

Chip-links

- HDMI
 - analog (APV/Beetle)
 - digital (VFAT/Beetle)
- optical (GBT, ...)
- ...

Front-end adapter

- ADC card
- digital FE card (VFAT)
- GBT receiver
- ...

Front-end FPGA card

(SRS standard)

modular firmware:

- SRS DAQ & control
- application specific FW

