General Electronics Planning

FE ASIC

Define electronics system for TP,
Formation of design teams.

ASIC design starts

FE ASIC design team
Approx. 8 man years
of design time
needed.

Submission of FE AISC (VFAT3/GdSP)

Readout systems

2011 Short Term :

VFAT2 , Turbo hardware and Labview DAQ software

2012

We are here.

Medium Term :

VFAT2 + SRS

Off Detector
uTCA development

2014

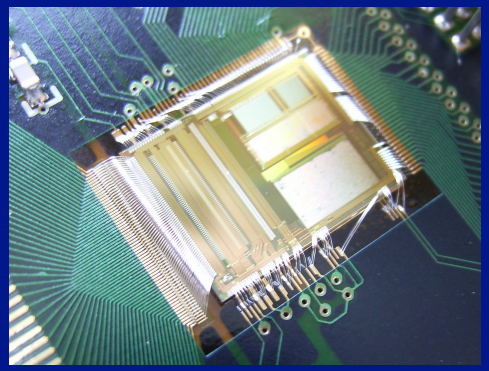
Long Term :

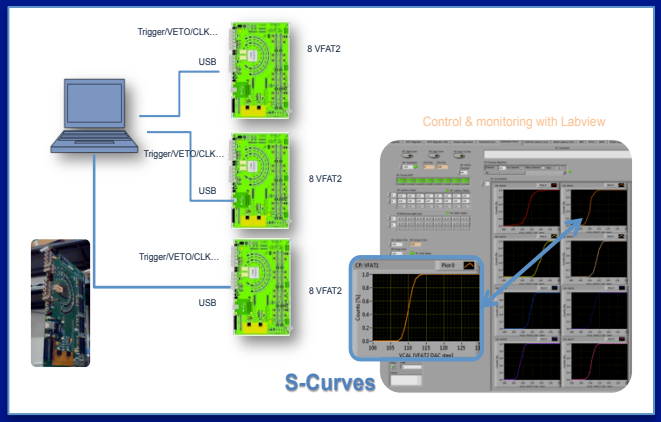
2015

Full and final system
On & Off detector electronics.
VFAT3/GdSP + GBT + uTCA system

VFAT2 + Turbo for 2012 Test beams

2012 test beams will operate with the same VFATs and DAQ system as last year. Namely VFAT2 + Turbo.





E. Oliveri …. (VFAT2 + Turbo system expert)

S. Colafranceschi & A.Marinov …. Physics

VFAT2 + SRS (status and 2012 plans)

VFAT2 chips – 24 wafers produced in 2011 .
Status : Dicing in Germany through Novapack.
Expected back beginning of June 2012.

SRS Hardware >>
VFAT2 hybrid design + SRS hardware …. S. Martoiu & H. Muller,
(including W. Billereau of the CERN PCB design service)

Production of hybrids by industry.

SRS firmware and software >>
DAQ software & firmware to be written >> Volunteers please.

Hybrid and SRS testing : S. Martoiu + ENHEP

VFAT2 + Integrated GEM PCB Development in 2012

Aim : Integrate power and all internal signals on a GEM PCB.

1) Eliminate most ground loops by supplying power via the GEM PCB instead of via individual cables. Help reduce common mode noise.
2) Remove all cables from the GEM detector due to space limitations.

Note : Multiple options will be available on the prototype, ie.

1) Power + Signals in HDMI cable.
2) Power via GEM PCB, Signals via cable.
3) Power + Signals via GEM PCB.

GEM Integrated PCB design …. A.Marinov, W. Billereau, R.de.Oliveira, A.C.Garcia, P.Aspell

Off detector uTCA
Homing in on the "Payload"

Homing in on the payload and what to do with it is very important for 2012.

This involves :

1) Determining the size and content of the data packet from the front-end.
2) Understanding what processing is required locally on each GLIB/AMC.
3) Deciding the content and data rates of trigger data shared between GLIB/AMC cards and their neigbours. Is a custom backplane required ?

This is an iterative process and requires the combined inputs from physics needs, trigger algorithms and electronics understanding of bandwidth limits.

Summary of 2012 plans for Read Out Systems + man power

Subject	Work	Personnel
VFAT2 + Turbo	No further development. Use in test beams.	E. Oliveri S. Colafranceschi A. Marinov
VFAT2 Hybrids	Design Testing	S. Martoiu CERN + ENHEP
SRS system	Hardware Design Software & Firmware	S. Martoiu ??
Integrated GEM PCB	Design Production	A.Marinov, W.Billereau, R.de.Oliveira, A.C.Garcia ?
uTCA	Understanding and homing in on system spec.	G.DeLentdecker, Y.Yang (ULB) CERN

Coordination P. Aspell