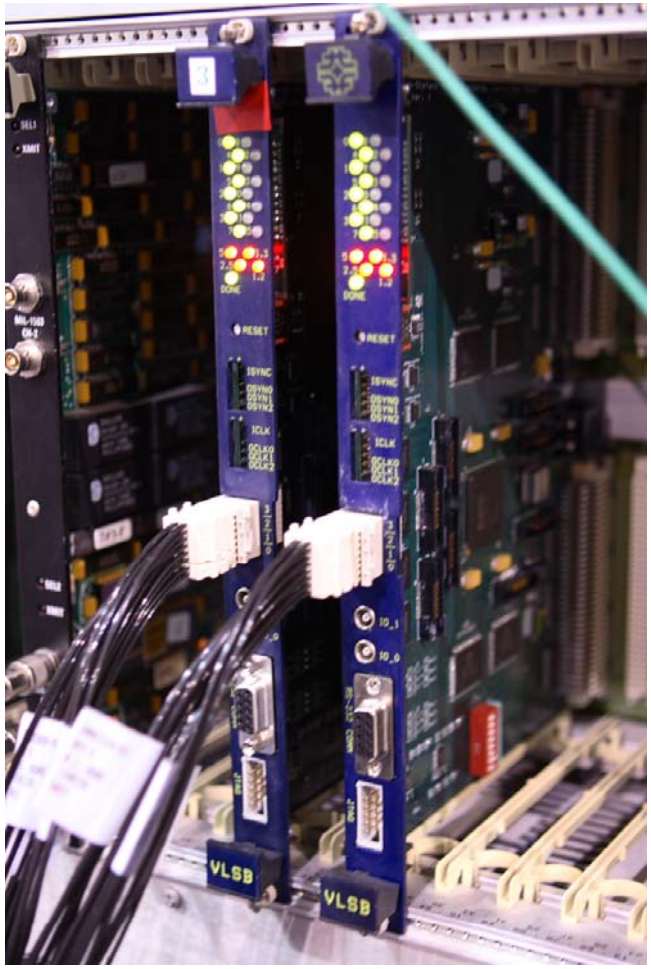
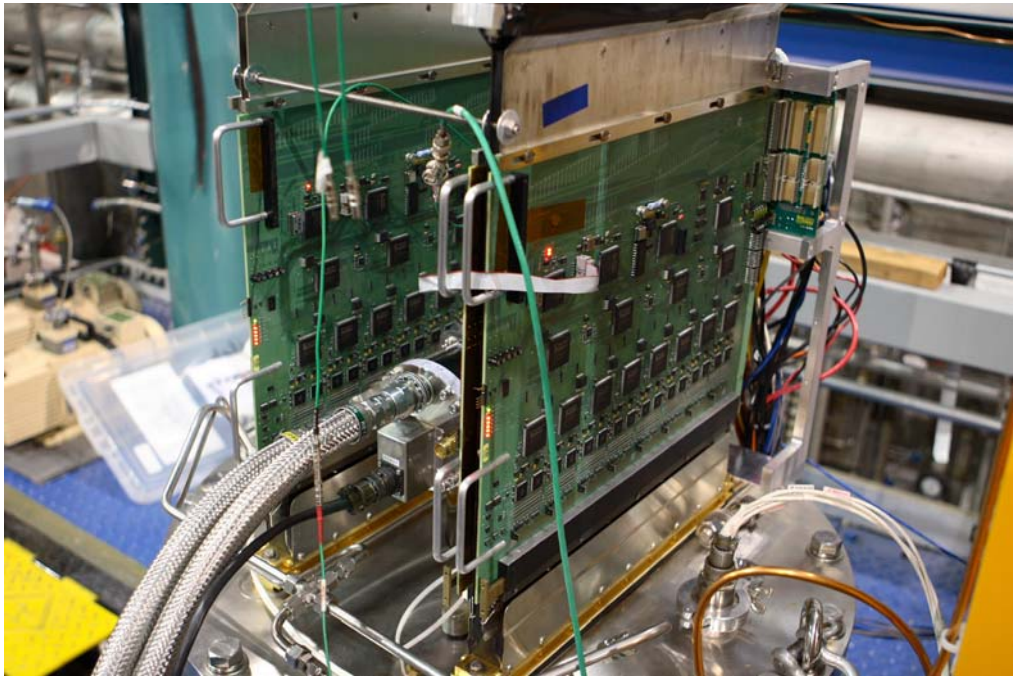
MICE Tracker Readout Update





- AFE IIt firmware development
- VLSB firmware development
- Hardware progress
- Summary

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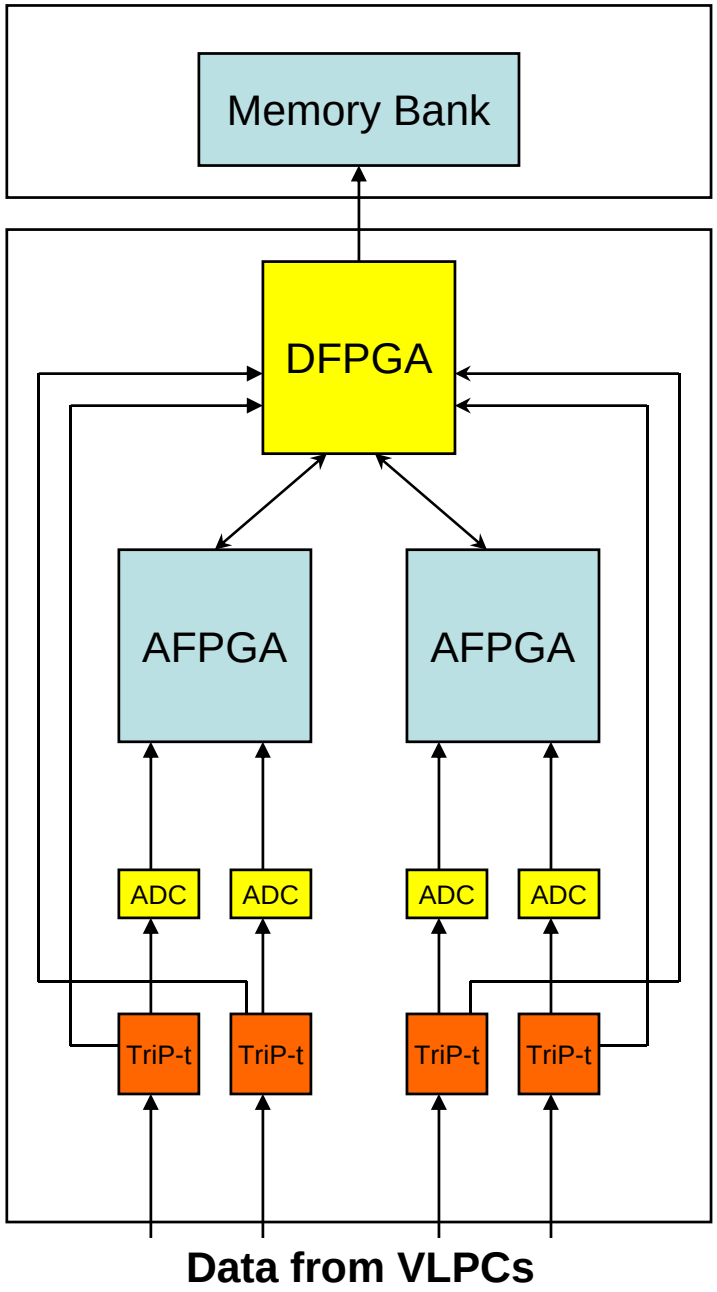
Terry Hart, MICE Tracker DAQ Workshop, July 24, 2007

Updates since July 12, 2007 Tracker Meeting shown in bold, italic, purple text.

AFE IIt Firmware Modifications



Modifications needed for data buffering

- Shorten time to digitize data
  - Zero suppression
  - End digitization series after last channel above threshold

    These are done.

- Protocol for data transfers between DFPGA and AFPGA
  - Bitmaps from DFPGA to AFPGA
  - Digitized data from AFPGA to DFPGA

    This is done.

- Buffer triggers in DFPGA FIFO

  This is done.

Immediate AFE IIt Firmware Tasks

- Synthesize AFGPA and DFPGA firmware modifications.
  - FNAL concentrating of AFPGA
  - RAL concentrating on DFPGA
  - Compilation of latest code versions to be done soon.
    - ***Kwame Bowie and Bill Luebke working on this at FNAL.***
    - ***DFPGA compilation successful***
    - ***AFPGA compilation underway***

- Test operation of entire board.
  - ***Signal timing needs to be checked.***
  - Check compatibility of modified firmware with existing firmware.
  - ChipScope signal analyzer will check if signals match simulations.
  - ***Testing will follow successful synthesis immediately.***

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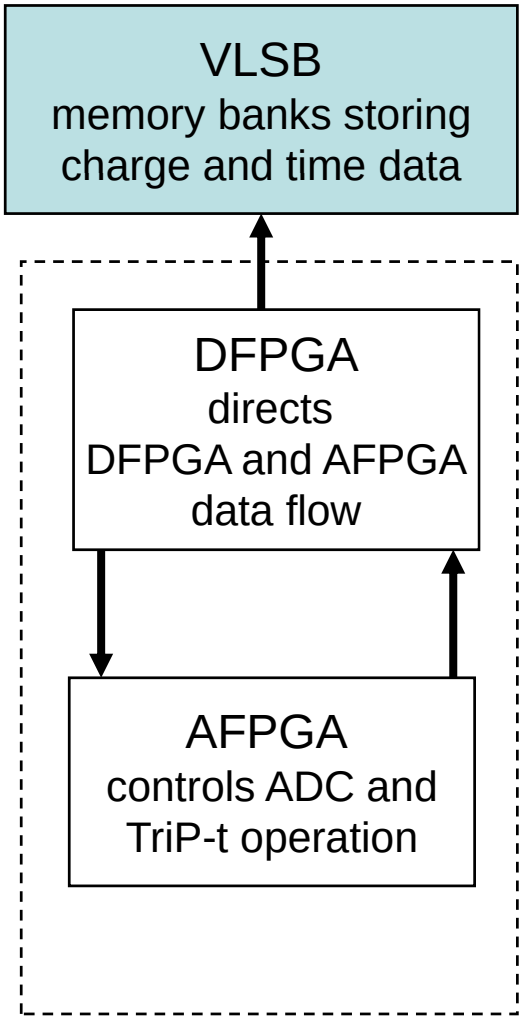
VLSB Firmware

- Main task: set up initial signals correctly for simulation
  - Documentation and expertise are limited
    - ***Not as dire as previously thought; Bill Haynes at FNAL very helpful.***
  - Need to dig into code
    - ***My main work over the past week***
  - ***Simulations of unmodified firmware completed.***
    - ***Access to computer with Aldec simulation tools***
    - ***Compile firmware***
    - ***Set up initial signals and run simulations until input data and address are written to memory bank addresses.***

- Modifications for MICE
  - Event counter during spill ***(will check with Malcolm)***
  - Fast clear of VLSB memory ***(follow up with Bill Haynes)***
  - Overwrite memory addresses when there's null data so that data are stored in continuous memory blocks.

  (immediate task now that simulation works with original code)
  - Enable Direct Memory Access block transfer ***(done)***



Hardware Updates

- VLSB Boards
  - 9 boards are built (to be spares),
  - 15 more to be made
    - Supervision of VLSB board assembly from FNAL CD to FNAL APC hasn't been smooth.
    - Process of VLSB board assembly being worked out.

- AFE IIt boards/Cryostat
  - Data taken for 2 of 4 production cryostats (8 boards assigned).
  - Preliminary assignment of 7 of 8 boards made for 2 remaining cryostats.
  - 8 spare boards remaining after 15 assigned boards

(23 total AFE IIt boards for MICE)

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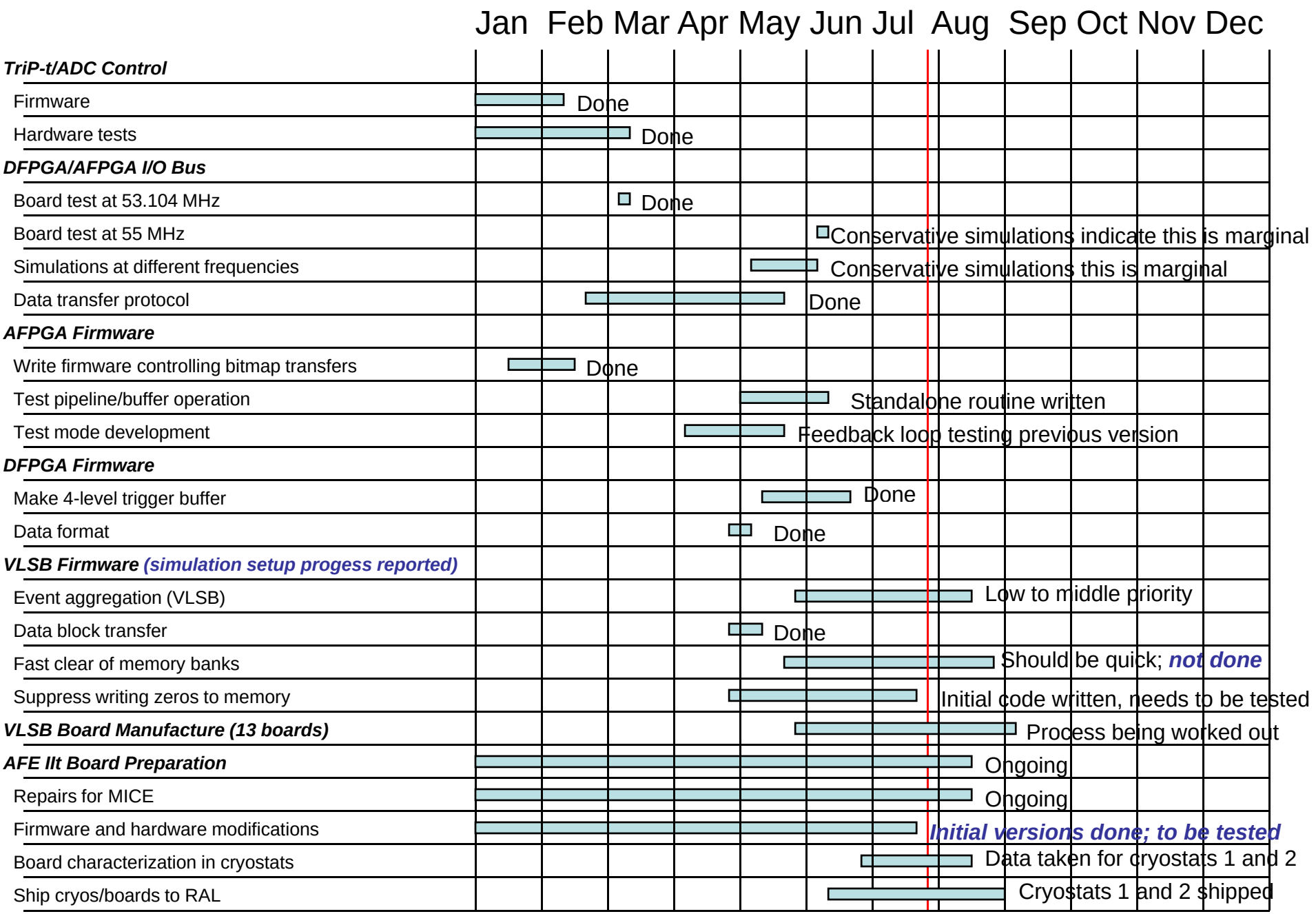
Jan Feb Mar Apr May Jun Jul Aug Sep Oct Nov Dec
TriP-t/ADC Control
Firmware
Done
Hardware tests
Done
DFPGA/AFPGA I/O Bus
Board test at 53.104 MHz
Done
Board test at 55 MHz
Conservative simulations indicate this is marginal
Simulations at different frequencies
Conservative simulations this is marginal
Data transfer protocol
Done
AFPGA Firmware
Write firmware controlling bitmap transfers
Done
Test pipeline/buffer operation
Standalone routine written
Test mode development
Feedback loop testing previous version
DFPGA Firmware
Make 4-level trigger buffer
Done
Data format
Done
VLSB Firmware (simulation setup progess reported)
Event aggregation (VLSB)
Low to middle priority
Data block transfer
Done
Fast clear of memory banks
Should be quick; not done
Suppress writing zeros to memory
Initial code written, needs to be tested
VLSB Board Manufacture (13 boards)
Process being worked out
AFE IIt Board Preparation
Ongoing
Repairs for MICE
Ongoing
Firmware and hardware modifications
Initial versions done; to be tested
Board characterization in cryostats
Data taken for cryostats 1 and 2
Ship cryos/boards to RAL
Cryostats 1 and 2 shipped

Summary

- First version of AFE IIt firmware development to enable trigger buffering done
- Analysis of AFE IIt signals to be started soon.
  - ***Compilation of DFPGA code done.***
  - ***Compilation of AFPGA code to be done soon.***
  - ***Tests of timing and how close signals are to simulation results to start immediately.***
- VLSB firmware development almost done.
  - ***Simulation of initial firmware done (This was the hard part.)***
  - ***Simulation of our modifications will follow immediately.***
- Almost all AFE IIt boards for MICE are available ***(will check on this)***.
- VLSB board assembly for MICE stalled for now ***(will check on this)***.

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