AFEIIt Initialisation and Control

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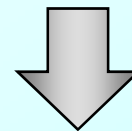
AFEIIt Software

- Currently using Excel spreadsheets to initialise/control AFEIIt boards

- Aim is to translate VB routines into DATE compatible C code for slow control and monitoring in final system

- Work commenced on 22nd June…

Core Software Modules

- ## DATE "Equipment Types"

  - **SBS810**: Arms & provides interface to SBS 810 VME adaptor (replaces CAEN interface in existing DATE package)

  - **AFEIIt**: Arms & reads out AFEIIt hardware - one instance for each AFEIIt board in system

- ## Utility modules

  - **MIL1553**: Provides read/write interface via MIL1553 card

  - **AFEIItUtils**: Low level FPGA & TriPt access routines + basic utility and error checking functions

  - **AFEIItInterface**: High level configuration and readout functions

  - **ErrorHandler**: Macros to simplify error handling & reporting

AFEIIt Parameters

- Attempt has been made to ensure that all AFEIIt parameters are configurable within DATE

  – Even debug settings (i.e. charge injection setup)

- Total of 230 parameters for each board (so far)

- Includes flag to disable 'arming'

  – During normal operation boards only need to be initialised at power up, not every run

Usage 'Outside' DATE Framework

- All AFEIIt code written within DATE framework

- However, useful to test modules without DATE paraphernalia (GUIs, run control, logger…)

- Have set up build environment enabling standalone programs to access all AFEIIt functionality with no DATE involvement (from user perspective)

- Additional modules simplify 'standalone' operation:

  - **MsgHandler**:   Simple macros to permit switching between DATE logger and output to screen (with debugging info) for all messages

  - **SBS810Parameters**:

  - **AFEIItParameters**:   Functions for creating & loading/saving (to file) DATE style parameter structures

Initialisation & Readout Commands

- Initialisation (ArmAFEIIt)

  - Turn FPGAs on

  - Program Analog FPGAs

  - Program Digital FPGAs

  - Configure clock generator

  - Configure Analog FPGAs

  - Configure Digital FPGAs

  - Power on TriPts

  - Configure TriPts

  Implemented

  - Configure VLPC bias offsets

  - Configure VLPC temperature control

- Readout (ReadEventAFEIIt)

  To do...

  - Read VLPC temperature & heating power

~80% Complete

Initial Testing

- Evaluation with actual hardware delayed, due to unavailability of Linux SBS drivers

    - Hardware poorly supported, binary rpm packages incompatible with modern kernels

    - Requested src rpm, but considered 'proprietary' software $\Rightarrow$ had to wait for manufacturer to process licensing agreement

    - Received src rpm last Friday – failed to build…

    - Managed to identify/update all depreciated references, now appears to function correctly

- Initial tests demonstrate AFEIIt code fundamentally operational – few tweaks/bug fixes required

Summary & Outlook

- Work on translating AFEIIt initialisation & slow control routines from Excel to DATE compatible C is well underway

- Development environment is in place, most initialisation functions implemented

- Hardware tests now possible with working SBS driver – some work required…

- Expect AFEIIt code to be complete & tested by the 3rd week of August